

IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

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Thank you for your cooperation and understanding,

WeEn Semiconductors

1. General description

Planar passivated sensitive gate four quadrant triac in a TO252 (DPAK) surface-mountable plastic package intended for use in general purpose bidirectional switching and phase control applications. This sensitive gate "series E" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Direct triggering from low power drivers and logic ICs
- High blocking voltage capability
- Low holding current for low current loads and lowest EMI at commutation
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate
- Surface-mountable package
- Triggering in all four quadrants

3. Applications

- General purpose motor controls
- General purpose switching

4. Quick reference data

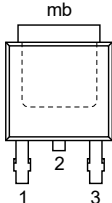
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 102\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	65	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	-	71	A
T_j	junction temperature		-	-	125	°C
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	-	2.5	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7	-	4	10	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	5	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	11	25	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	2.5	20	mA
V_T	on-state voltage	$I_T = 10\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	1.3	1.65	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	-	50	-	V/ μs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 DPAK (TO252N)	 sym051
2	T2	main terminal 2		
3	G	gate		
mb	T2	mounting base; main terminal 2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT137S-600E	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	TO252N

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{mb}} \leq 102\text{ }^{\circ}\text{C}$; Fig. 1; Fig. 2; Fig. 3	-	8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 4; Fig. 5	-	65	A
		full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 16.7\text{ ms}$	-	71	A
I^2t	I^2t for fusing	$t_{\text{p}} = 10\text{ ms}$; SIN	-	21	A^2s
di_{T}/dt	rate of rise of on-state current	$I_{\text{G}} = 20\text{ mA}$	-	50	$\text{A}/\mu\text{s}$
			-	50	$\text{A}/\mu\text{s}$
		$I_{\text{G}} = 50\text{ mA}$	-	10	$\text{A}/\mu\text{s}$
		$I_{\text{G}} = 20\text{ mA}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_{j}	junction temperature		-	125	$^{\circ}\text{C}$

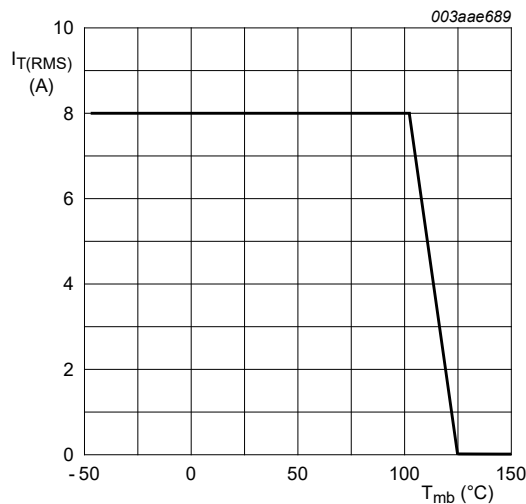
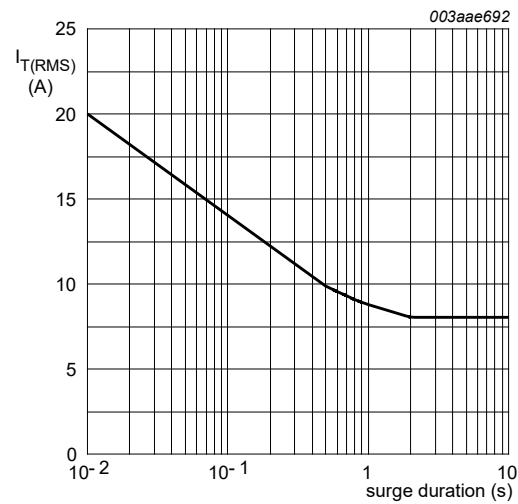


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



$f = 50\text{ Hz}$
 $T_{\text{mb}} \leq 102\text{ }^{\circ}\text{C}$

Fig. 2. RMS on-state current as a function of surge duration; maximum values

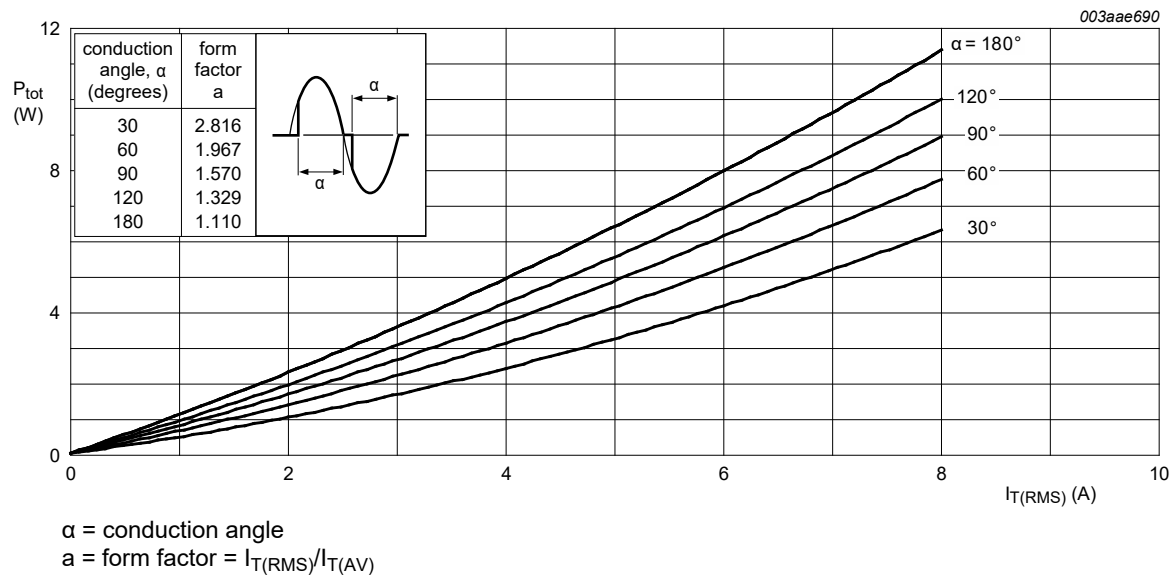


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

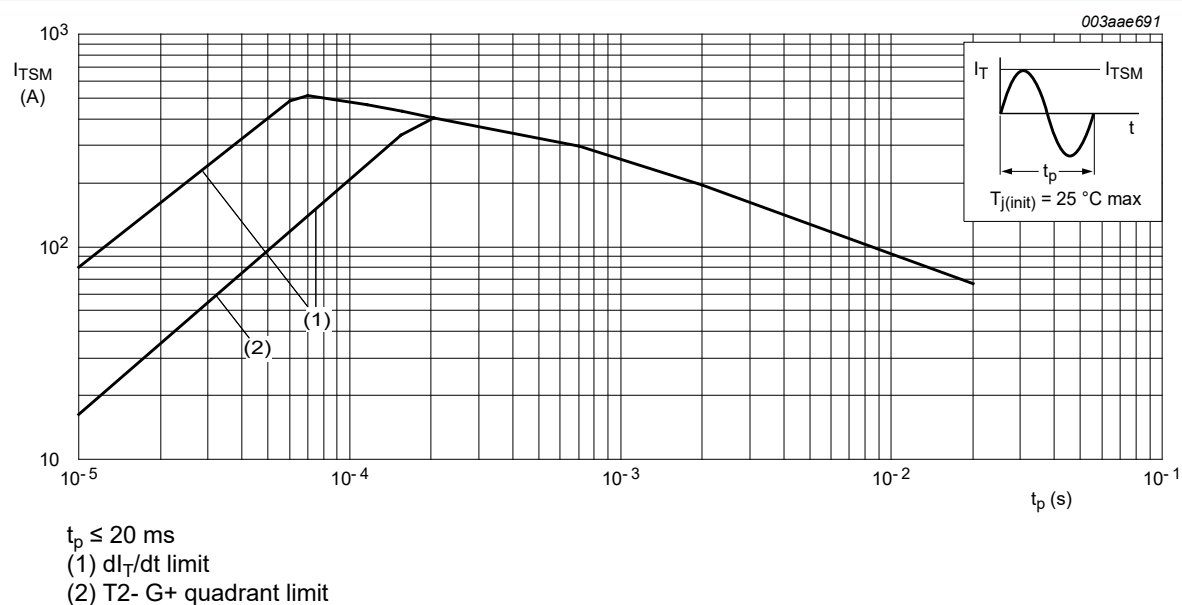
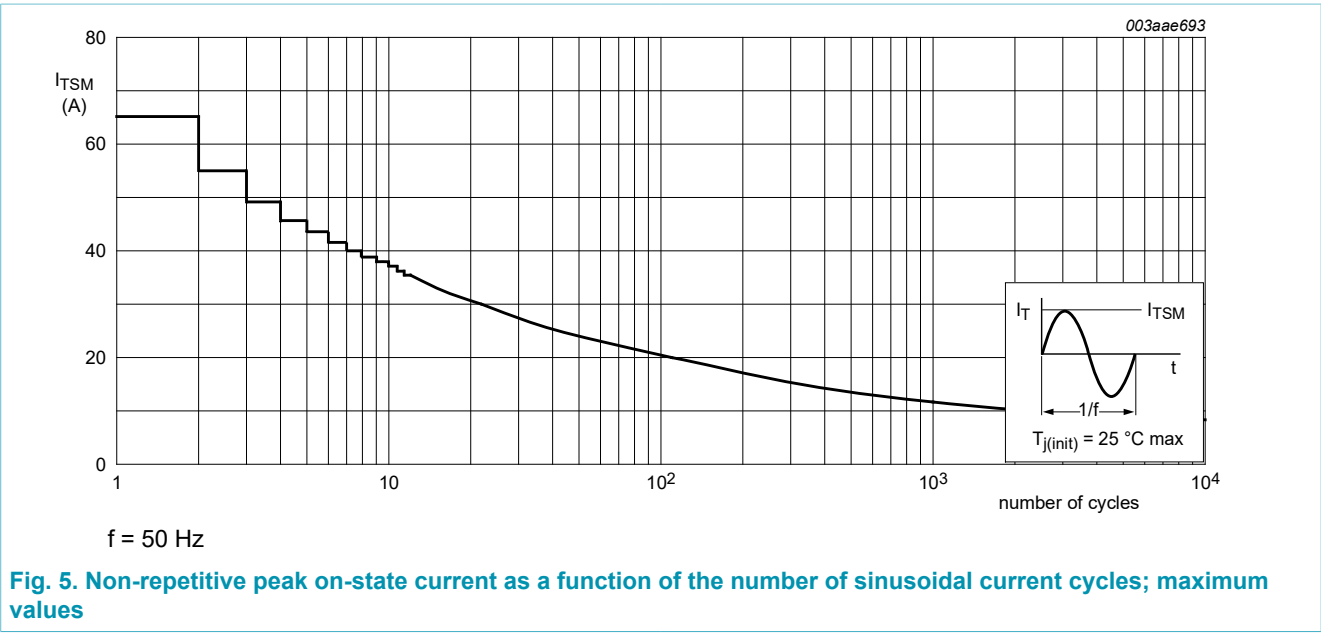


Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	half cycle; Fig. 6	-	-	2.4	K/W
		full cycle; Fig. 6	-	-	2	K/W
R _{th(j-a)}	thermal resistance from junction to ambient free air	PCB (FR4) mounted; minimum pad sizes	-	75	-	K/W

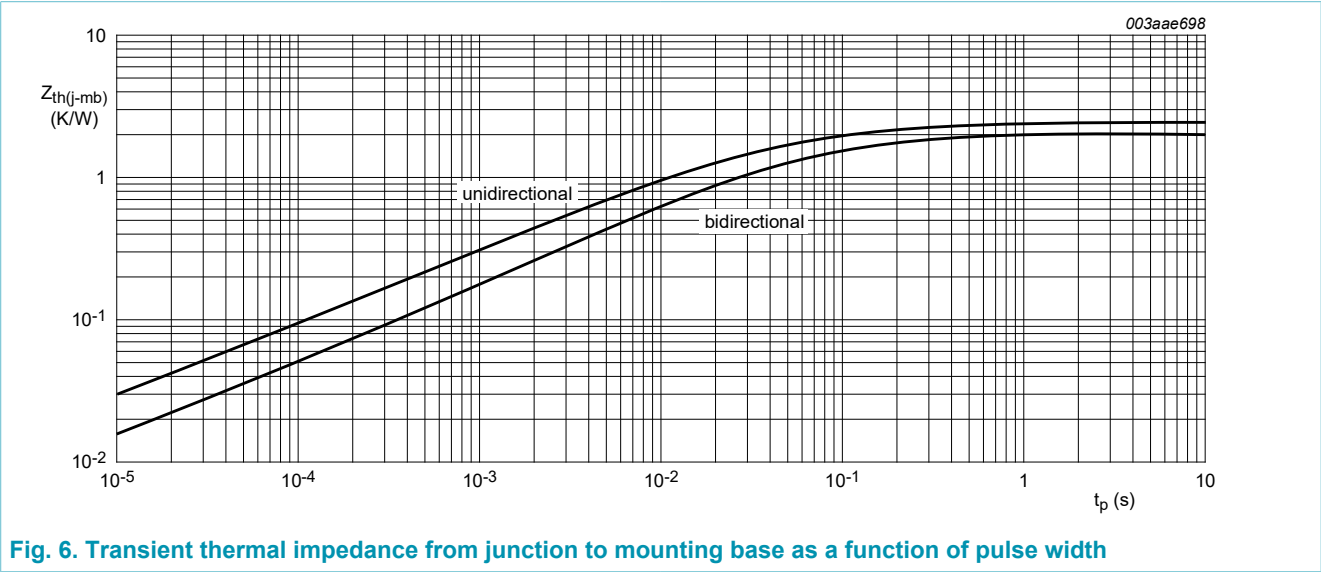
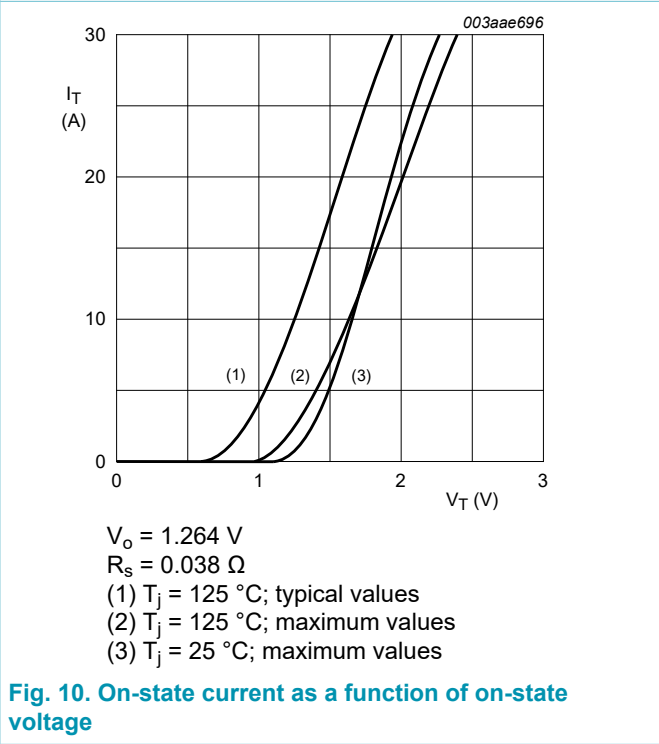
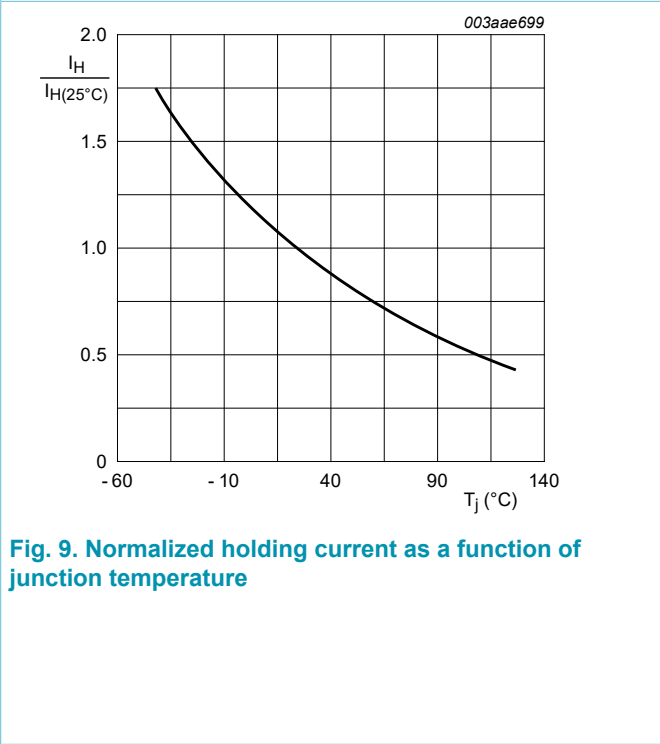
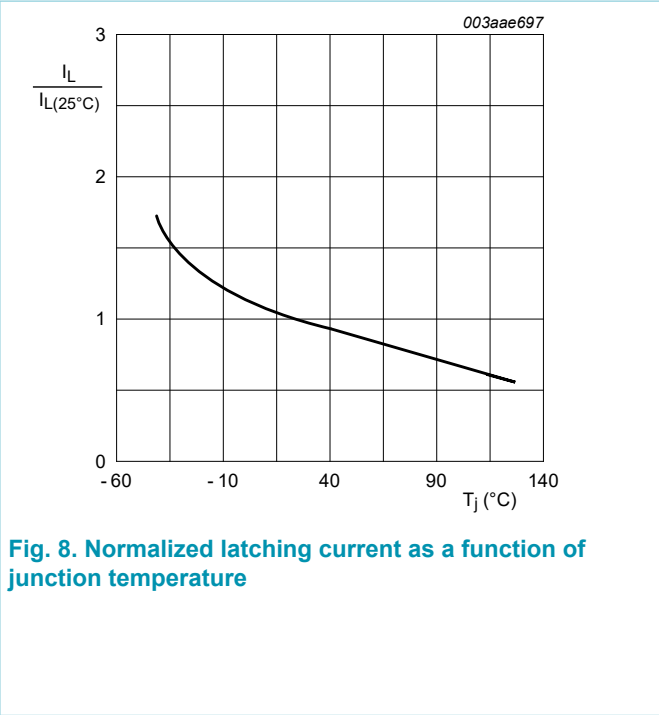
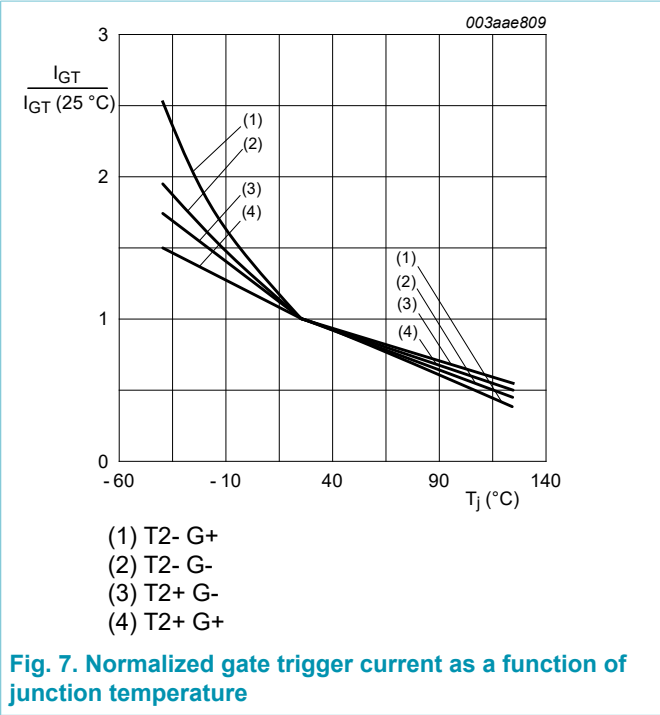


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7		-	2.5	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7		-	4	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7		-	5	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7		-	11	25	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8		-	3	25	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8		-	14	35	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8		-	3	25	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8		-	4	35	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9		-	2.5	20	mA
V_T	on-state voltage	$I_T = 10\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10		-	1.3	1.65	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11		-	0.7	1	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 11		0.25	0.4	-	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit		-	50	-	V/ μs
t_{gt}	gate-controlled turn-on time	$I_{TM} = 12\text{ A}$; $V_D = 600\text{ V}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 5\text{ A}/\mu\text{s}$		-	2	-	μs



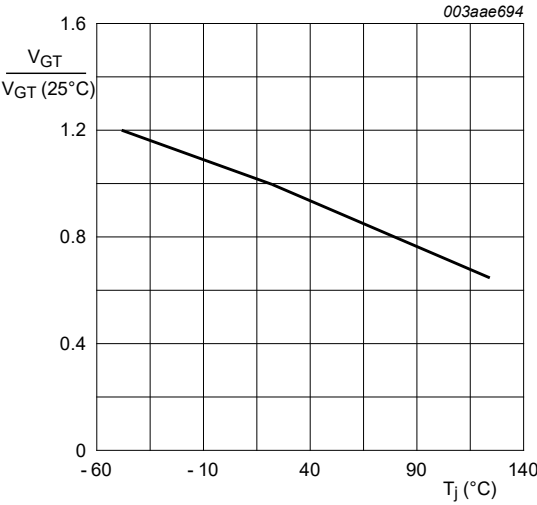


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

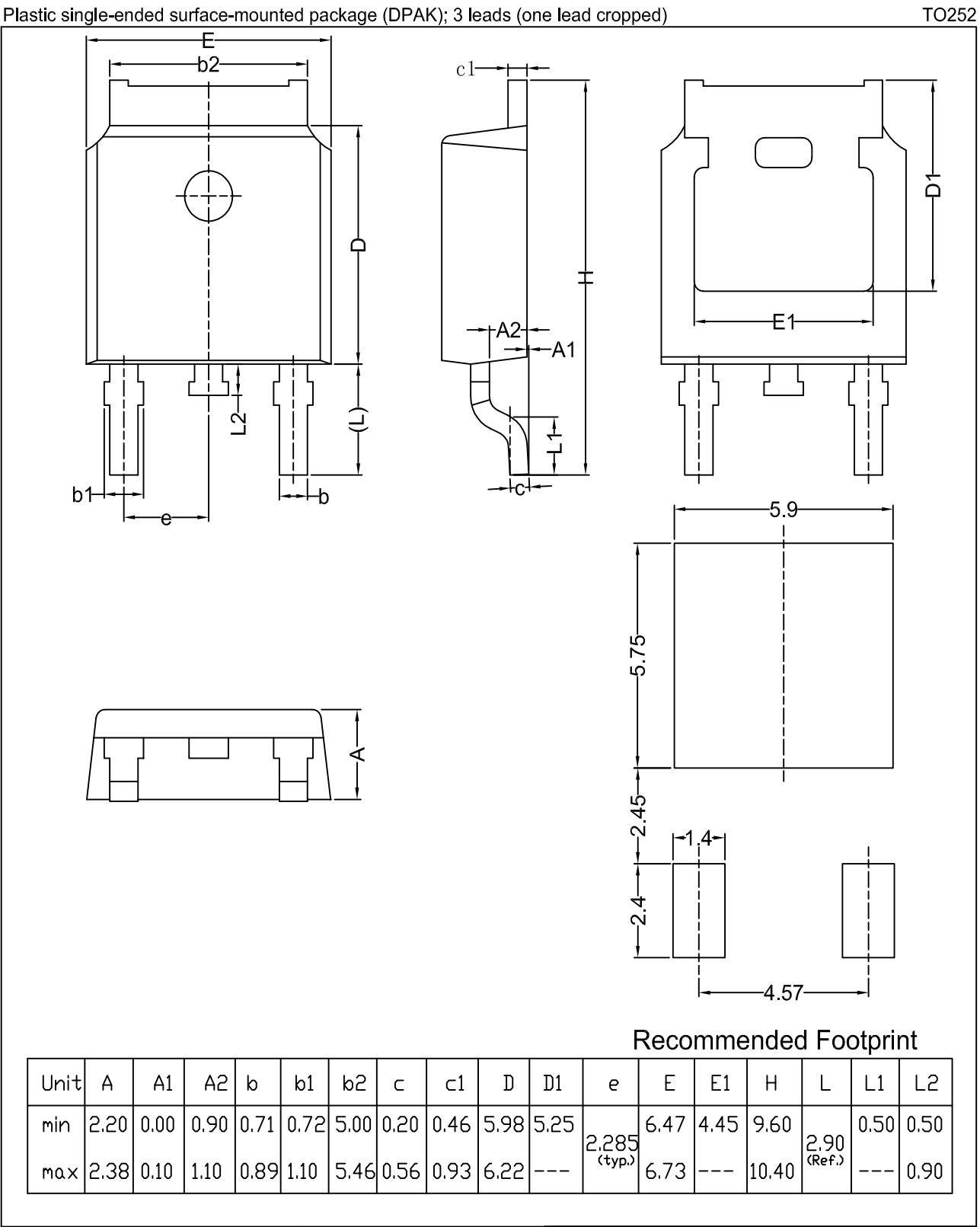


Fig. 12. Package outline DPAK (TO252N)

11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 1 November 2016
