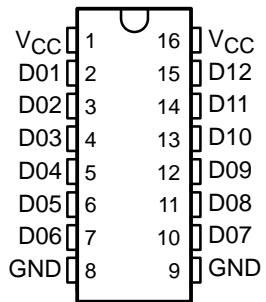


- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current to 200 mA
- 12-Bit Array Structure Suited for Bus-Oriented Systems

description/ordering information

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 12-bit high-speed Schottky diode array suitable for clamping to V_{CC} and/or GND.

D, N, NS, OR PW PACKAGE
(TOP VIEW)

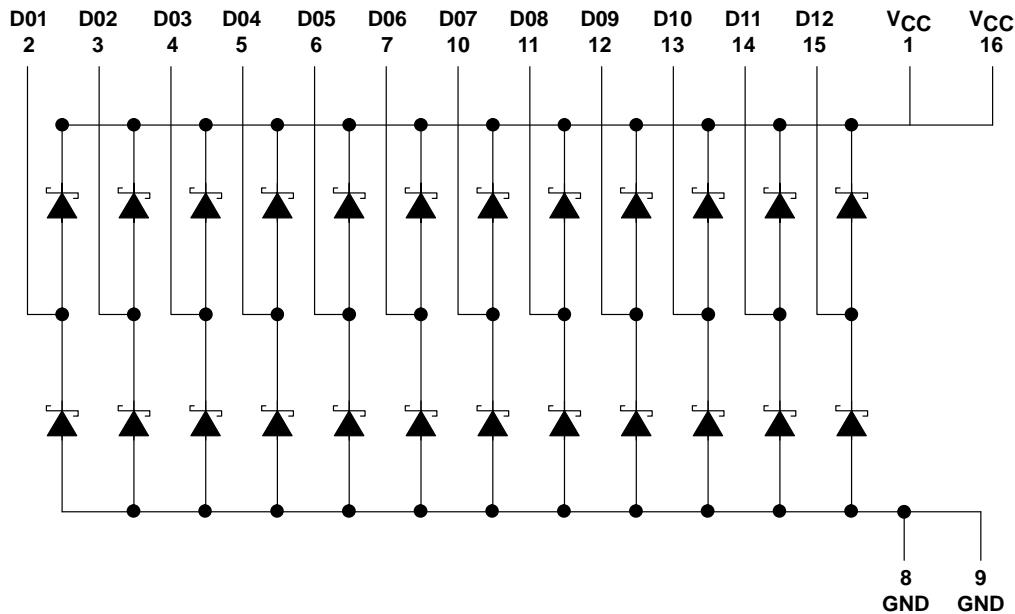


ORDERING INFORMATION

| T _A | PACKAGE [†] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|---------------|-----------------------|------------------|
| 0°C to 70°C | PDIP – N | Tube | SN74S1051N | SN74S1051N |
| | SOIC – D | Tube | SN74S1051D | S1051 |
| | | Tape and reel | SN74S1051DR | |
| | SOP – NS | Tape and reel | SN74S1051NSR | 74S1051 |
| | TSSOP – PW | Tape and reel | SN74S1051PWR | S1051 |

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

schematic diagrams



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74S1051
12-BIT SCHOTTKY BARRIER DIODE
BUS-TERMINATION ARRAY

SDLS018B – SEPTEMBER 1990 – REVISED MARCH 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Operating free-air temperature range 0°C to 70°C

Storage temperature range, T_{sta} -65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

† These values apply for $t_W \leq 100 \mu s$, duty cycle $\leq 20\%$.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 2)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | |
|-----------------|------------------------|---------------------------------|-------------------------|------|------|------|------|--|
| VF | Static forward voltage | To V _{CC} | I _F = 18 mA | 0.85 | 1.05 | 1.05 | V | |
| | | | I _F = 50 mA | 1.05 | 1.3 | 1.3 | | |
| | From GND | I _F = 18 mA | 0.75 | 0.95 | 0.95 | | | |
| | | | I _F = 50 mA | 0.95 | 1.2 | 1.2 | | |
| V _{FM} | Peak forward voltage | | I _F = 200 mA | 1.45 | 1.45 | 1.45 | V | |
| IR | Static reverse current | To V _{CC} | V _R = 7 V | 5 | 5 | 5 | μA | |
| | | From GND | | 5 | 5 | 5 | | |
| C _t | Total capacitance | V _R = 0 V, f = 1 MHz | | 8 | 16 | 16 | pF | |
| | | V _R = 2 V, f = 1 MHz | | 4 | 8 | 8 | | |

§ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

| PARAMETER | | TEST CONDITIONS | MIN | TYP \pm | MAX | UNIT |
|-----------|----------------------------|---|-----|-----------|-----|------|
| I_x | Internal crosstalk current | Total I_F current = 1 A, See Note 3 | | 0.8 | 2 | mA |
| | | Total I_F current = 198 mA, See Note 3 | | 0.02 | 0.2 | |

§ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

NOTE 3: I_v is measured under the following conditions with one diode static, all others switching:

Switching diodes: $t_w = 100 \mu s$, duty cycle = 20%

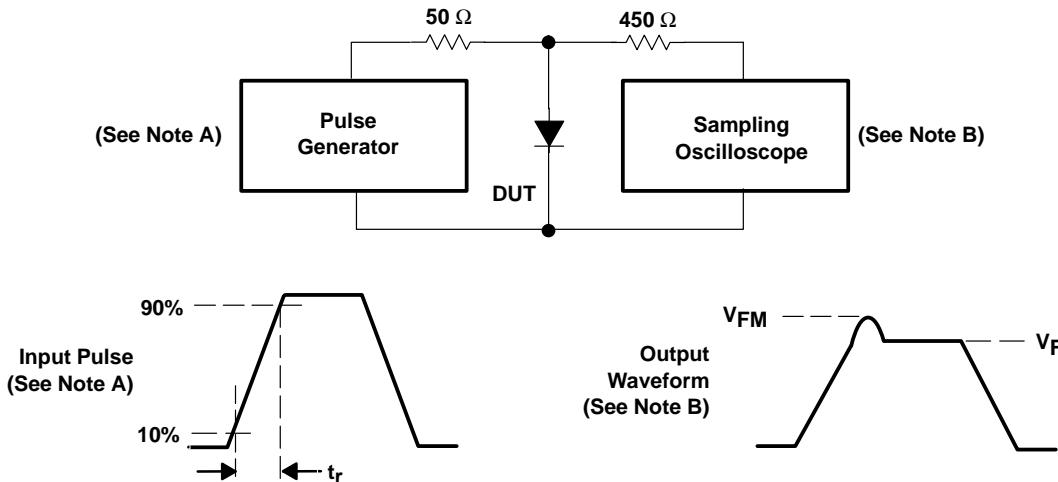
Switching diode: $V_W = 5 \text{ V}$

The static diode input current is the internal crosstalk current, I_v .

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

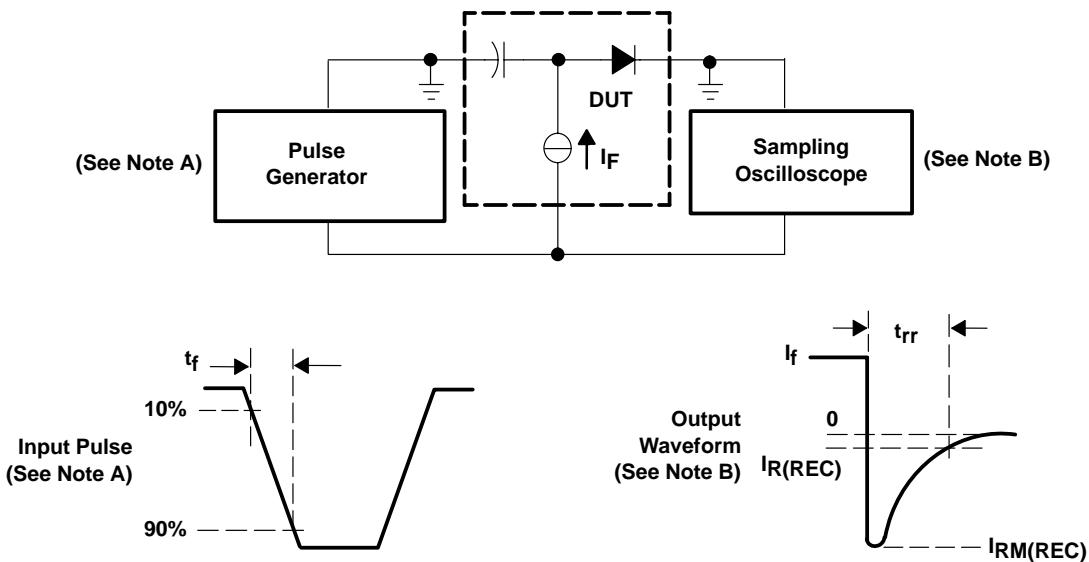
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--|-----|-----|-----|------|
| t_{rr} | Reverse recovery time $I_F = 10 \text{ mA}, \quad I_{RM(REC)} = 10 \text{ mA}, \quad I_{R(REC)} = 1 \text{ mA}, \quad R_L = 100 \Omega$ | | 8 | 16 | ns |

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_r = 20\ \text{ns}$, $Z_O = 50\ \Omega$, freq = 500 Hz, duty cycle = 1%.
 B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq 350\ \text{ps}$, $R_i = 50\ \Omega$, $C_i \leq 5\ \text{pF}$.

Figure 1. Forward Recovery Voltage



NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_f = 0.5\ \text{ns}$, $Z_O = 50\ \Omega$, $t_w \geq 50\ \text{ns}$, duty cycle = 1%.
 B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq 350\ \text{ps}$, $R_i = 50\ \Omega$, $C_i \leq 5\ \text{pF}$.

Figure 2. Reverse Recovery Time

SN74S1051
12-BIT SCHOTTKY BARRIER DIODE
BUS-TERMINATION ARRAY

SDLS018B – SEPTEMBER 1990 – REVISED MARCH 2003

APPLICATION INFORMATION

Large negative transients at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1051 diode termination array helps suppress negative transients caused by transmission-line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split-resistor or Thevenin-equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver reduce negative transients, but they also can increase propagation delays down the line because a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current when the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. Typical current-versus-voltage curves for the SN74S1051 are shown in Figures 3 and 4.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 5 was evaluated. The resulting waveforms with and without the diode are shown in Figure 6.

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when the diode arrays are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

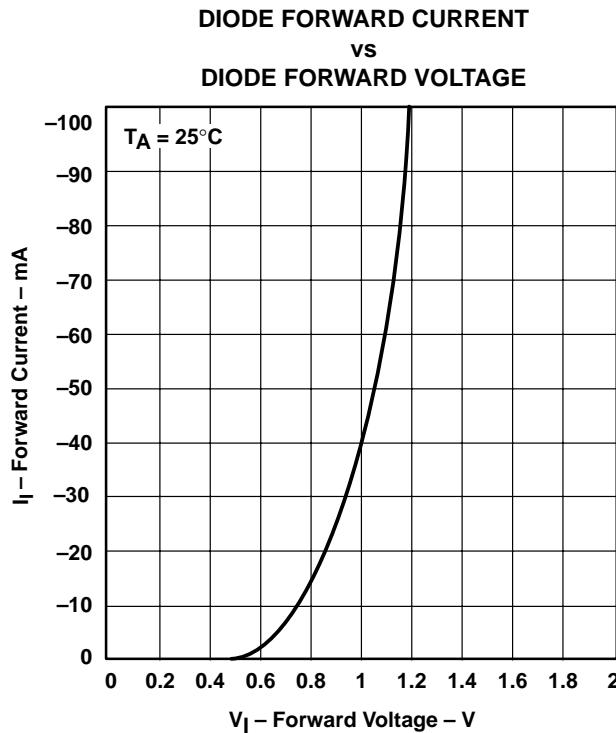


Figure 3. Typical Input Current vs Input Voltage (Lower Diode)

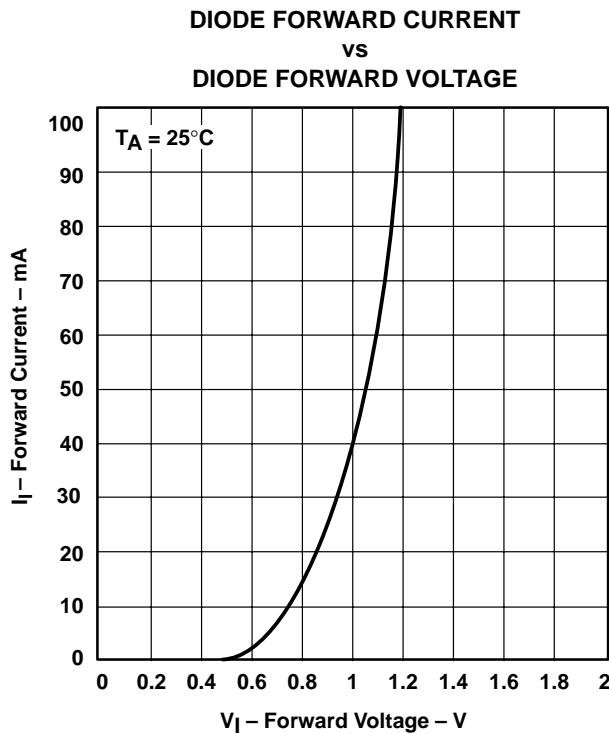


Figure 4. Typical Input Current vs Input Voltage
(Upper Diode)

APPLICATION INFORMATION

$$Z_0 = 50 \Omega$$

Length = 36 in.

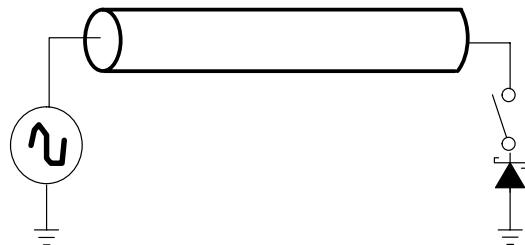


Figure 5. Diode Test Setup

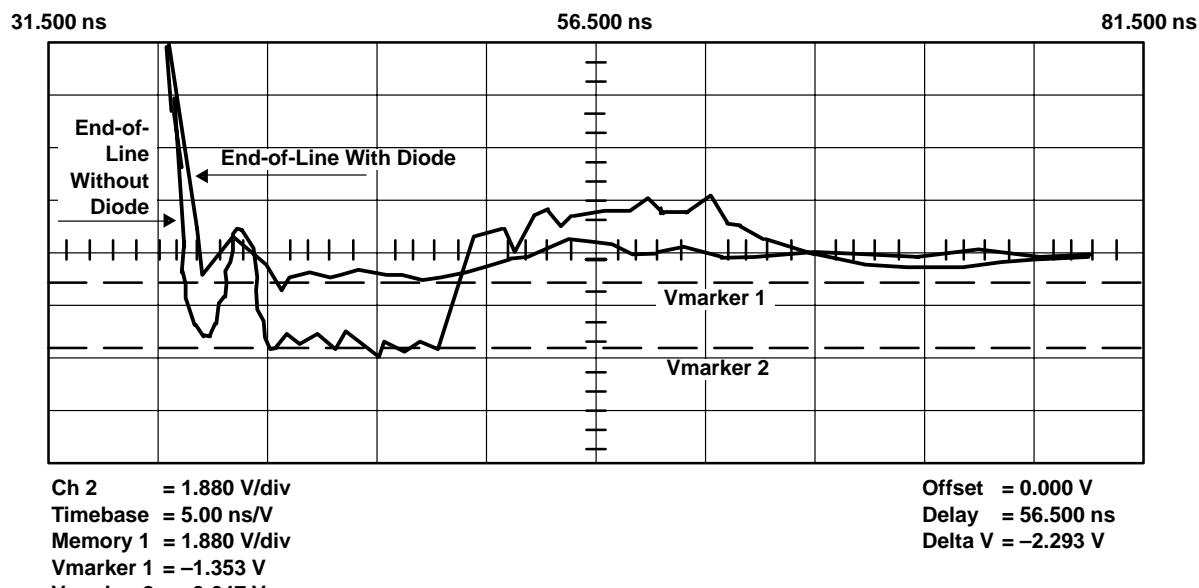


Figure 6. Reduction of Negative Transients at the End of a Transmission Line

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|---|
| SN74S1051D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S1051 | Samples |
| SN74S1051DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S1051 | Samples |
| SN74S1051DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S1051 | Samples |
| SN74S1051DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S1051 | Samples |
| SN74S1051DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S1051 | Samples |
| SN74S1051DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S1051 | Samples |
| SN74S1051N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S1051N | Samples |
| SN74S1051NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S1051N | Samples |
| SN74S1051NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74S1051 | Samples |
| SN74S1051NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74S1051 | Samples |
| SN74S1051NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74S1051 | Samples |
| SN74S1051PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S1051 | Samples |
| SN74S1051PWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S1051 | Samples |
| SN74S1051PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S1051 | Samples |
| SN74S1051PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S1051 | Samples |
| SN74S1051PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S1051 | Samples |
| SN74S1051PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S1051 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

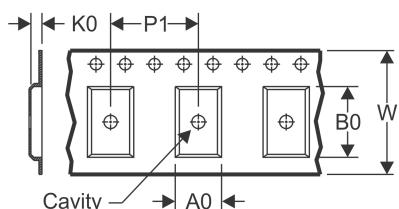
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74S1051DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74S1051NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74S1051PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

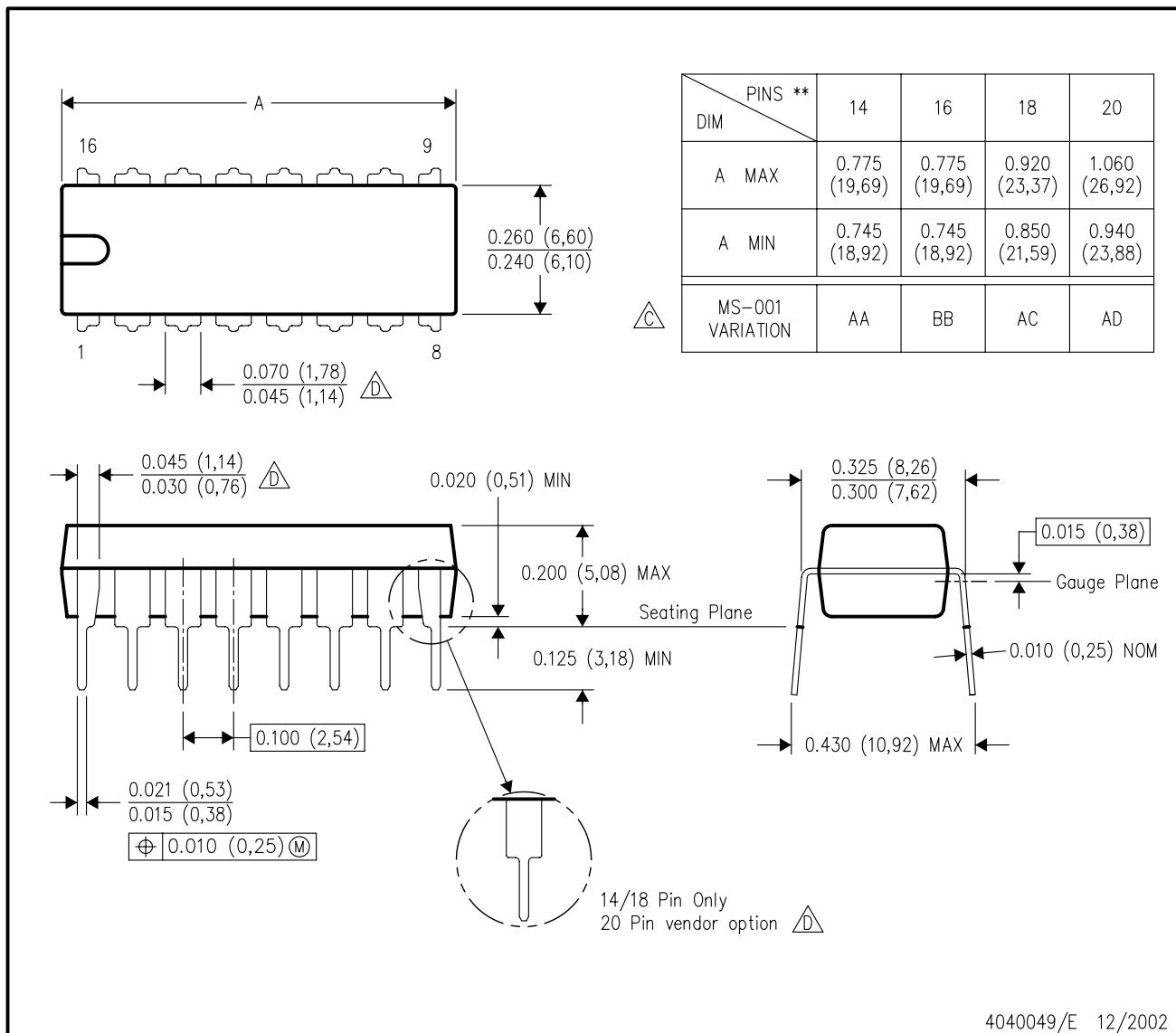

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74S1051DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74S1051NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74S1051PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

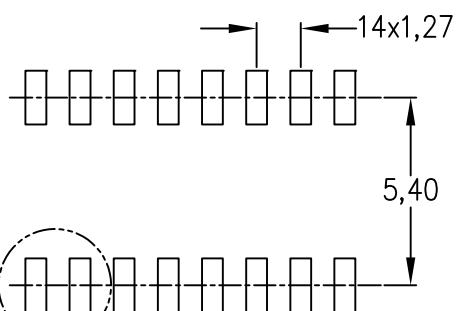
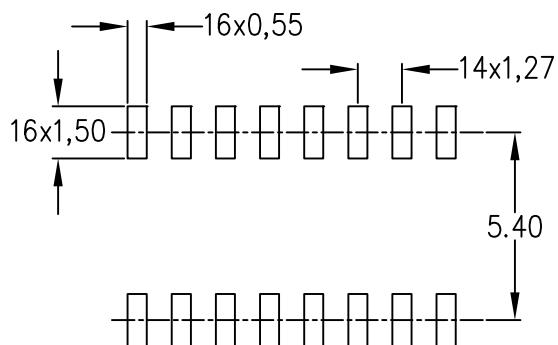
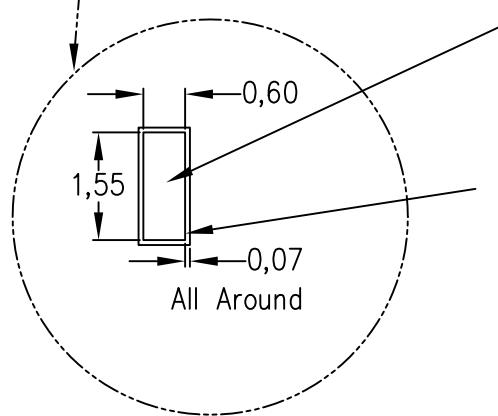
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

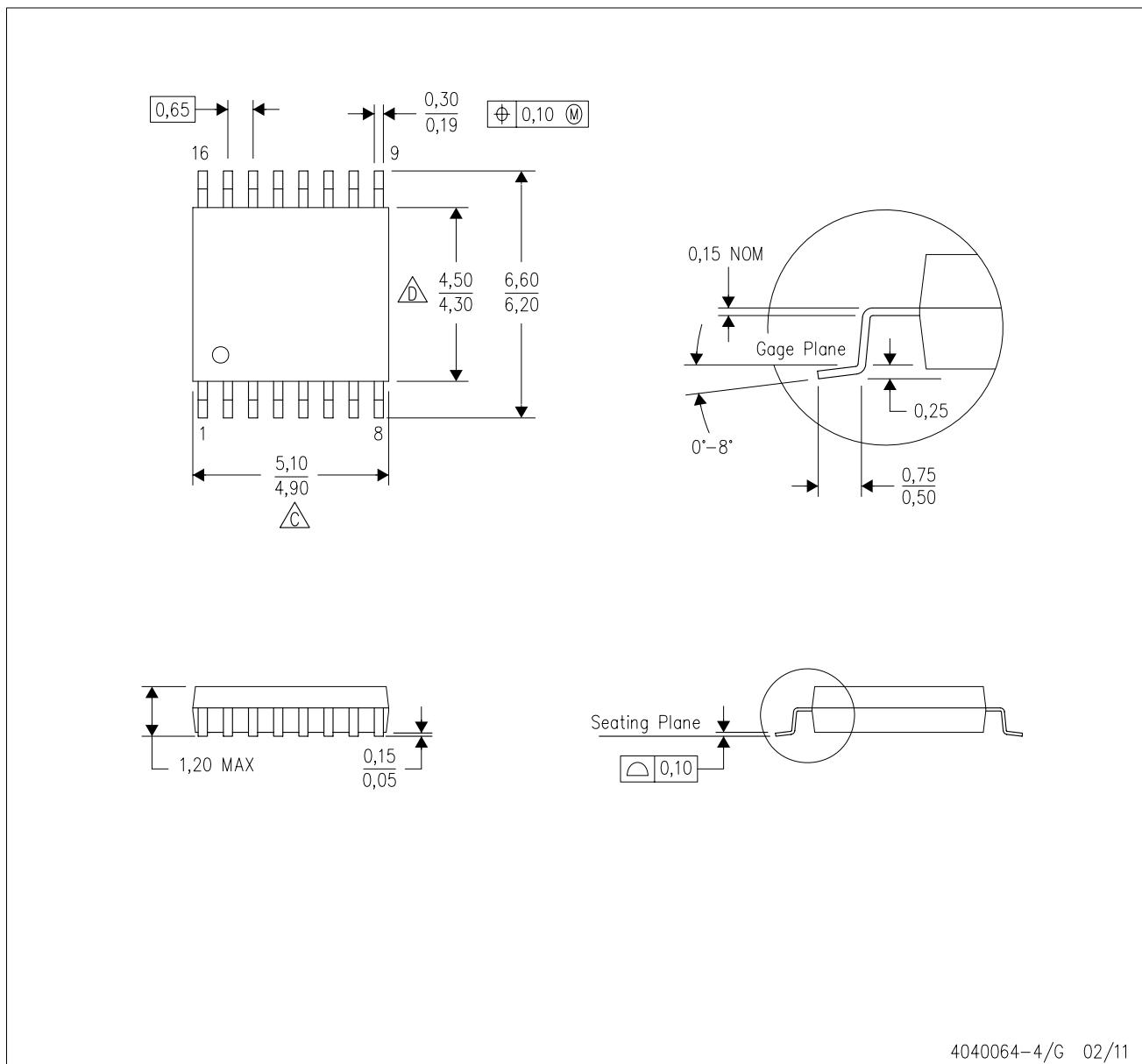
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

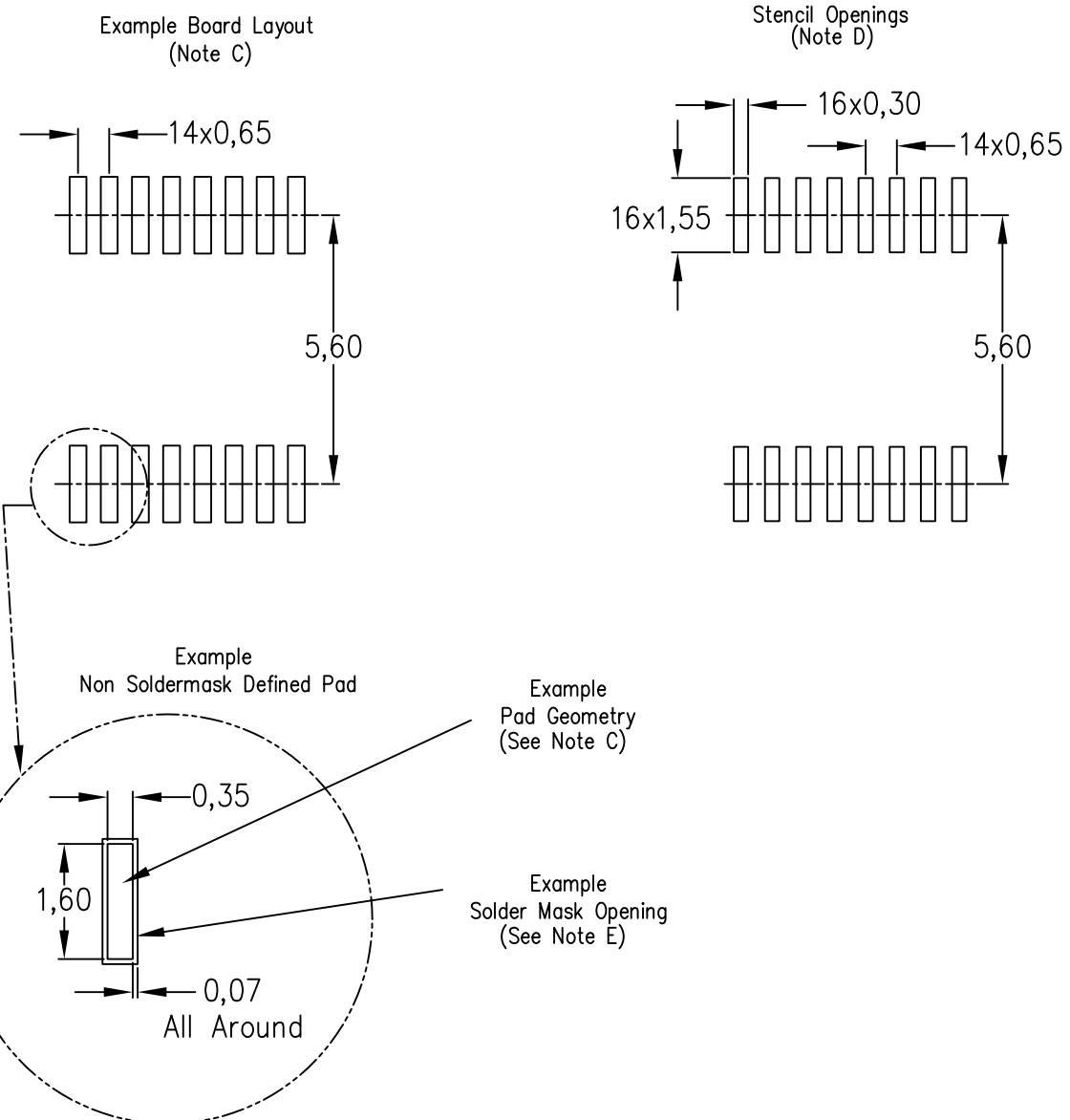
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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