

AT28C16

T-46-13-27

Features

- Fast Read Access Time - 150ns
- Fast Byte Write - 200 μ s or 1 ms
- Self-Timed Byte Write Cycle
 - Internal Address and Data Latches
 - Internal Control Timer
 - Automatic Clear Before Write
- Direct Microprocessor Control
 - DATA POLLING
- Low Power
 - 30mA Active Current
 - 100 μ A CMOS Standby Current
- High Reliability
 - Endurance: 10^4 or 10^5 cycles
 - Data Retention: 10 years
- 5V $\pm$ 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

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16K (2K x 8)
CMOS
E²PROM

Description

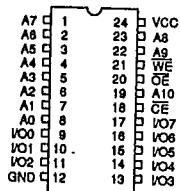
The AT28C16 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C16 is a 16k memory organized as 2,048 words x 8 bits. The device is manufactured with Atmel's reliable non-volatile CMOS technology.

The AT28C16 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by DATA polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

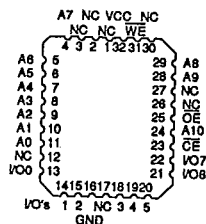
The CMOS technology offers fast access times of 150ns at low power dissipation. When the chip is deselected the standby current is less than 100 μ A.

Atmel's 28C16 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of E²PROM are available for device identification or tracking.

Pin Configurations



Pin Name	Function
A0 - A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

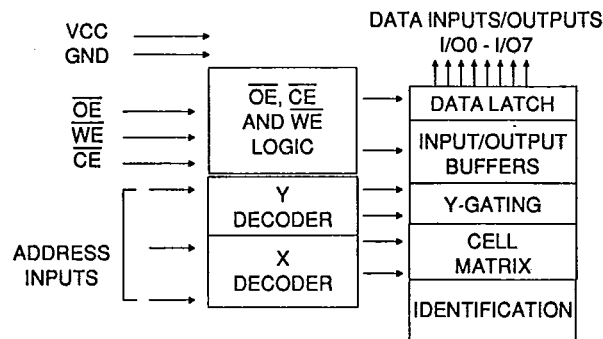


Note: PLCC package pins 1 and 17 are DON'T CONNECT.



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Block Diagram



Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V _{IL}	V _{IL}	V _{IH}	DOUT
Write ⁽²⁾	V _{IL}	V _{IH}	V _{IL}	DIN
Standby/Write Inhibit	V _{IH}	X ⁽¹⁾	X	High Z
Write Inhibit	X	X	V _{IH}	
Write Inhibit	X	V _{IL}	X	
Output Disable	X	V _{IH}	X	High Z
Chip Erase	V _{IL}	V _H ⁽³⁾	V _{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.

2. Refer to A.C. Programming Waveforms.

3. V_H = 12.0V ± 0.5V.

Device Operation

READ: The AT28C16 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C16 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

FAST BYTE WRITE: The AT28C16F offers a byte write time of 200µs maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

DATA POLLING: The AT28C16 provides **DATA POLLING** to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the

complement of that data for I/O₇ (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) V_{cc} sense— if V_{cc} is below 3.8V (typical) the write function is inhibited. (b) V_{cc} power on delay— once V_{cc} has reached 3.8V the device will automatically time out 5ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C16 may be set to the high state by the **CHIP CLEAR** operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of E²PROM memory are available to the user for device identification. By raising A₉ to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

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Absolute Maximum Ratings*

Temperature Under Bias.....-55°C to +125°C

Storage Temperature.....-65°C to +150°C

All Input Voltages

(including N.C. Pins)

with Respect to Ground -0.6V to +6.25V

All Output Voltages

with Respect to Ground -0.6V to V_{CC} +0.6VVoltage on $\overline{OE}$ and A9

with Respect to Ground -0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. and A.C. Operating Range

		AT28C16-15	AT28C16-20	AT28C16-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V _{CC} Power Supply		5V±10%	5V±10%	5V±10%

D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} =0V to V _{CC} + 1V		10	μA
I _{LO}	Output Leakage Current	V _{I/O} =0V to V _{CC}		10	μA
I _{SB1}	V _{CC} Standby Current CMOS	$\overline{CE}$ =V _{CC} -0.3V to V _{CC} + 1.0V		100	μA
I _{SB2}	V _{CC} Standby Current TTL	$\overline{CE}$ =2.0V to V _{CC} + 1.0V	Com.	2	mA
			Ind., Mil.	3	mA
I _{CC}	V _{CC} Active Current A.C.	f=5MHz; I _{OUT} =0mA $\overline{CE}$ =V _{IL}	Com.	30	mA
			Ind., Mil.	45	mA
V _{IL}	Input Low Voltage			0.8	V
V _{IH}	Input High Voltage		2.0		V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA		.4	V
V _{OH}	Output High Voltage	I _{OH} =-400μA	2.4		V

Pin Capacitance (f=1MHz T=25°C) ⁽⁴⁾

	Typ	Max	Units	Conditions
C _{IN}	4	6	pF	V _{IN} = 0V
C _{OUT}	8	12	pF	V _{OUT} = 0V



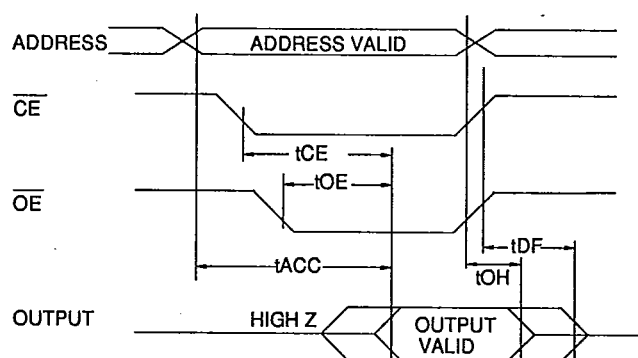


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A.C. Read Characteristics

Symbol	Parameter	AT28C16-15		AT28C16-20		AT28C16-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
$t_{CE}^{(1)}$	$\overline{CE}$ to Output Delay		150		200		250	ns
$t_{OE}^{(2)}$	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
$t_{DF}^{(3,4)}$	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

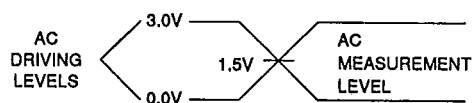
A.C. Read Waveforms



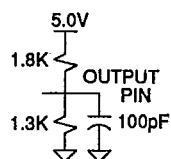
Notes:

- $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
- $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
- t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first ($C_L = 5pF$).
- This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level

 $t_R, t_F < 20ns$

Output Test Load

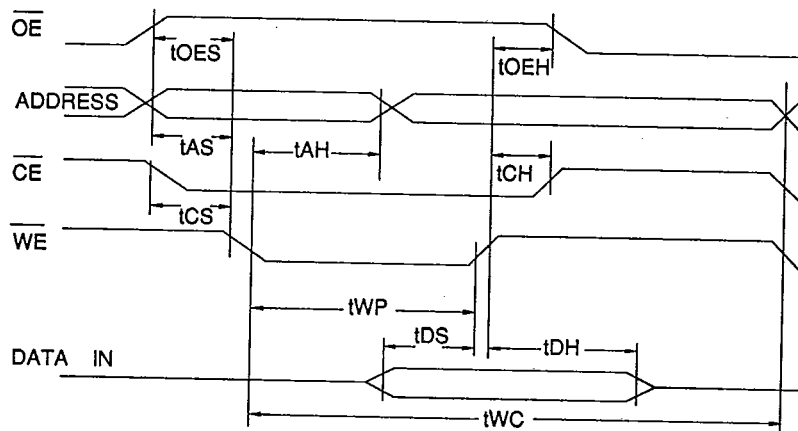
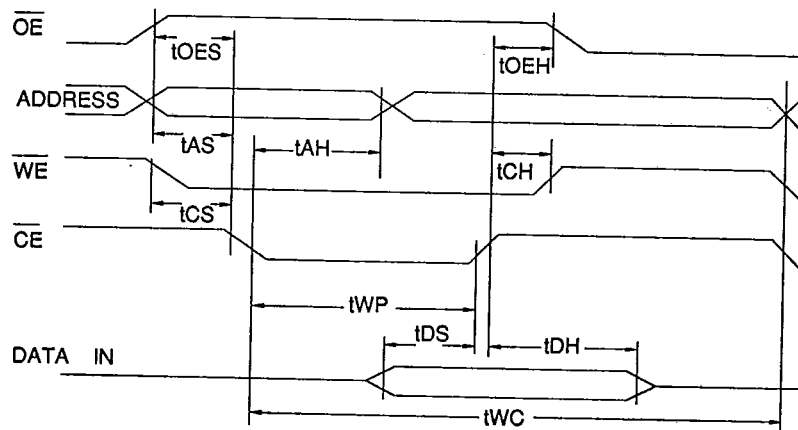


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A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10			ns
t_{WC}	Write Cycle Time	AT28C16	0.5	1.0	ms
		AT28C16E/F	100	200	μ s

A.C. Write Waveforms- $\overline{WE}$ Controlled**A.C. Write Waveforms- $\overline{CE}$ Controlled**



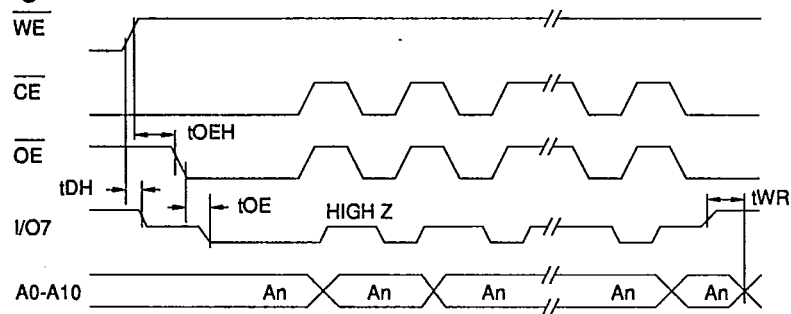
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Data Polling Characteristics⁽¹⁾

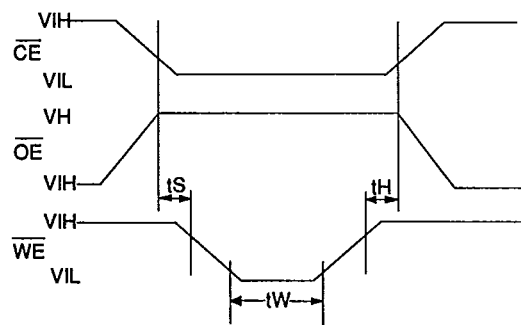
Symbol	Parameter	Min	Typ	Max	Units
t _{DH}	Data Hold Time	10			ns
t _{OE}	$\overline{\text{OE}}$ Hold Time	10			ns
t _{OE}	$\overline{\text{OE}}$ to Output Delay			100	ns
t _{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Data Polling Waveforms



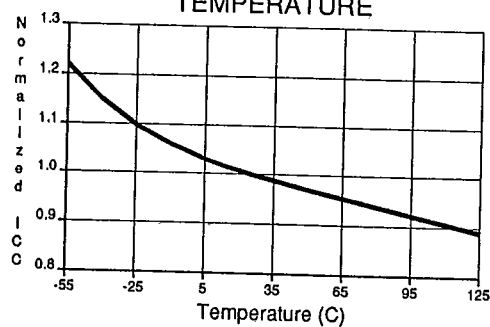
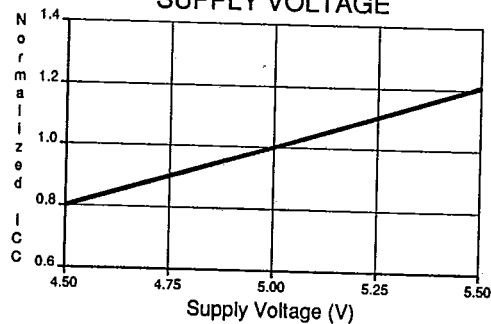
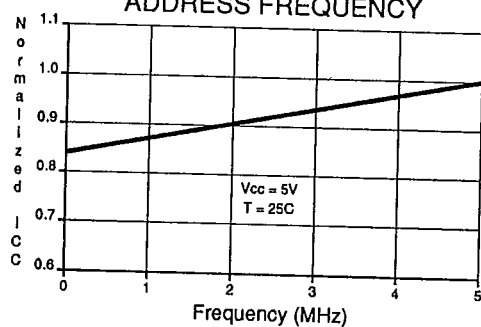
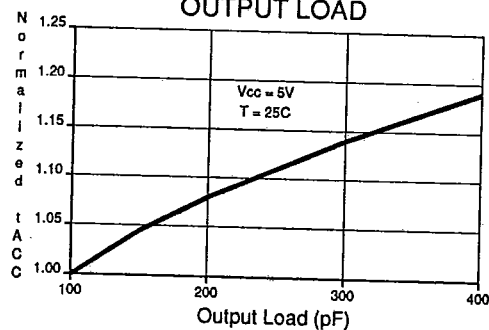
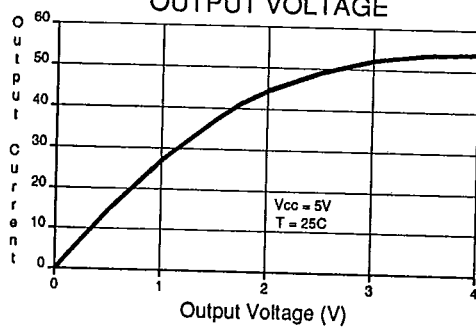
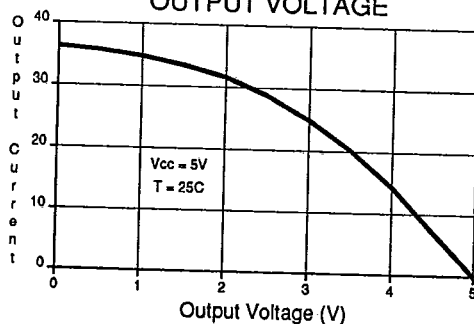
Chip Erase Waveforms



t_S = t_H = 1μsec (min.)
t_W = 10msec (min.)
V_H = 12.0V ± 0.5V

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NORMALIZED SUPPLY CURRENT vs.
TEMPERATURENORMALIZED SUPPLY CURRENT vs.
SUPPLY VOLTAGENORMALIZED SUPPLY CURRENT vs.
ADDRESS FREQUENCYNORMALIZED ACCESS TIME vs.
OUTPUT LOADOUTPUT SINK CURRENT vs.
OUTPUT VOLTAGEOUTPUT SOURCE CURRENT vs.
OUTPUT VOLTAGE**ATMEL**



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Ordering Information

tACC (ns)	Icc (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C16(E,F)-15DC	24D6	Commercial (0°C to 70°C)
			AT28C16(E,F)-15JC	32J	
			AT28C16(E,F)-15LC	32L	
			AT28C16(E,F)-15PC	24P6	
			AT28C16(E,F)-15SC	24S	
150	45	0.1	AT28C16(E,F)-15DI	24D6	Industrial (-40°C to 85°C)
			AT28C16(E,F)-15JI	32J	
			AT28C16(E,F)-15LI	32L	
			AT28C16(E,F)-15PI	24P6	
			AT28C16(E,F)-15SI	24S	
			AT28C16(E,F)-15DM	24D6	Military (-55°C to 125°C)
			AT28C16(E,F)-15LM	32L	
			AT28C16(E,F)-15DM/883	24D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT28C16(E,F)-15LM/883	32L	
200	30	0.1	AT28C16(E,F)-20DC	24D6	Commercial (0°C to 70°C)
			AT28C16(E,F)-20JC	32J	
			AT28C16(E,F)-20LC	32L	
			AT28C16(E,F)-20PC	24P6	
			AT28C16(E,F)-20SC	24S	
200	45	0.1	AT28C16(E,F)-20DI	24D6	Industrial (-40°C to 85°C)
			AT28C16(E,F)-20JI	32J	
			AT28C16(E,F)-20LI	32L	
			AT28C16(E,F)-20PI	24P6	
			AT28C16(E,F)-20SI	24S	
			AT28C16(E,F)-20DM	24D6	Military (-55°C to 125°C)
			AT28C16(E,F)-20LM	32L	
			AT28C16(E,F)-20DM/883	24D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT28C16(E,F)-20LM/883	32L	
250	30	0.1	AT28C16(E,F)-25DC	24D6	Commercial (0°C to 70°C)
			AT28C16(E,F)-25JC	32J	
			AT28C16(E,F)-25LC	32L	
			AT28C16(E,F)-25PC	24P6	
			AT28C16(E,F)-25SC	24S	
			AT28C16-W	DIE	
250	45	0.1	AT28C16(E,F)-25DI	24D6	Industrial (-40°C to 85°C)
			AT28C16(E,F)-25JI	32J	
			AT28C16(E,F)-25LI	32L	
			AT28C16(E,F)-25PI	24P6	
			AT28C16(E,F)-25SI	24S	
			AT28C16(E,F)-25DM	24D6	Military (-55°C to 125°C)
			AT28C16(E,F)-25LM	32L	
			AT28C16(E,F)-25DM/883	24D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT28C16(E,F)-25LM/883	32L	

AT28C16**Ordering Information**

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t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
300	45	0.1	AT28C16(E,F)-30DM/883 AT28C16(E,F)-30LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	AT28C16(E,F)-35DM/883 AT28C16(E,F)-35LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
450	45	0.1	AT28C16(E,F)-45DM/883 AT28C16(E,F)-45LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

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Package Type

24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die

Options

Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 μs
F	Fast Write Option: Write Time = 200 μs

ATMEL