National Semiconductor Corporation

DM54ALS242B/DM74ALS242B/ DM54ALS243A/DM74ALS243A Quad TRI-STATE® Bidirectional Bus Drivers

General Description

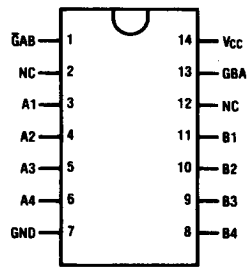
These octal TRI-STATE® bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems. The ALS242B has inverting buffers, while the ALS243A has non-inverting buffers. The direction enable gating is configured with separate control over either buffer direction and the two control buffers are complementary. Connecting these control inputs to one common line implements single line direction control, while individual control can put both buffer directions into TRI-STATE simultaneously (disabled state) or put both buffer directions into the active state (data latch state). The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

Features

- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Functional and pin compatible with the DM54/74LS counterpart
- Improved switching performance with less power dissipation compared with the DM54/74LS counterpart
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low level drive current: 54ALS = 12 mA, 74ALS = 24 mA

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DM54ALS242BJ, DM54ALS243AJ, DM74ALS242BM, DM74ALS242BN, DM74ALS243AM, DM74ALS243AN
See NS Package Number J14A, M14A or N14A

Function Table

Inputs		'ALS242B	'ALS243A
$\overline{G}AB$	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	
Dedicated Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0 to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS242B, 243A			DM74ALS242B, 243A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature (unless otherwise specified)

Symbol	Parameter	Conditions		DM54ALS242B, 243A			DM74ALS242B, 243A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High Level Output	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			2.4			V
			I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 54ALS (Max)			0.25	0.4		0.25	0.4	V
		I_{OL} = 74ALS (Max)			—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V (5.5V for I/O Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V (Note 1)				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V (Note 1)				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS242B Active Outputs High			10	20		10	16	mA
		Active Outputs Low			14	26		14	21	mA
		Outputs TRI-STATE			12	24		12	19	mA
		V_{CC} = 5.5V, ALS243A Active Outputs High			15	30		15	25	mA
		Active Outputs Low			20	35		20	30	mA
		Outputs TRI-STATE			21	37		21	32	mA

Note 1: For the I/O ports, the parameters I_{IH} and I_{IL} include the TRI-STATE output currents (I_{OZH} and I_{OZL}).

'ALS242B Switching Characteristics over recommended operating free-air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	54ALS242B		74ALS242B		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	A or B	B or A	2	15	2	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	14	2	10	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$AB	B	4	22	4	18	ns
t_{PZL}	Output Enable Time to Low Level Output				7	25	7	21	ns
t_{PHZ}	Output Disable Time to High Level Output		$\overline{G}$AB	B	2	16	2	14	ns
t_{PLZ}	Output Disable Time to Low Level Output				2	18	2	12	ns
t_{PZH}	Output Enable Time to High Level Output		GBA	A	4	22	4	18	ns
t_{PZL}	Output Enable Time to Low Level Output				7	25	7	21	ns
t_{PHZ}	Output Disable Time from High Level Output		GBA	A	2	16	2	14	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	18	2	12	ns

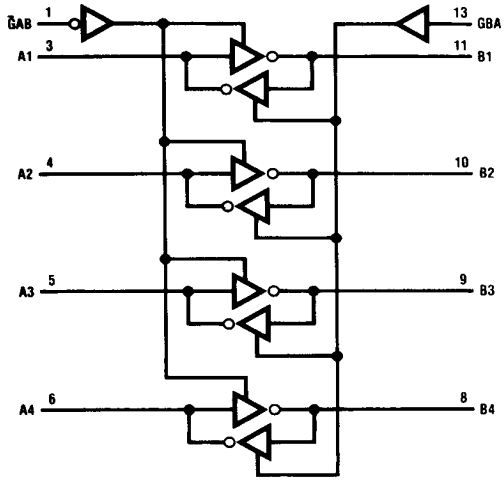
'ALS243A Switching Characteristics over recommended operating free-air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	54ALS243A		74ALS243A		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	A or B	B or A	4	15	4	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				4	15	4	11	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$AB	B	7	25	7	20	ns
t_{PZL}	Output Enable Time to Low Level Output				7	25	7	20	ns
t_{PHZ}	Output Disable Time to High Level Output		$\overline{G}$AB	B	2	16	2	14	ns
t_{PLZ}	Output Disable Time to Low Level Output				3	27	3	22	ns
t_{PZH}	Output Enable Time to High Level Output		GBA	A	7	25	7	20	ns
t_{PZL}	Output Enable Time to Low Level Output				7	25	7	20	ns
t_{PHZ}	Output Disable Time from High Level Output		GBA	A	2	16	2	14	ns
t_{PLZ}	Output Disable Time from Low Level Output				3	27	3	22	ns

Note 1: See Section 1 for test waveforms and output loads.

Logic Diagrams

DM54/74ALS242B



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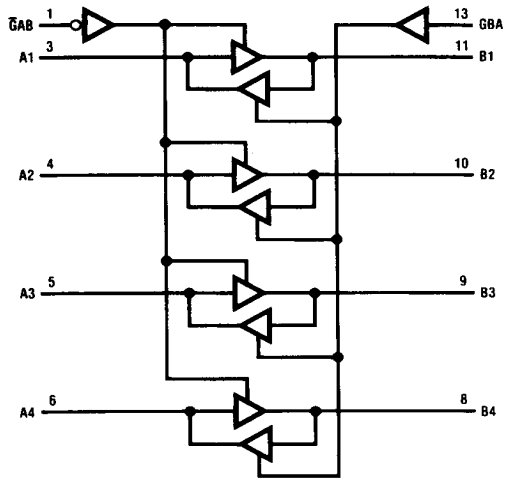
DM54/74ALS243A



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