18-Channel Gamma Buffer with Regulator

ADD8708

FEATURES

18 precision gamma reference outputs
Mask-programmable gamma resistors:
0.2% resolution and 0.1% accuracy
Mask-programmable voltage regulator: 0.4% accuracy
Upper 9 buffers swing to V_{DD}
Lower 9 buffers swing to GND
Single-supply operation: 7.5 V to 16.5 V
Gamma current drive: 15 mA per channel
Peak output current: 150 mA
Output voltage stable under load conditions
Pin-to-pin compatible with ADD8709
48-lead, Pb-free LQFP and LFCSP

APPLICATIONS

LCD TV panels
LCD monitor panels

GENERAL DESCRIPTION

The ADD8708 is an 18-channel integrated gamma reference for use in high resolution LCD TV and monitors panels. The output buffers feature high current drive and low offset voltage to provide an accurate and stable gamma curve. The top nine channels swing to V_{DD}; the lower nine channels swing to GND.

Integrating the gamma setup resistors drastically reduces the external component count while increasing the gamma curve accuracy. To accommodate multiple column drivers and panel architectures, the ADD8708 is mask programmable to a 0.2% resolution using the on-chip 500 resistor string. An on-board voltage regulator provides a fixed input for the resistor string, isolating the gamma curve from the supply ripple.

The ADD8708 is specified over the temperature range of –40°C to +105°C and comes in both a 48-lead, Pb-free, lead-frame chip-scale package and a Pb-free, low-profile, quad flat package.

FUNCTIONAL BLOCK DIAGRAM

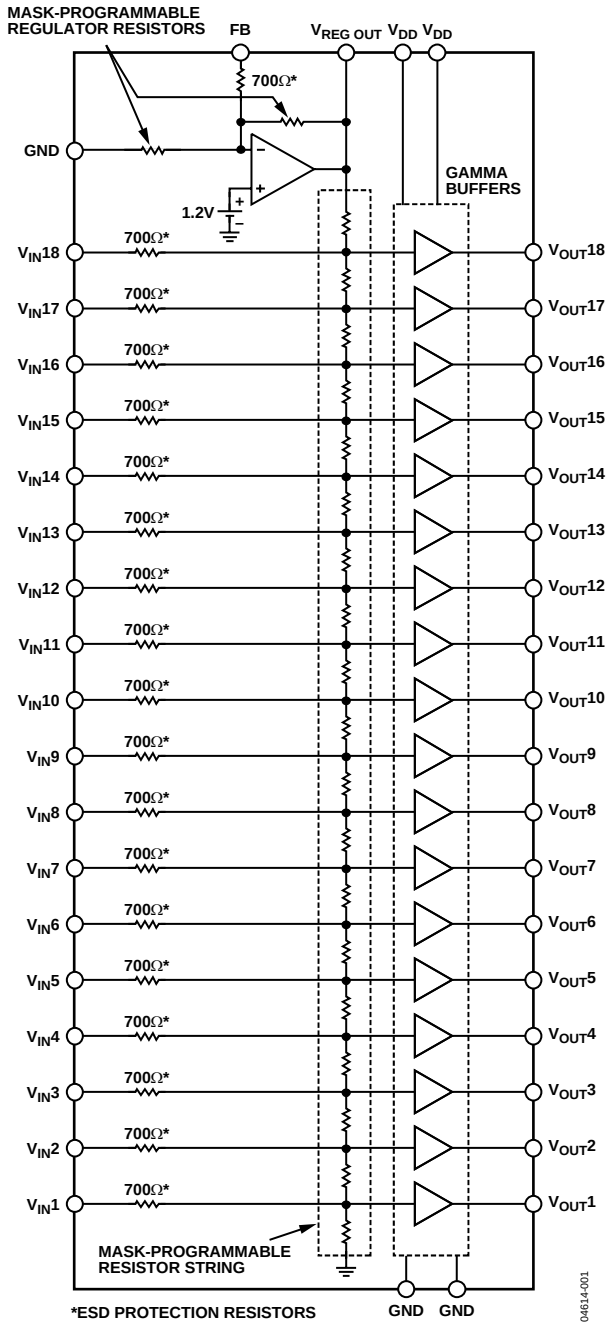

Figure 1. 48-Lead LQFP or LFCSP

Rev. 0

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REVISION HISTORY

10/04—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

V_{DD} = 16 V, T_A @ 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GAMMA CURVE CHARACTERISTICS						
Accuracy	R_{ACC}[1]			0.1	0.4	%
Programming Resolution	R_{RES}	500 segments		0.2		%
Total Resistor String	R_{TOTAL}			15		kΩ
BUFFER CHARACTERISTICS						
OUTPUTS						
Output Voltage Range (Ch18 to Ch10)	V_{OUT}	I_L = 100 µA	1.4		V_{DD}	V
Output Voltage Range (Ch9 to Ch1)	V_{OUT}	I_L = 100 µA	0		V_{DD} – 1.4	V
Output vs. Load (Ch18, Ch17, Ch2, Ch1)	ΔV_{OUT}[2]	I_L = 20 mA		15		mV
Output vs. Load (Ch16 to Ch3)	ΔV_{OUT}[2]	I_L = 5 mA		5		mV
INPUTS						
Offset Voltage	V_{OS}			5	15	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +105°C		20		µV/°C
Input Bias Current	I_B	−40°C ≤ T_A ≤ +105°C		0.5	1.5	µA
Input Voltage Range (Ch18 to Ch10)	V_{IN}		1.4		V_{DD}	V
Input Voltage Range (Ch9 to Ch1)	V_{IN}		0		V_{DD} – 1.4	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 200 pF	4	6		V/µs
Bandwidth	BW	–3 dB, R_L = 10 kΩ, C_L = 200 pF		4.5		MHz
Settling Time to 0.1%	t_S	1 V, R_L = 10 kΩ, C_L = 200 pF		1.1		µs
Phase Margin	Φ_o	R_L = 10 kΩ, C_L = 200 pF		55		Degrees
Power Supply Rejection Ratio	PSRR	V_{DD} = 7 V to 17 V, −40°C ≤ T_A ≤ +105°C	68	90		dB
VOLTAGE REGULATOR						
Programmable Range	$V_{REG\ OUT}$		5		V_{DD} – 0.6	V
Initial Regulator Accuracy	V_{ACC}	No load; $V_{REG\ OUT}$ = 14.4V		0.4	1.5	%
Dropout Voltage	V_{DO}	I_L = 100 µA		100	150	mV
		I_L = 5 mA		310	350	mV
Line Regulation	REG_{LINE}	V_{IN} = 8.5 V to 16.5 V, V_{OUT} = 8 V		0.01	0.20	%/V
Load Regulation	REG_{LOAD}	I_O = 100 µA to 10 mA		0.02	0.10	%/mA
Maximum Load Current	I_O	−40°C ≤ T_A ≤ +105°C	5			mA
Feedback Reference Voltage	V_{REF}			1.2		V
Feedback Input Bias Current	$I_{B\ FB}$	−40°C ≤ T_A ≤ +105°C	-150	10	150	nA
SYSTEM ACCURACY						
Total Error[3, 4]	$V_{Total\ Error}$	−40°C ≤ T_A ≤ +105°C		0.5	3	%
POWER SUPPLY						
Supply Voltage	V_{DD}		7.5		16	V
Supply Current	I_{SY}	No load; −40°C ≤ T_A ≤ +105°C		9.5	16	mA

[1] Gamma curve accuracy includes resistor matching and buffer errors, but excludes the regulator error.
[2] ΔV_{OUT} is the shift from the desired output voltage under the specified current load.
[3] Total error is the difference between the designed and actual output voltage divided by the actual regulator output voltage or full-scale voltage.
[4] Total error includes regulator error, resistor string error, bias current effects, and buffer offset voltage.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V_{DD})	18 V
Input Voltage	−0.5 V to V_{DD}
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range[1]	−40°C to +105°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
ESD Tolerance (HBM)	±1500 V
ESD Tolerance (MM)	±200 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Package Characteristics

Package Type	θ_{JA}[2]	θ_{JA}[3]	Unit
LFCSP (CP)	28.3	47.7	°C/W
LQFP (ST)	N/A	74.57	°C/W

[1] See the Application Notes section.
[2] θ_{JA} for exposed pad soldered to JEDEC 4-layer board.
[3] θ_{JA} for exposed pad not soldered down.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

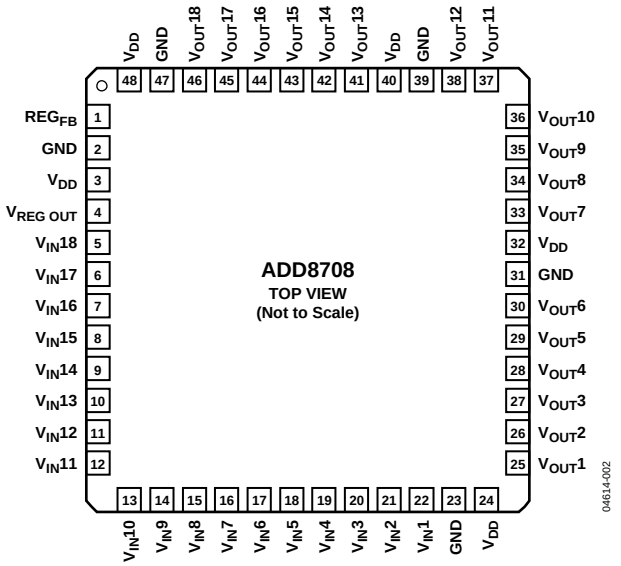

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Name	Description
1	REG_{FB}	Regulator Feedback. Compares a percentage of the regulator output to the internal 1.2 V voltage reference. Internal resistors are used to program the desired regulator output voltage.
2	GND	Ground. Normally 0 V.
3	V_{DD}	Supply Voltage. Normally 16 V.
4	$V_{REG\ OUT}$	Regulator output voltage. Provides reference voltage to resistor string and is internally connected to the top of the resistor string.
5	$V_{IN}18$	Buffer inputs. Normally floating.[1]
6	$V_{IN}17$	
7	$V_{IN}16$	
8	$V_{IN}15$	
9	$V_{IN}14$	
10	$V_{IN}13$	
11	$V_{IN}12$	
12	$V_{IN}11$	
13	$V_{IN}10$	
14	$V_{IN}9$	
15	$V_{IN}8$	
16	$V_{IN}7$	
17	$V_{IN}6$	
18	$V_{IN}5$	
19	$V_{IN}4$	
20	$V_{IN}3$	
21	$V_{IN}2$	
22	$V_{IN}1$	
23	GND	Ground. Normally 0 V.
24	V_{DD}	Supply Voltage. Normally 16 V.

[1] External resistors can be added to modify the internal resistor string to change the gamma voltage. An external resistor calculator is available upon request from your local sales office.

Pin No.	Name	Description
25	$V_{OUT}1$	Buffer Outputs. These buffers can swing to ground.
26	$V_{OUT}2$	
27	$V_{OUT}3$	
28	$V_{OUT}4$	
29	$V_{OUT}5$	
30	$V_{OUT}6$	
31	GND	Ground. Normally 0 V.
32	V_{DD}	Supply voltage. Normally 16 V.
33	$V_{OUT}7$	Buffer Output. These buffers can swing to ground.
34	$V_{OUT}8$	
35	$V_{OUT}9$	
36	$V_{OUT}10$	Buffer Output. These buffers can swing to V_{DD}.
37	$V_{OUT}11$	
38	$V_{OUT}12$	
39	GND	Ground. Normally 0 V.
40	V_{DD}	Normally 16 V.
41	$V_{OUT}13$	Buffer Outputs. These buffers can swing to V_{DD}.
42	$V_{OUT}14$	
43	$V_{OUT}15$	
44	$V_{OUT}16$	
45	$V_{OUT}17$	
46	$V_{OUT}18$	
47	GND	Ground. Normally 0 V.
48	V_{DD}	Supply voltage. Normally 16 V.

TYPICAL PERFORMANCE CHARACTERISTICS

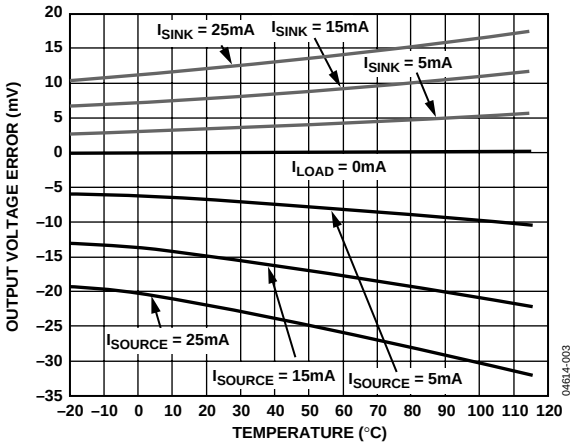

Figure 3. Output Voltage Error vs. Temperature

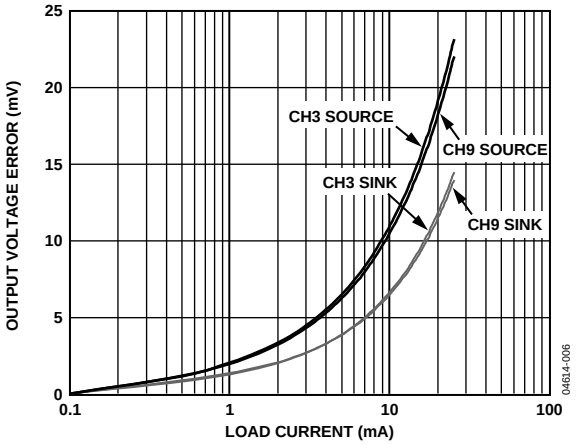

Figure 6. Output Voltage Error vs. Load Current (Channels 3 and 9)

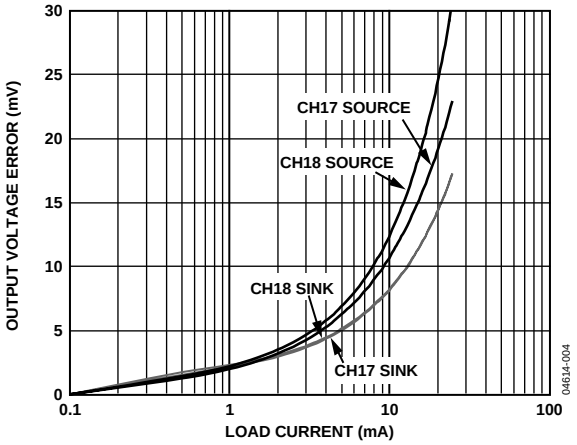

Figure 4. Output Voltage Error vs. Load Current (Channels 17 and 18)

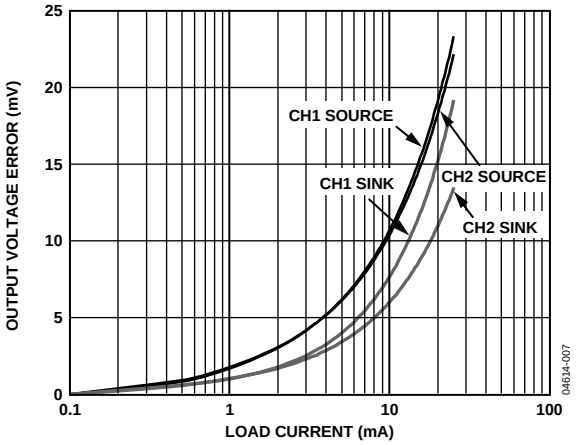

Figure 7. Output Voltage Error vs. Load Current (Channels 1 and 2)

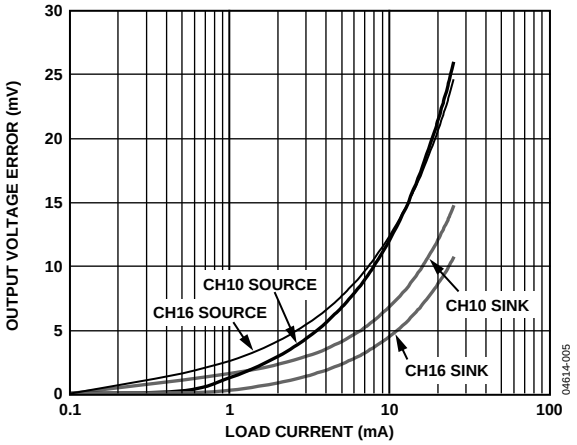

Figure 5. Output Voltage Error vs. Load Current (Channels 10 and 16)

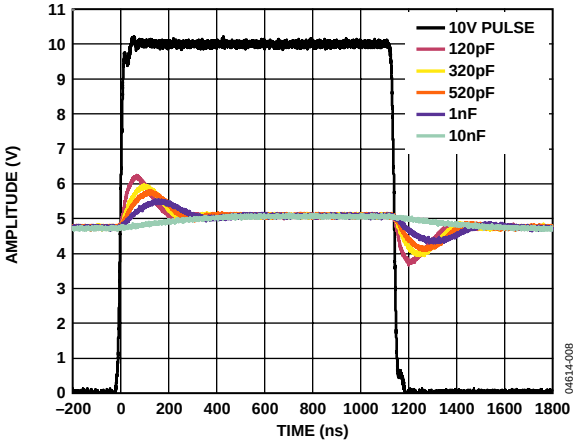

Figure 8. Gamma Buffers Transient Load Response vs. Capacitive Loading

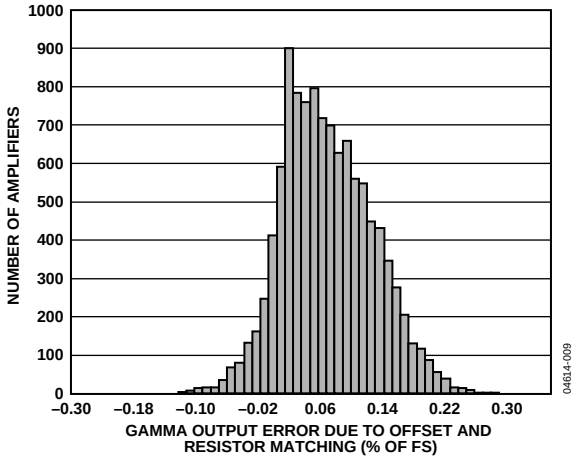

Figure 9. Gamma Output Voltage Error

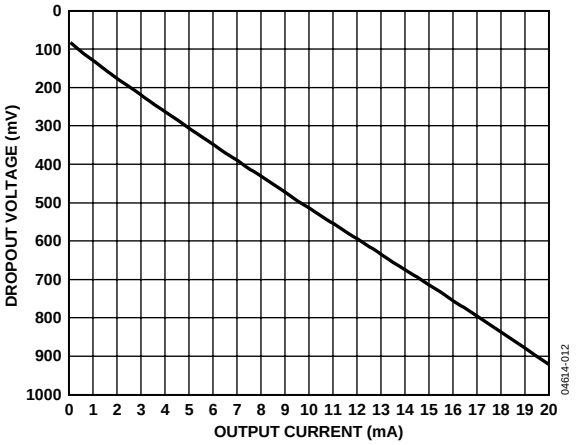

Figure 12. Dropout Voltage vs. Output Current

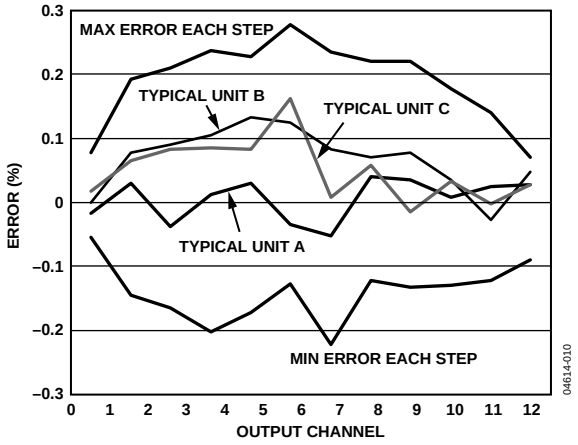

Figure 10. Gamma Output Error per Channel (920 Parts)

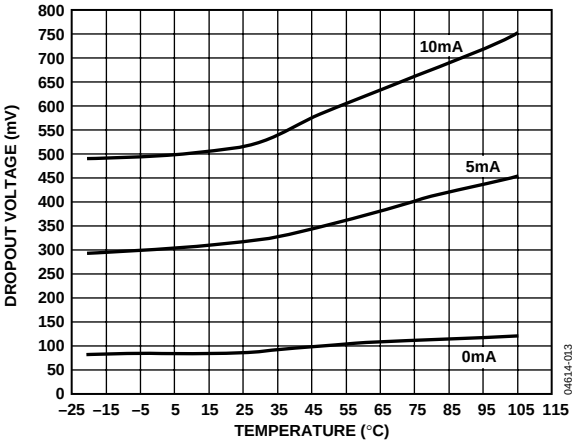

Figure 13. Dropout Voltage vs. Temperature

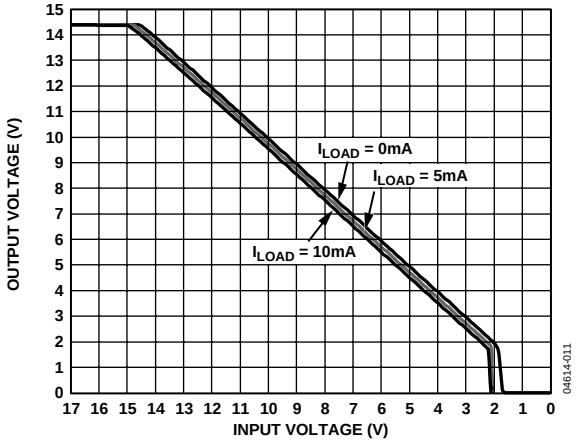

Figure 11. Dropout Characteristics

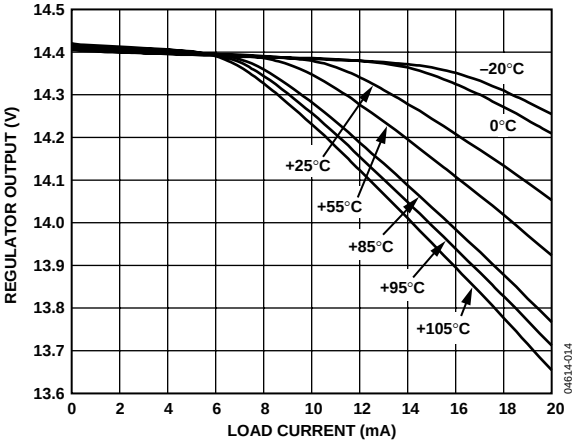

Figure 14. Regulator Output vs. I_{LOAD} over Temperature

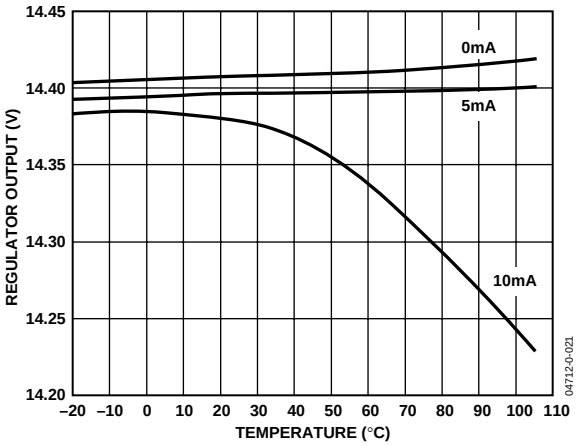

Figure 15. Regulator Output vs. Temperature

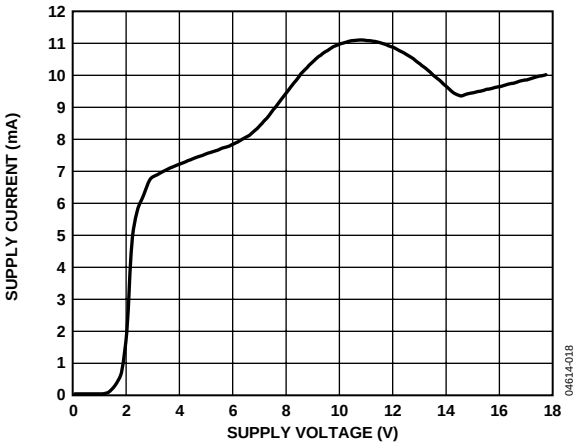

Figure 18. Supply Current vs. Supply Voltage

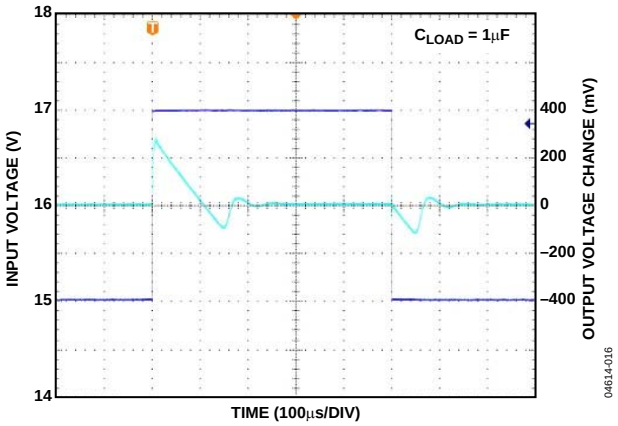

Figure 16. Regulator Line Transient Response

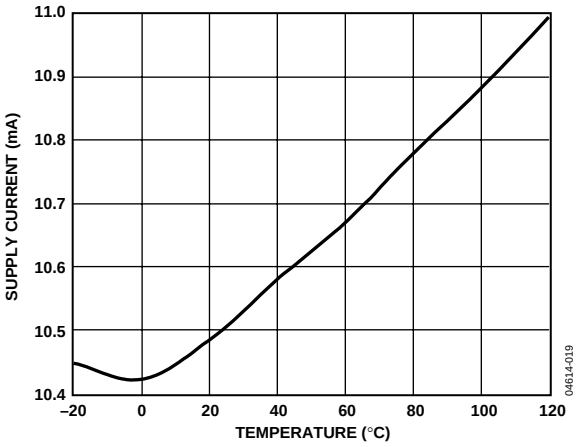

Figure 19. Supply Current vs. Temperature

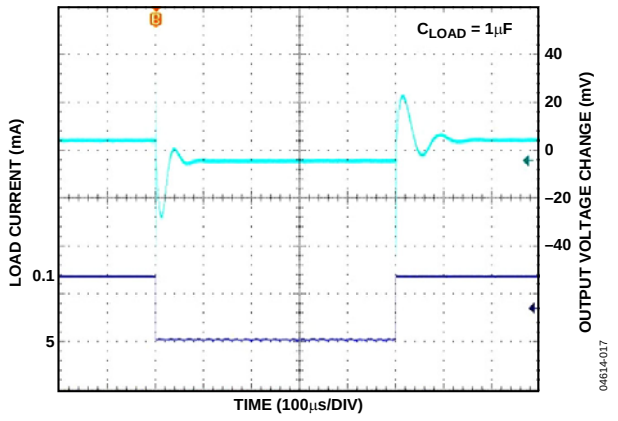

Figure 17. Regulator Load Transient Response

APPLICATION NOTES

The ADD8708 is a mask-programmable gamma reference generator that allows source drivers to be optimized for the different combinations of liquid crystals, glass sizes, etc. in large LCD panels. It generates 18 gamma reference outputs that can be mask-programmed in 0.2% increments using the 500 matched internal resistors (see Figure 20), so that every point on the curve can be targeted within 0.1% of the desired value.

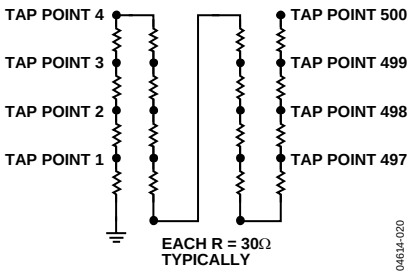

Figure 20. 500 Mask-Programmable Resistor String

In a typical panel application, the selected source drivers have an internal gamma curve that is not ideal for the specific panel (see Figure 21). The ADD8708 allows the gamma curve in the source drivers to be adjusted appropriately, and also ensures that all the source drivers have the same gamma curve.

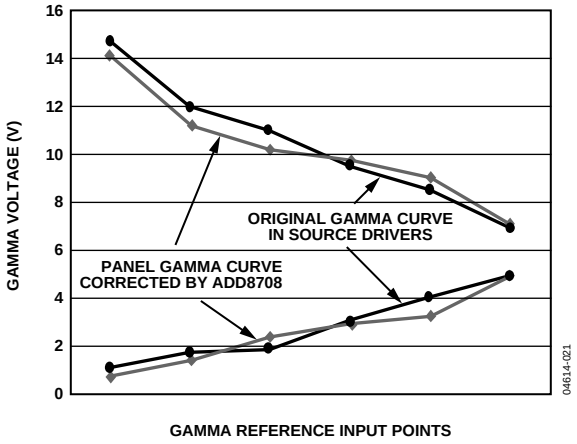

Figure 21. Original and Corrected Gamma Curves

The matching and tracking accuracy of the internal resistors is typically 0.1% with worst-case deviation from the desired curve within 0.4% of the ideal gamma curve, over temperature.

The ADD8708 also includes a low-dropout linear regulator to provide a stable reference level for the gamma curve for optimum panel performance.

TAP POINT SELECTION

The ADD8708 uses a single resistor string consisting of 500 individual elements. The tap points are mask programmable and completely independent of each other. See the Tap Point and Regulator Voltage Request Form in this data sheet.

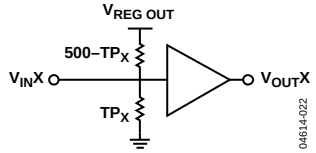

Figure 22. Gamma Buffers Tap Point Circuit

Tap point voltages can be derived from the following equation:

$$V_{OUT}X = \frac{TP_X}{500} \times V_{REG\ OUT}$$

where TP_X is the desired tap point for the Xth channel.

Table 5. Typical Mask Implementation[1]

V_{DD} = 16 V, $V_{REG\ OUT}$ = 14.4 V, 0 ≤ X ≤ 500

	Tap Point (X)	Voltage	Units
$V_{OUT}18$	500	14.400	V
$V_{OUT}17$	396	11.405	V
$V_{OUT}16$	369	10.627	V
$V_{OUT}15$	361	10.397	V
$V_{OUT}14$	354	10.195	V
$V_{OUT}13$	350	10.080	V
$V_{OUT}12$	341	9.821	V
$V_{OUT}11$	317	9.130	V
$V_{OUT}10$	299	8.611	V
$V_{OUT}9$	225	6.480	V
$V_{OUT}8$	211	6.077	V
$V_{OUT}7$	177	5.098	V
$V_{OUT}6$	167	4.810	V
$V_{OUT}5$	163	4.694	V
$V_{OUT}4$	154	4.435	V
$V_{OUT}3$	146	4.205	V
$V_{OUT}2$	118	3.398	V
$V_{OUT}1$	7	0.202	V

[1] ADD8708 release samples do not have these typical values. The values on the samples are nonmonotonic and can be provided upon request.

VOLTAGE REGULATOR

The on-board voltage regulator provides a regulated voltage to the resistor chain to provide stable gamma voltages.

The two mask-programmable internal resistors, R_1 and R_2, and a reference voltage set the output of the regulator. The typical values of these parts are shown in Figure 23. In addition, see the Tap Point and Regulator Voltage Request Form in this data sheet.

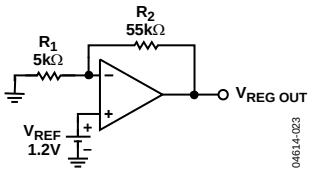

Figure 23. Voltage Regulator

The internal resistors have a typical accuracy of 0.1%. External resistors can be used to adjust the regulator voltage; however, it is not recommended. Please contact your local sales office for further details.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADD8708 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADD8708. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices, potentially causing failure.

LAND PATTERN

The LFCSP package comes with a thermal pad. Soldering down this thermal pad dramatically improves the heat dissipation of the package. It is necessary to attach vias that connect the soldered thermal pad to another layer on the board. This provides an avenue to dissipate the heat away from the part. Without vias, the heat is isolated directly under the part.

Subdivide the solder paste, or stencil layer, for the thermal pad to reduce solder balling and splatter. It is not critical how the subdivisions are arranged, as long as the total coverage of the solder paste for the thermal pad is greater than 50%. The land pattern is critical to heat dissipation. A suggested land pattern is shown in Figure 22.

The thermal pad is attached to the substrate. In the ADD8708, the substrate is connected to V_{DD}. To be electrically safe, the thermal pad should be soldered to an area on the board that is electrically isolated or connected to V_{DD}. Attaching the thermal pad to ground adversely affects the performance of the part.

OPERATING TEMPERATURE RANGE

The junction temperature is as follows:

$$T_J = T_{AMB} + \theta_{JA} \times P_{DIS}$$

where:
T_{AMB} = ambient temperature.
θ_{JA} = junction-to-ambient thermal resistance, in °C/watt.
P_{DIS} = power dissipated in the device, in watts.

For the ADD8708, P_{DIS} can be calculated by this equation:

$$P_{DIS} = V_{DD} \times I_{DQ} + \Sigma(I_{OUT\,X(+)} \times (V_{DD} - V_{OUT\,X})) + \Sigma(-I_{OUT\,X(-)} \times V_{OUT\,X}) + (V_{DD} - V_{REG\,OUT}) \times I_{LOAD}$$

where:

$V_{DD} \times I_{DQ}$ = nominal system power requirements.
$I_{OUT\,X(+)} \times (V_{DD} - V_{OUT\,X})$ = positive-current amplifier load power dissipation (current comes from V_{DD}).
$-I_{OUT\,X(-)} \times V_{OUT\,X}$ = negative-current amplifier load power dissipation (current goes to GND).
$(V_{DD} - V_{REG\,OUT}) \times I_{LOAD}$ = regulator load power dissipation.

In this example, T_{AMB} = 95°C. To calculate P_{DIS}, assume the values in Table 6.

Table 6.

	$V_{OUT\,X}$ (V)	$I_{OUT\,X}$ (mA)	P (W)
$V_{OUT}18$	14.400	4.3	0.00688
$V_{OUT}17$	11.405	5.2	0.0239
$V_{OUT}16$	10.627	−4.4	0.0468
$V_{OUT}15$	10.397	7.3	0.0409
$V_{OUT}14$	10.195	7.6	0.0441
$V_{OUT}13$	10.080	−3.9	0.0393
$V_{OUT}12$	9.821	8.3	0.0513
$V_{OUT}11$	9.130	7.9	0.0543
$V_{OUT}10$	8.611	−4.5	0.0389
$V_{OUT}9$	6.480	−4.2	0.0272
$V_{OUT}8$	6.077	5.6	0.0556
$V_{OUT}7$	5.098	−3.3	0.0168
$V_{OUT}6$	4.810	−6.9	0.0332
$V_{OUT}5$	4.694	5.7	0.0644
$V_{OUT}4$	4.435	3.5	0.0405
$V_{OUT}3$	4.205	9.6	0.113
$V_{OUT}2$	3.398	−9.5	0.0323
$V_{OUT}1$	0.202	−7.2	0.00145
$\Sigma(I_{OUT\,X(+)} \times (V_{DD} - V_{OUT\,X})) + \Sigma(-I_{OUT\,X(-)} \times V_{OUT\,X})$			0.731

$V_{DD} \times I_{DQ}$ = 16 V × 15 mA = 0.240 W
$(V_{DD} - V_{REG\,OUT}) \times I_{LOAD}$ = (16 V − 14.4 V) × 5 mA = 0.008 W
P_{DIS} = 0.240 W + 0.731 W + 0.008 W =0.979 W

Example 1

Exposed pad soldered down with via θ_{JA} = 28.3°C/W:

T_J = 95°C + (28.3°C/W) × (0.979 W) = 122.7°C

where 150°C is the maximum junction temperature that is guaranteed before the part breaks down. The maximum process limit is 125°C. Because T_J is < 150°C and < 125°C, this example demonstrates a condition where the part should perform within process limits.

Example 2

Exposed pad not soldered down θ_{JA} = 47.7°C/W:

T_J = 95°C + (47.7°C/W) × (0.979 W) = 141.7°C

In this example, T_J is < 150°C but > 125°C. Although the part should not exhibit any damage in this situation, the process limits have been exceeded. The part may no longer operate as intended.

These examples show that soldering down the exposed pad is important for proper heat dissipation. Under the same power-up and loading conditions, the unsoldered part has a higher temperature than the soldered part. Therefore, it is strongly advised that the exposed pad be soldered to V_{DD} to maintain part integrity.

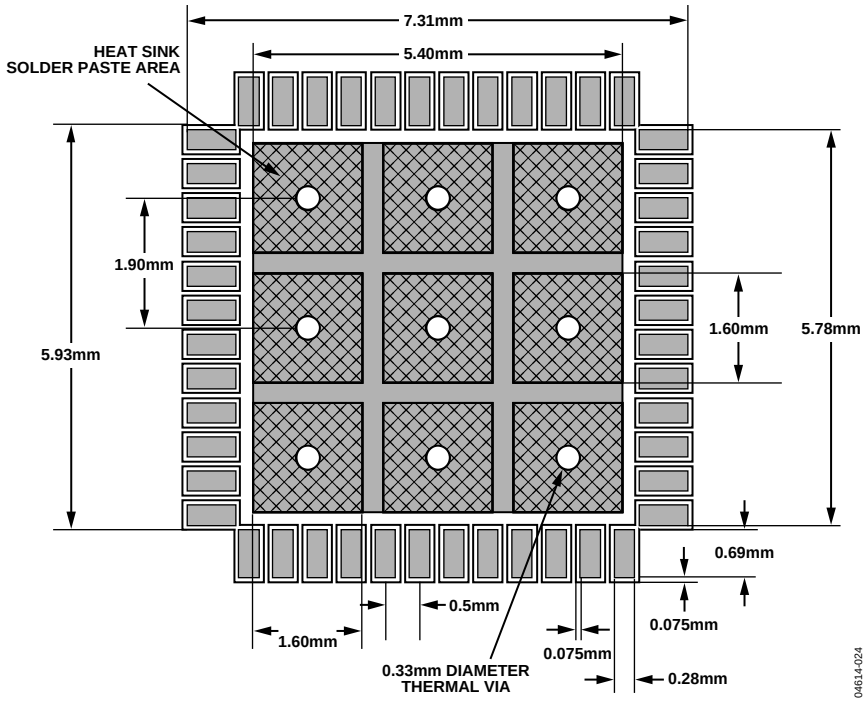

Figure 24. 48-Pin LFCSP (CP-48) Land Pattern—Dimensions Shown in Millimeters

Notes:

1. Areas in black represent the board metallization.
2. Areas in white represent the solder mask and vias.
3. Hatched area is for the heat sink solder paste.
4. The thermal pad is electrically active. The solder mask opening should be 0.150 mm larger than the pad size, resulting in 0.075 mm of clearance between the copper pad and solder mask.

TYPICAL APPLICATIONS CIRCUIT

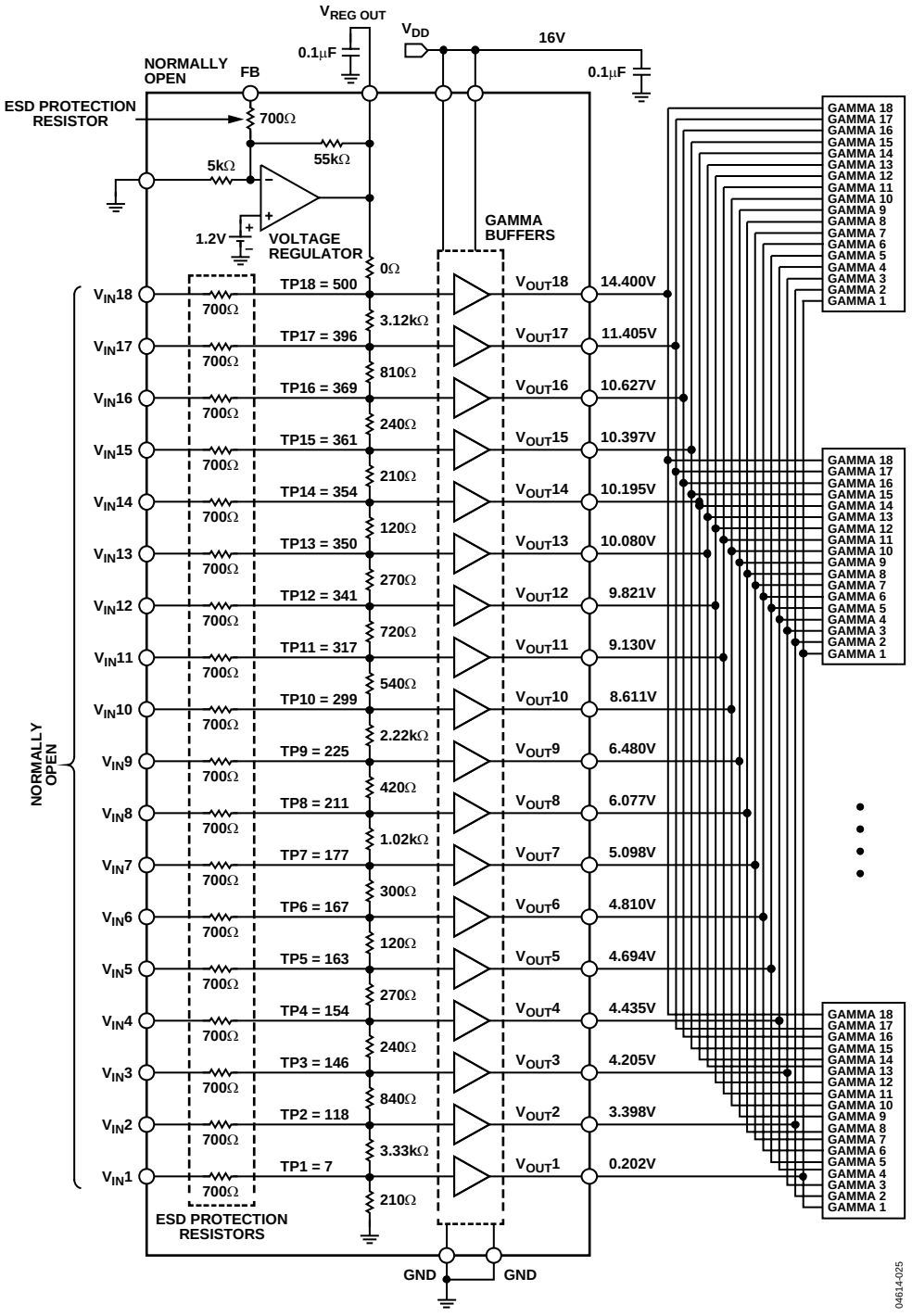

Figure 25. Typical Application Circuit

TAP POINT AND REGULATOR VOLTAGE REQUEST FORM

REGULATOR SECTION—$V_{REG\ OUT}$

To ensure correct regulator operation V_{DD} must exceed V_{REG} by 600 mV minimum—that is, a V_{REG} = 14.4 V requires a minimum V_{DD} = 15.0 V.

Parameter	Value (6.9 V – 15.4 V)
$V_{REG\ OUT}$	

TAP POINT SECTION

Gamma output voltages are calculated using the following formula:

$$V_{OUT} = \frac{TP \times V_{REG\ OUT}}{500}$$

A Microsoft® Excel spreadsheet is available which automatically calculates the best tap point based on $V_{REG\ OUT}$ and the desired output voltages for each gamma output.

Output	Tap Point
$V_{OUT}18$	
$V_{OUT}17$	
$V_{OUT}16$	
$V_{OUT}15$	
$V_{OUT}14$	
$V_{OUT}13$	
$V_{OUT}12$	
$V_{OUT}11$	
$V_{OUT}10$	
$V_{OUT}9$	
$V_{OUT}8$	
$V_{OUT}7$	
$V_{OUT}6$	
$V_{OUT}5$	
$V_{OUT}4$	
$V_{OUT}3$	
$V_{OUT}2$	
$V_{OUT}1$	

CUSTOMER INFORMATION

Name: _____

Company: _____

Address: _____

_____

Date: _____

Please return this form to your local sales office.

OUTLINE DIMENSIONS

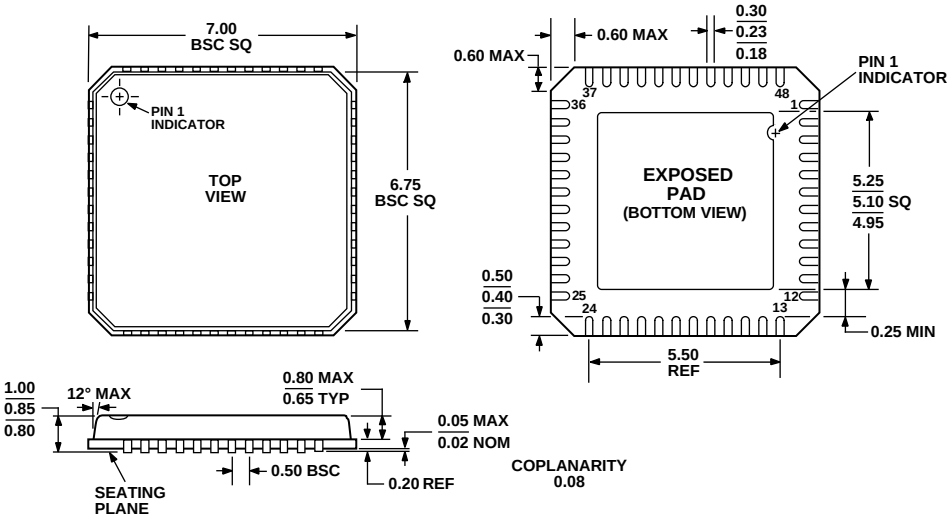

Figure 26. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body
(CP-48)
Dimensions shown in millimeters

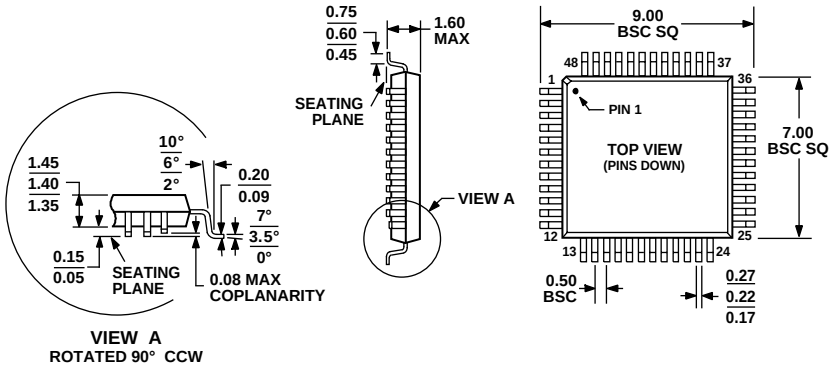

Figure 27. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADD8708WCPZ-REEL7[2]	–40°C to +105°C	48-Lead Lead Frame Chip Scale Package	CP-48
ADD8708WSTZ-REEL[2]	–40°C to +105°C	48-Lead Low Profile Quad Flat Package	ST-48

[1] Available in reels only.
[2] Z = Pb-free part.

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