

**Panasonic**

MOS FET

MTM684100LBF

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Dual P-channel MOSFET

For switching

#### ■ Features

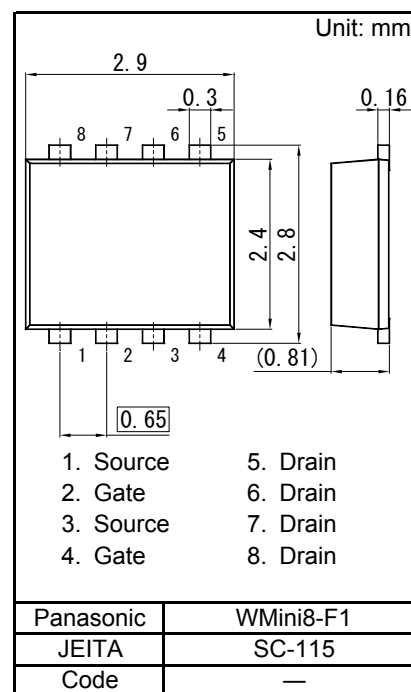
- Low drain-source On-state Resistance  
RDS(on) typ. = 32 mΩ (VGS = -4.0 V)
- Low drive voltage: 1.8V drive
- Halogen-free / RoHS compliant  
(EU RoHS / UL-94 V-0 / MSL: Level 1 compliant)

#### ■ Marking Symbol: 1C

#### ■ Basic Part Number: Dual MTM23110 (Individual)

#### ■ Packaging

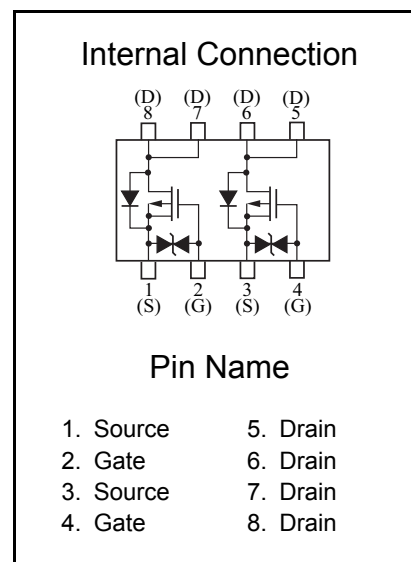
Embossed type (Thermo-compression sealing) : 3 000 pcs / reel (standard)



#### ■ Absolute Maximum Ratings Ta = 25 °C

Parameter		Symbol	Rating	Unit
FET1	Drain-source Voltage	VDS	-12	V
	Gate-source Voltage	VGS	±8	V
FET2	Drain current	ID	-4.8	A
	Peak drain current	IDp	-19	A
Overall	Total power dissipation <sup>*1</sup>	PD	1.0	W
	Channel temperature	Tch	150	°C
	Operating ambient temperature	Topr	-40 to +85	°C
	Storage temperature	Tstg	-55 to +150	°C

Note) <sup>\*1</sup> Glass epoxy board: 25.4 mm × 25.4 mm × 0.8 mm Copper foil  
of the drain portion should have a area of 300 mm<sup>2</sup> or more  
PD absolute maximum rating without a heat sink: 400 mW



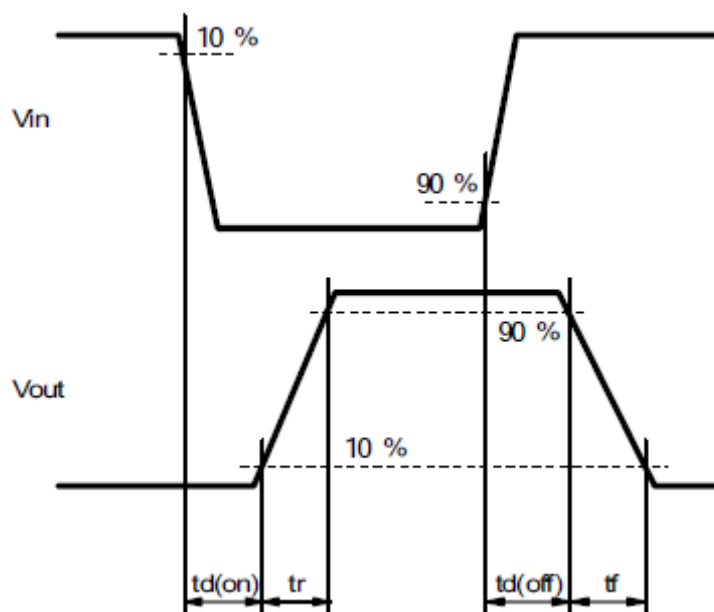
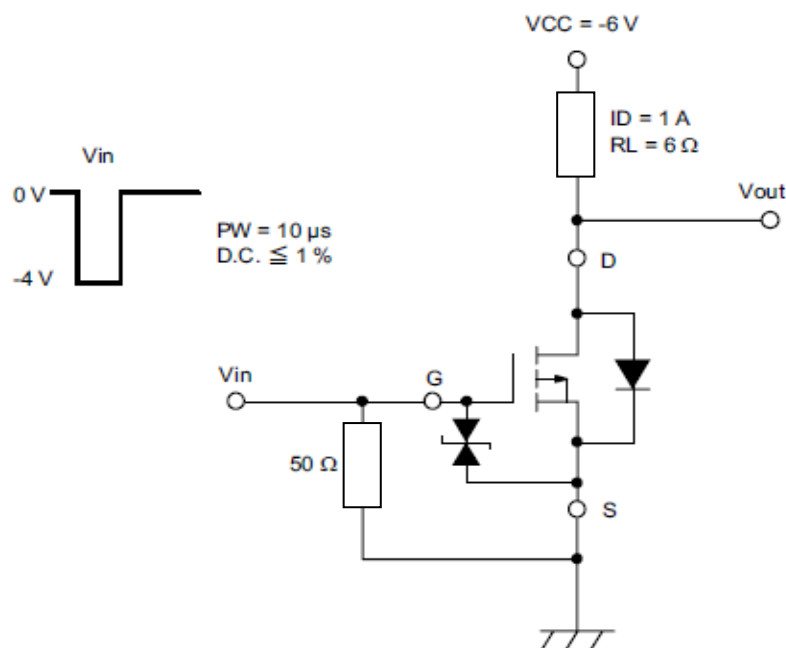
■ Electrical Characteristics Ta = 25°C ± 3°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	VDSS	ID = -1 mA, VGS = 0	-12			V
Drain-source cutoff current	IDSS	VDS = -12 V, VGS = 0			-1.0	μA
Gate-source cutoff current	IGSS	VGS = ±6.4 V, VDS = 0			±10	μA
Gate threshold voltage	Vth	ID = -1.0 mA, VDS = -6.0 V	-0.3	-0.65	-1.0	V
Drain-source ON resistance	RDS(ON)1	ID = -1.0 A, VGS = -4.0 V		32	42	mΩ
	RDS(ON)2	ID = -0.5 A, VGS = -2.5 V		37	55	mΩ
	RDS(ON)3	ID = -0.2 A, VGS = -1.8 V		50	75	mΩ
Forward transfer admittance	Yfs	ID = -1.0 A, VDS = -10 V	3.5			S
Short-circuit input capacitance (Common source)	Ciss	VDS = -10 V, VGS = 0, f = 1 MHz		1200		pF
Short-circuit output capacitance (Common source)	Coss			110		pF
Reverse transfer capacitance (Common source)	Crss			110		pF
Turn-on delay time <sup>*1</sup>	td(on)	VDD = -6 V, VGS = 0 V to -4 V		8		ns
Rise time <sup>*1</sup>	tr	ID = -1.0 A		11		ns
Turn-off delay time <sup>*1</sup>	td(off)	VDD = -6 V, VGS = -4 V to 0 V		235		ns
Fall time <sup>*1</sup>	tf	ID = -1.0 A		85		ns

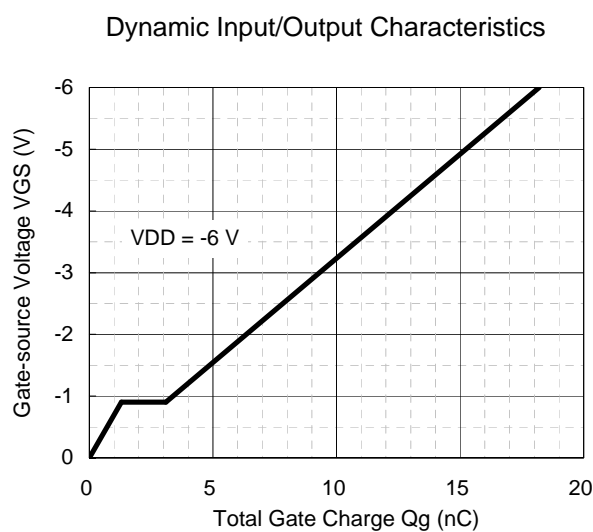
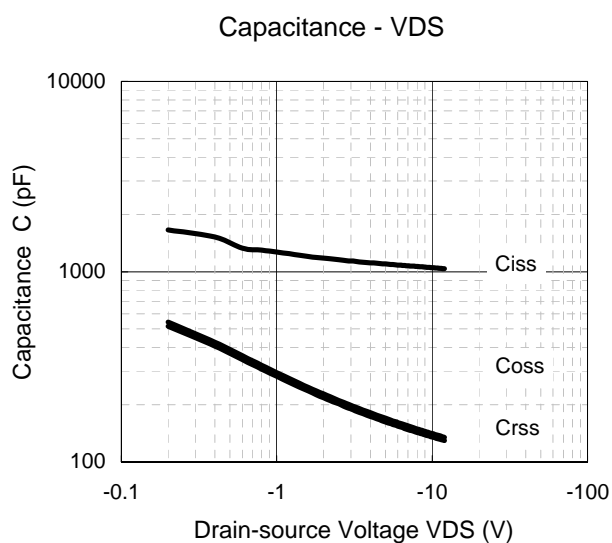
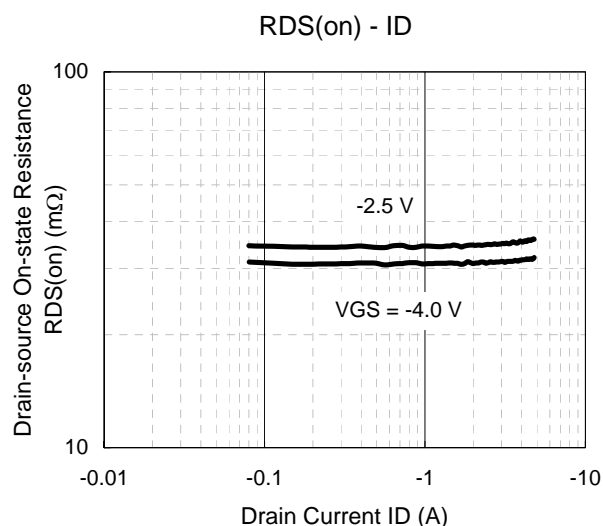
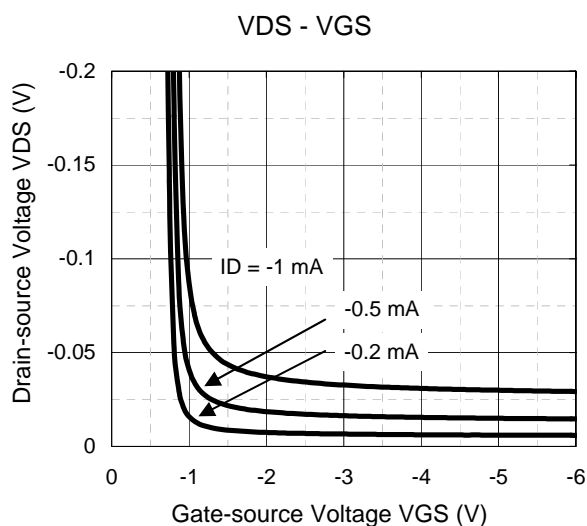
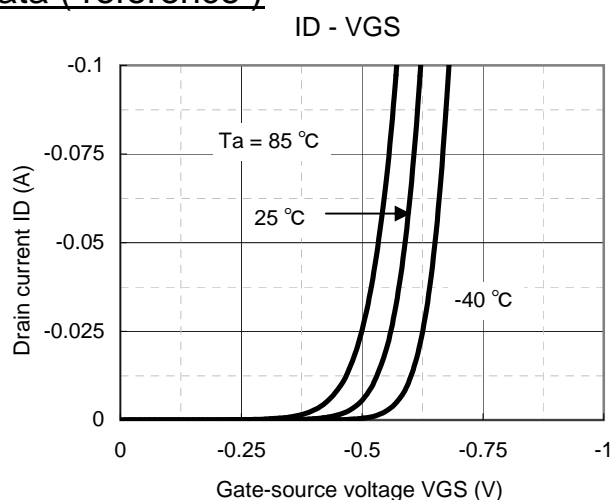
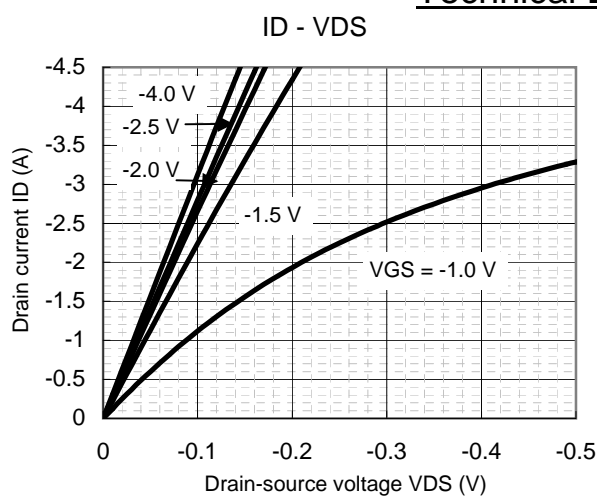
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

2. \*1 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

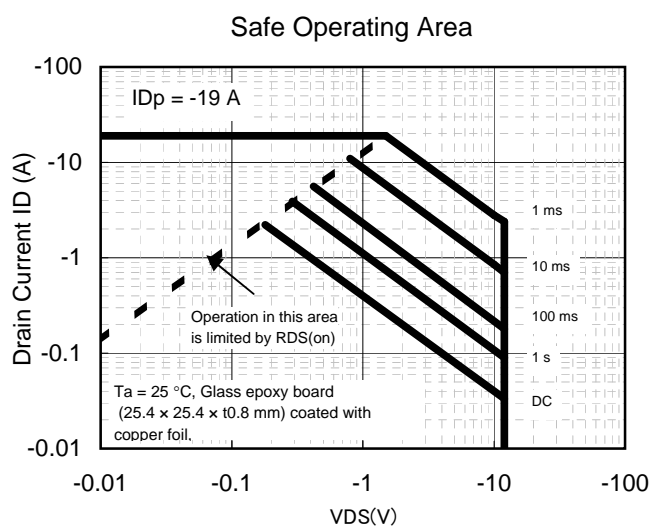
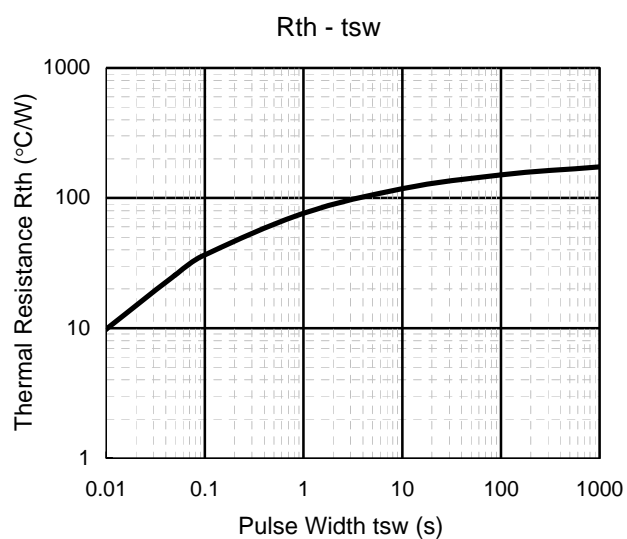
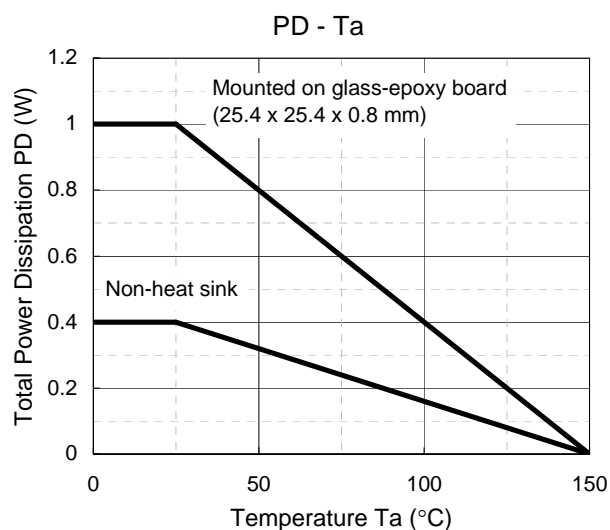
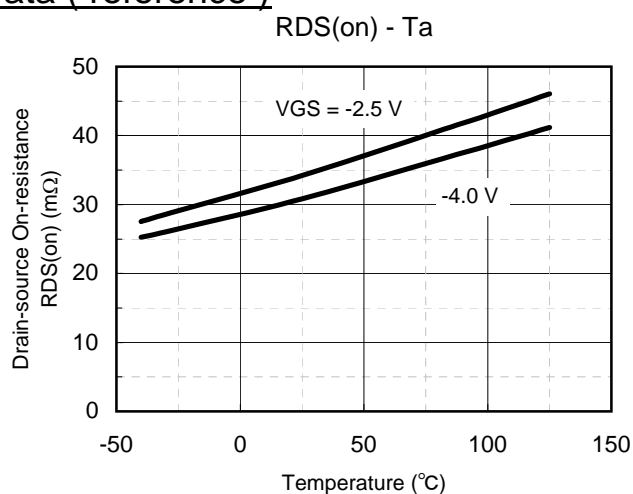
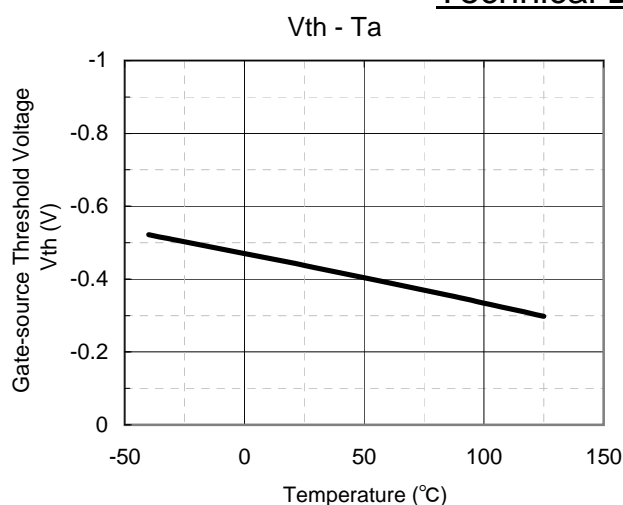
\*2 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time



Technical Data ( reference )

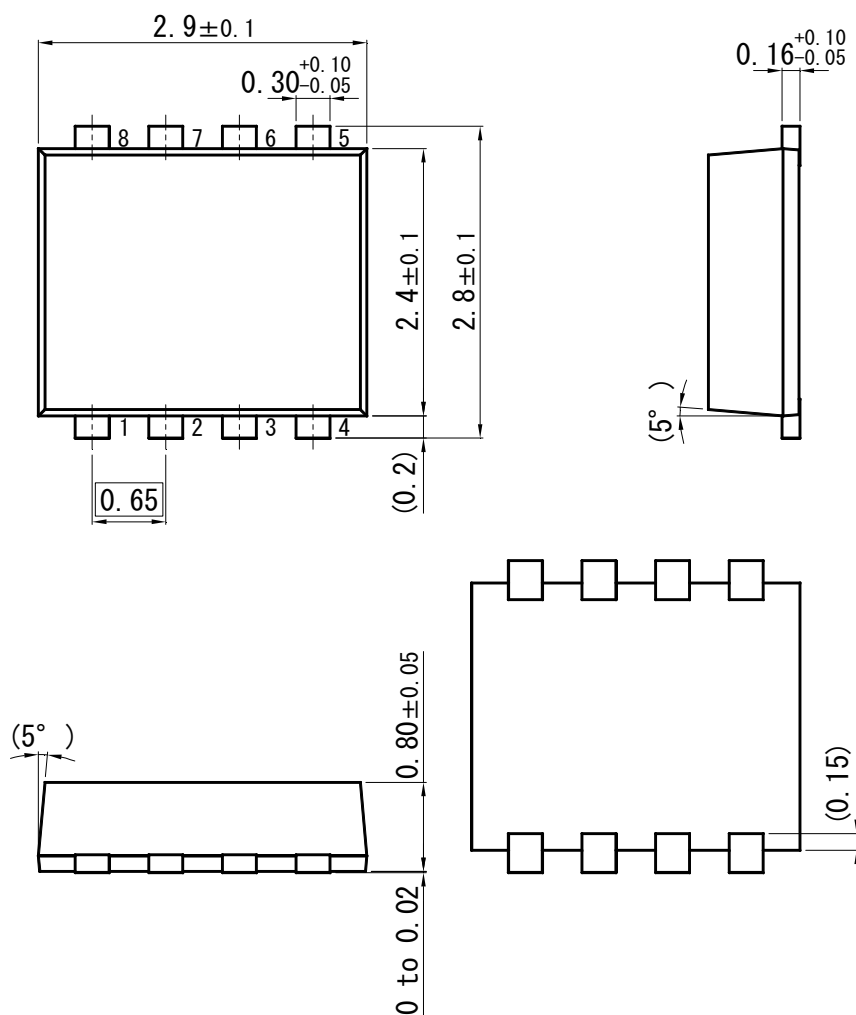


# Technical Data ( reference )

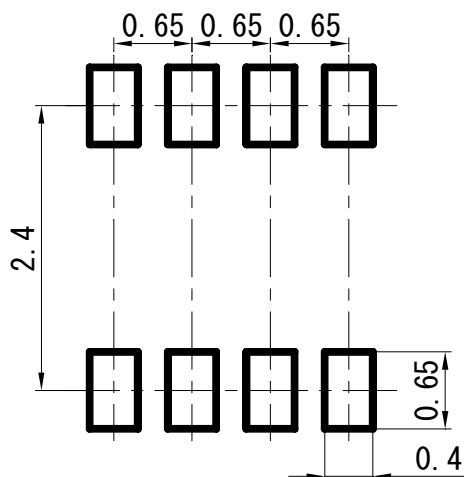


WMini8-F1

Unit : mm



■ Land Pattern (Reference) (Unit : mm)



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