

MOSFET – Power, Single N-Channel

40 V, 1.1 mΩ, 258 A

NVMYS1D2N04CL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPAK4 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter		Value	Unit
V _{DSS}	Drain-to-Source Voltage		40	V
V _{GS}	Gate-to-Source Voltage		±20	V
I _D	Continuous Drain Current R _{θJC} (Notes 1, 3)	Steady State	T _C = 25 °C	258
			T _C = 100 °C	182
P _D	Power Dissipation R _{θJC} (Note 1)		T _C = 25 °C	134
			T _C = 100 °C	67
I _D	Continuous Drain Current R _{θJA} (Notes 1, 2, 3)	Steady State	T _A = 25 °C	44
			T _A = 100 °C	31
P _D	Power Dissipation R _{θJA} (Notes 1, 2)		T _A = 25 °C	3.9
			T _A = 100 °C	1.9
I _{DM}	Pulsed Drain Current	T _A = 25 °C, t _p = 10 μs	900	A
T _J , T _{stg}	Operating Junction and Storage Temperature Range		-55 to +175	°C
I _S	Source Current (Body Diode)		112	A
E _{AS}	Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 21 A)		1359	mJ
T _L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

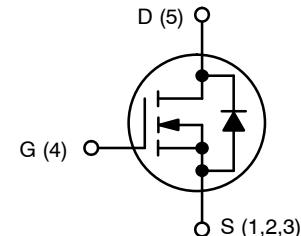
Symbol	Parameter	Value	Unit
R _{θJC}	Junction-to-Case - Steady State	1.12	°C/W
R _{θJA}	Junction-to-Ambient - Steady State (Note 2)	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

V _{(BR)DSS}	R _{DS(ON) MAX}	I _D MAX
40 V	1.1 mΩ @ 10 V	258 A
	1.7 mΩ @ 4.5 V	

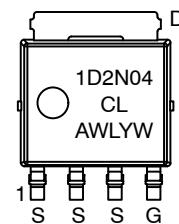


LFPAK4
CASE 760AB



N-CHANNEL MOSFET

MARKING DIAGRAM



1D2N04CL = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMYS1D2N04CL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA		40	–	–	V
V _{(BR)DSS/T_J}	Drain-to-Source Breakdown Voltage Temperature Coefficient			–	20	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25 °C	–	–	10	μA
			T _J = 125 °C	–	–	100	
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V		–	–	100	nA

ON CHARACTERISTICS (Note 4)

V _{GS(TH)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 180 μA		1.2	–	2.0	V
V _{GS(TH)/T_J}	Threshold Temperature Coefficient			–	–5.6	–	mV/°C
R _{D(on)}	Drain-to-Source On Resistance	V _{GS} = 4.5 V	I _D = 50 A	–	1.4	1.7	mΩ
		V _{GS} = 10 V	I _D = 50 A	–	0.9	1.2	
g _{FS}	Forward Transconductance	V _{DS} = 15 V, I _D = 50 A		–	285	–	S

CHARGES, CAPACITANCES & GATE RESISTANCE

C _{ISS}	Input Capacitance	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 20 V	–	6330	–	pF
C _{OSS}	Output Capacitance		–	3000	–	
C _{RSS}	Reverse Transfer Capacitance		–	118	–	
Q _{G(TOT)}	Total Gate Charge	V _{GS} = 4.5 V, V _{DS} = 20 V; I _D = 50 A	–	52	–	nC
Q _{G(TOT)}	Total Gate Charge		–	109	–	nC
Q _{G(TH)}	Threshold Gate Charge		–	9.0	–	
Q _{GS}	Gate-to-Source Charge	V _{GS} = 10 V, V _{DS} = 20 V; I _D = 50 A	–	16	–	
Q _{GD}	Gate-to-Drain Charge		–	20	–	
V _{GP}	Plateau Voltage		–	2.9	–	V

SWITCHING CHARACTERISTICS (Note 5)

t _{d(ON)}	Turn-On Delay Time	V _{GS} = 10 V, V _{DS} = 32 V, I _D = 50 A, R _G = 2.5 Ω	–	14	–	ns
t _r	Rise Time		–	8.1	–	
t _{d(OFF)}	Turn-Off Delay Time		–	79	–	
t _f	Fall Time		–	22	–	

DRAIN-SOURCE DIODE CHARACTERISTICS

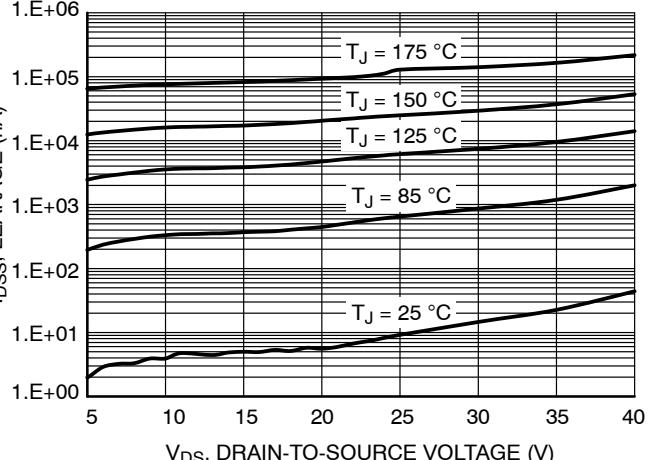
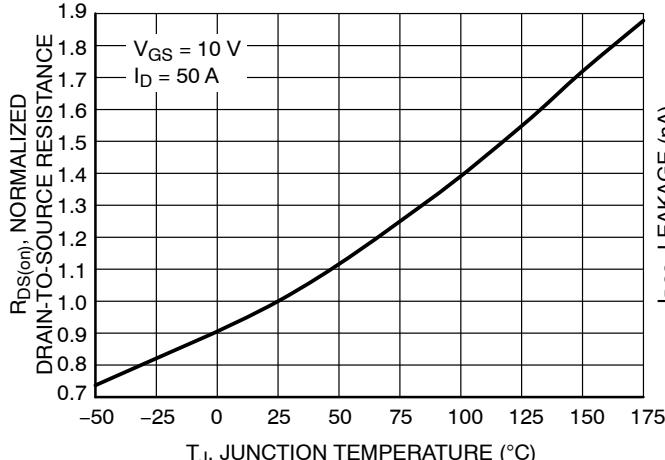
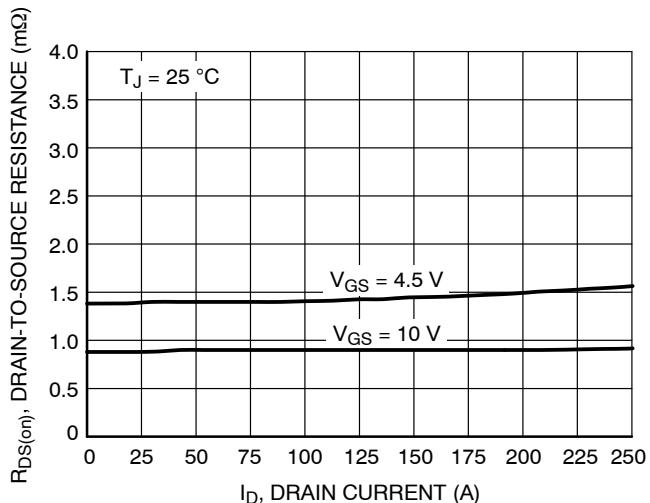
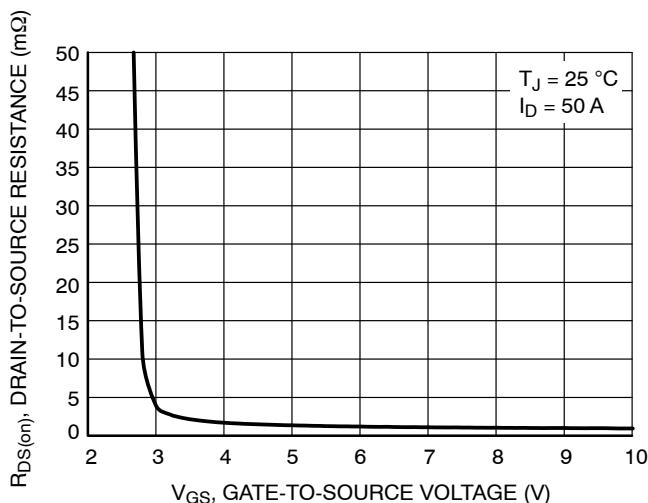
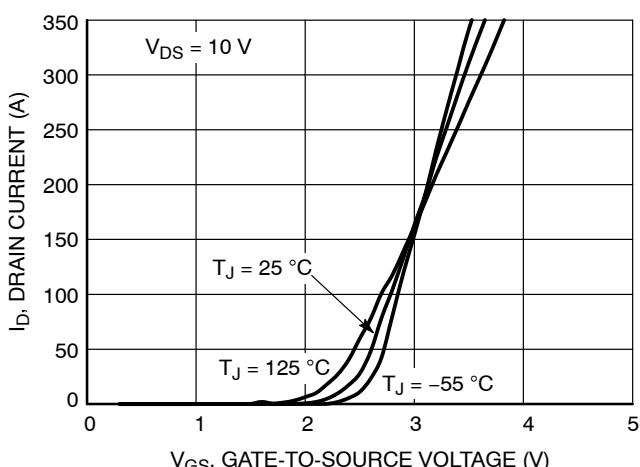
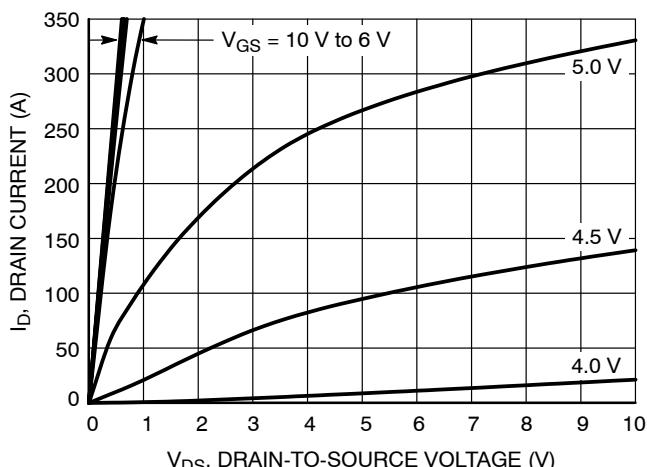
V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = 50 A	T _J = 25 °C	–	0.80	1.2	V
			T _J = 125 °C	–	0.65	–	
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 50 A	–	70	–	ns	
			–	42	–		
			–	28	–		
			–	107	–	nC	
Q _{RR}	Reverse Recovery Charge						

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

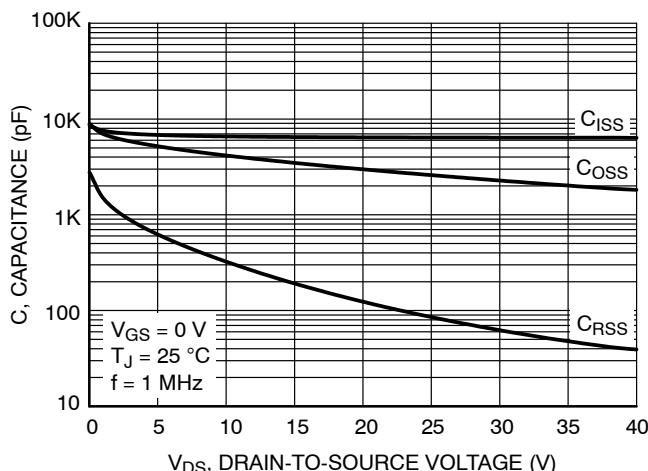


Figure 7. Capacitance Variation

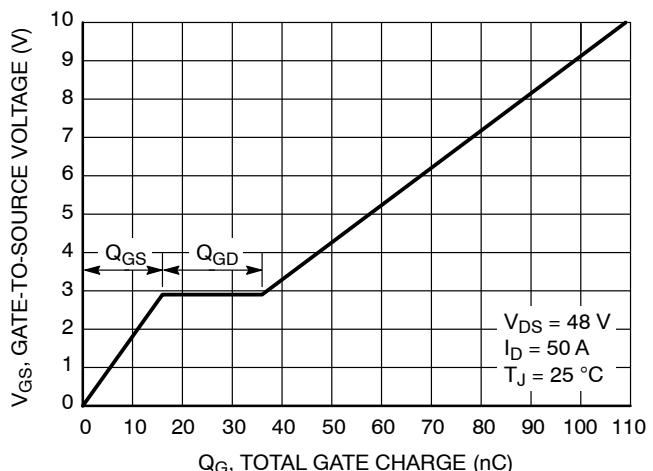


Figure 8. Gate-to-Source vs. Total Charge

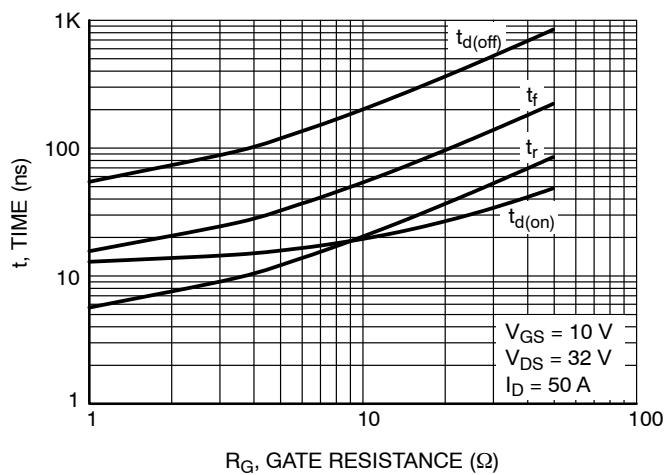


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

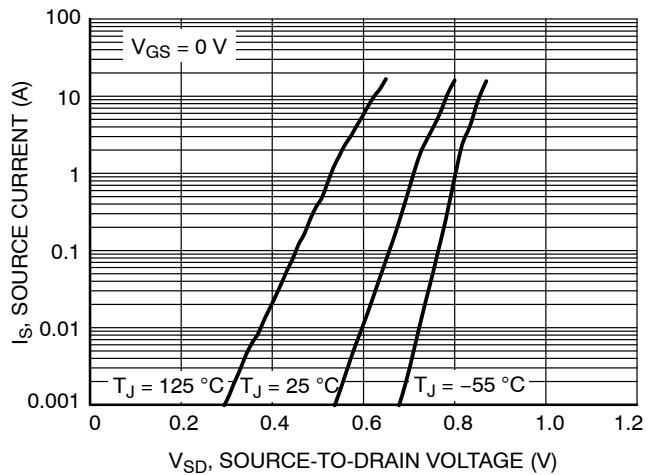


Figure 10. Diode Forward Voltage vs. Current

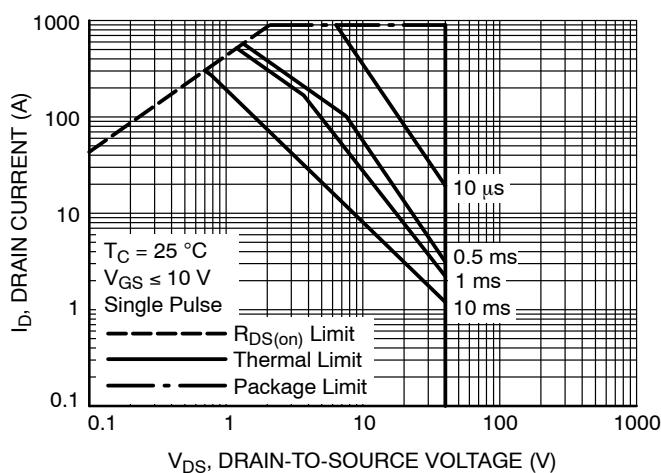


Figure 11. Maximum Rated Forward Biased Safe Operating Area

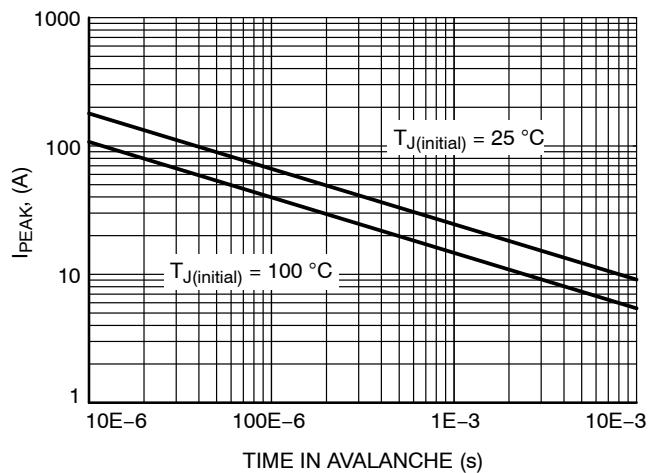


Figure 12. Maximum Drain Current vs. Time in Avalanche

NVMYS1D2N04CL

TYPICAL CHARACTERISTICS (continued)

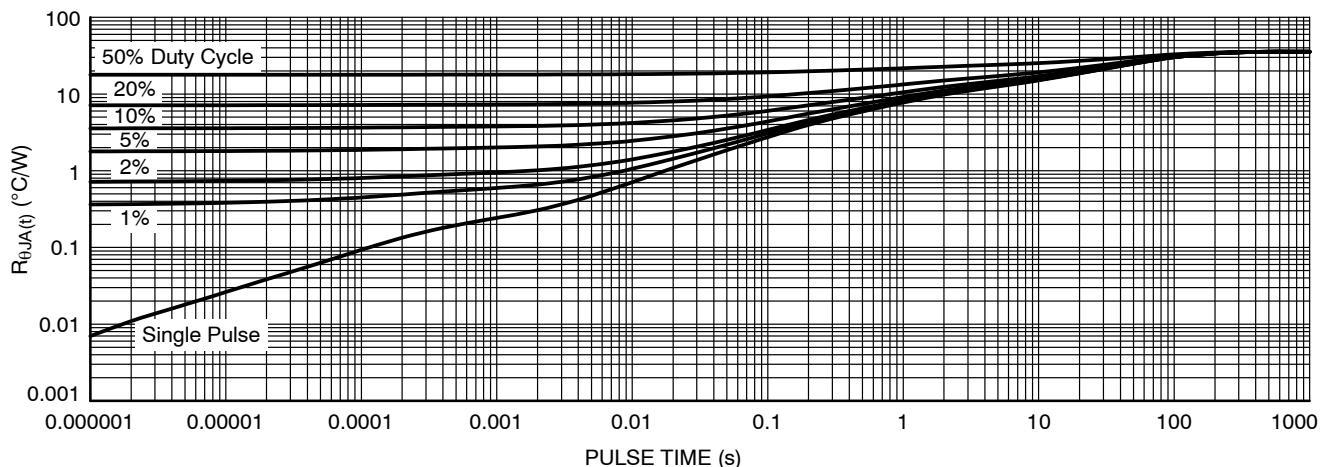


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMYS1D2N04CLTWG	1D2N04CL	LFPAK4 (Pb-Free)	3,000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

REVISION HISTORY

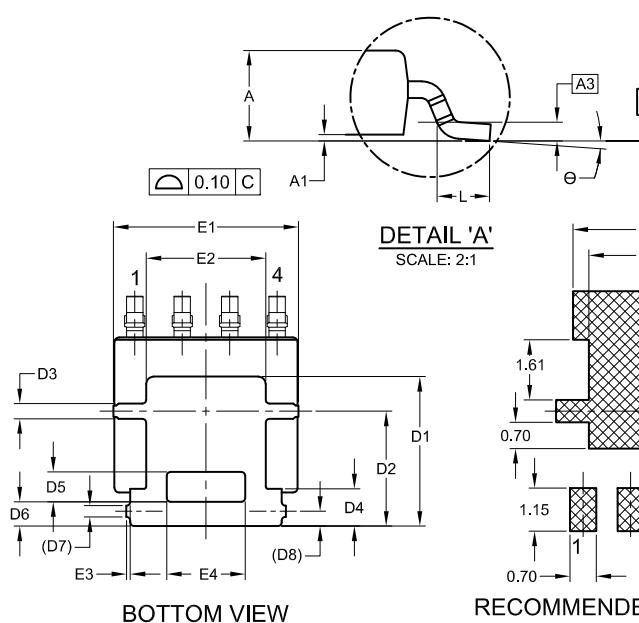
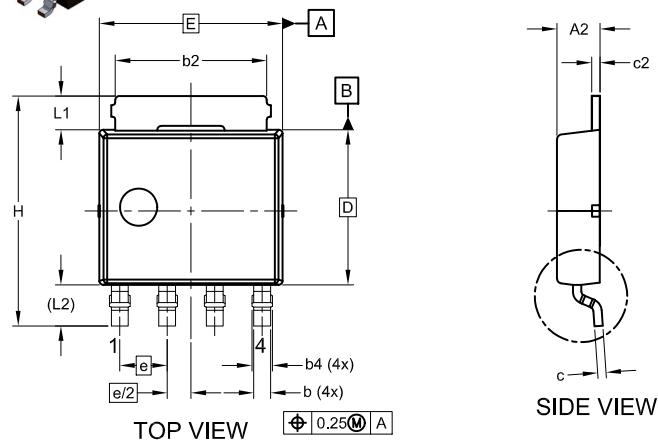
Revision	Description of Changes	Date
1	Rebranded the Data Sheet to onsemi format.	11/6/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



LFPAK4 4.90x4.15x1.15MM, 1.27P
CASE 760AB
ISSUE D

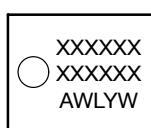
DATE 22 MAY 2024



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SODERRM/D.

**GENERIC
MARKING DIAGRAM***



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

MILLIMETER			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 BSC		
b	0.40	0.45	0.50
b2	3.80	4.10	4.40
b4	0.45	0.55	0.65
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.15 BSC		
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
D4	0.90	1.00	1.10
D5	0.70	0.80	0.90
D6	0.55	0.65	0.75
D7	0.31 REF		
D8	0.40 REF		
E	4.90 BSC		
E1	4.85	4.95	5.05
E2	3.10	3.20	3.30
E3	0.00	0.10	0.20
E4	2.00	2.10	2.20
e	1.27 BSC		
e/2	0.635 BSC		
e1	0.40 REF		
H	6.00	6.15	6.30
L	0.50	0.70	0.90
L1	0.80	0.90	1.00
L2	1.10 REF		
Theta	0°	4°	8°

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DESCRIPTION:	LFPAK4 4.90x4.15x1.15MM, 1.27P	PAGE 1 OF 1

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