

FEATURES

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Widebus™ Design for 2.5-V and 3.3-V Operation and Low Static Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **High Drive ($-24/24$ mA at 2.5-V V_{CC} and $-32/64$ mA at 3.3-V)**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **High-Impedance State During Power Up and Power Down Prevents Driver Conflict**
- **Uses Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating**
- **Auto3-State Eliminates Bus Current Loading When Output Exceeds $V_{CC} + 0.5$ V**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection**
 - Exceeds 2000 V Per MIL-STD-883, Method 3015
 - Exceeds 200 V Using Machine Model
 - Exceeds 1000 V Using Charged-Device Model, Robotic Method
- **Flow-Through Architecture Facilitates Printed Circuit Board Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package**

**SN54ALVTH16374...WD PACKAGE
SN74ALVTH16374...DGG, DGV, OR DL PACKAGE
(TOP VIEW)**

1OE	1	48	1CLK
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
V_{CC}	7	42	V_{CC}
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
V_{CC}	18	31	V_{CC}
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
2OE	24	25	2CLK

DESCRIPTION/ORDERING INFORMATION

The 'ALVTH16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the flip-flops store the logic levels set up at the data (D) inputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SN54ALVTH16374, SN74ALVTH16374

2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

SCES068G–JUNE 1996–REVISED NOVEMBER 2006

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

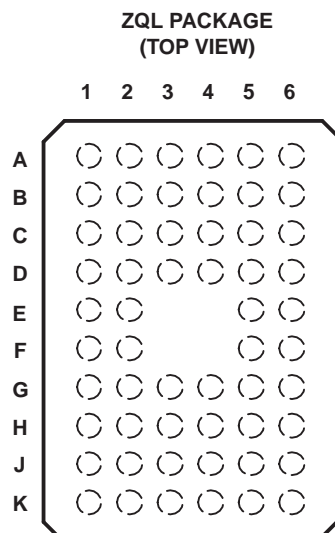
When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ALVTH16374 is characterized for operation over the full military temperature range of -55°C to 125°C .

The SN74ALVTH16374 is characterized for operation from -40°C to 85°C .

ORDERING INFORMATION

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – DGG	Reel of 2000	74ALVTH16374GRE4	
			SN74ALVTH16374GR	
	TVSOP – DGV	Reel of 2000	74ALVTH16374VRE4	
			SN74ALVTH16374VR	
	SSOP – DL	Tube of 25	74ALVTH16374DL	
			SN74ALVTH16374DLG4	
		Reel of 1000	SN74ALVTH16374DLR	
			SN74ALVTH16374DLRG4	



TERMINAL ASSIGNMENTS⁽¹⁾

	1	2	3	4	5	6
A	1 \overline{OE}	NC	NC	NC	NC	1CLK
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	V _{CC}	V _{CC}	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	V _{CC}	V _{CC}	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	2 \overline{OE}	NC	NC	NC	NC	2CLK

(1) NC – No internal connection

**FUNCTION TABLE
(each 8-bit section)**

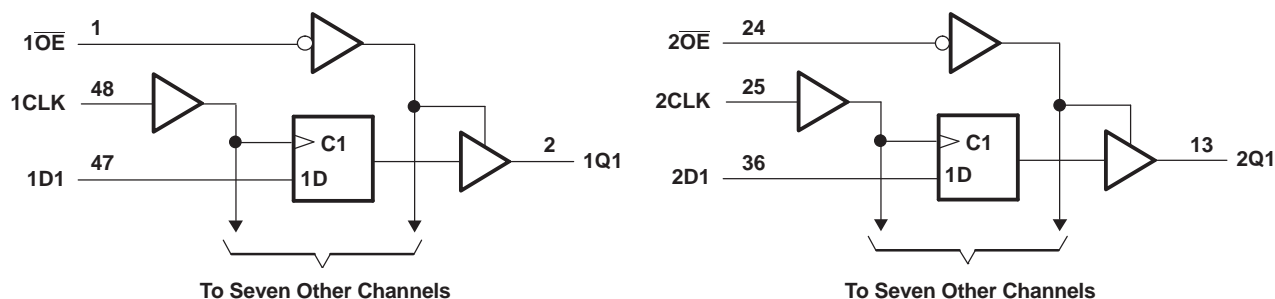
INPUTS			OUTPUT Q
\overline{OE}	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀
H	X	X	Z

SN54ALVTH16374, SN74ALVTH16374

2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCES068G–JUNE 1996–REVISED NOVEMBER 2006

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DL, and WD packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	4.6	V
V_I	Input voltage range ⁽²⁾	–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	7	V
V_O	Voltage range applied to any output in the high state ⁽²⁾	–0.5	7	V
I_O	Output current in the low state	SN54ALVTH16374 ⁽³⁾		96
		SN74ALVTH16374		128
I_O	Output current in the high state	SN54ALVTH16374 ⁽³⁾		–48
		SN74ALVTH16374		–64
I_{IK}	Input clamp current	$V_I < 0$	–50	mA
I_{OK}	Output clamp current	$V_O < 0$	–50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package		89
		DGV package		93
		DL package		94
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) Product preview

(4) The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions⁽¹⁾

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

		SN54ALVTH16374 ⁽²⁾			SN74ALVTH16374			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	2.3		2.7	2.3		2.7	V
V_{IH}	High-level input voltage	1.7			1.7			V
V_{IL}	Low-level input voltage			0.7			0.7	V
V_I	Input voltage	0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current			–6			–8	mA
I_{OL}	Low-level output current			6			8	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$			18			24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
T_A	Operating free-air temperature	–55		125	–40		85	$^{\circ}\text{C}$

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

(2) Product preview

Recommended Operating Conditions⁽¹⁾

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

		SN54ALVTH16374 ⁽²⁾			SN74ALVTH16374			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	3		3.6	3		3.6	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current			–24			–32	mA
I_{OL}	Low-level output current			24			32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$			48			64	
$\Delta t/\Delta v$	Input transition rise or fall rate			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
T_A	Operating free-air temperature	–55		125	–40		85	$^{\circ}\text{C}$

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

(2) Product preview

SN54ALVTH16374, SN74ALVTH16374

2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCES068G–JUNE 1996–REVISED NOVEMBER 2006

Electrical Characteristics

over operating free-air temperature range $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH16374 ⁽¹⁾		SN74ALVTH16374		UNIT
				MIN	TYP ⁽²⁾	MAX	MIN	
V _{IK}		V _{CC} = 2.3 V,	I _I = −18 mA	−1.2		−1.2		V
V _{OH}		V _{CC} = 2.3 V to 2.7 V, I _{OH} = −100 μA		V _{CC} − 0.2		V _{CC} − 0.2		V
		V _{CC} = 2.3 V	I _{OH} = −6 mA	1.8				
			I _{OH} = −8 mA			1.8		
V _{OL}		V _{CC} = 2.3 V to 2.7 V, I _{OL} = 100 μA		0.2		0.2		V
		V _{CC} = 2.3 V	I _{OL} = 6 mA	0.4				
			I _{OL} = 8 mA			0.4		
			I _{OL} = 18 mA	0.5				
			I _{OL} = 24 mA			0.5		
I _I	Control inputs	V _{CC} = 2.7 V,	V _I = V _{CC} or GND	±1		±1		μA
		V _{CC} = 0 or 2.7 V,	V _I = 5.5 V	10		10		
	Data inputs	V _{CC} = 2.7 V	V _I = 5.5 V	10		10		
			V _I = V _{CC}	1		1		
			V _I = 0	−5		−5		
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100		μA
I _{BHL} ⁽³⁾		V _{CC} = 2.3 V,	V _I = 0.7 V	115		115		μA
I _{BHH} ⁽⁴⁾		V _{CC} = 2.3 V,	V _I = 1.7 V	−10		−10		μA
I _{BHLO} ⁽⁵⁾		V _{CC} = 2.7 V,	V _I = 0 to V _{CC}	300		300		μA
I _{BHHO} ⁽⁶⁾		V _{CC} = 2.7 V,	V _I = 0 to V _{CC}	−300		−300		μA
I _{EX} ⁽⁷⁾		V _{CC} = 2.3 V,	V _O = 5.5 V	125		125		μA
I _{OZ(PU/PD)} ⁽⁸⁾		V _{CC} ≤ 1.2 V, V _O = 0.5 V to V _{CC} , V _I = GND or V _{CC} , \overline{OE} = don't care		±100		±100		μA
I _{OZH}		V _{CC} = 2.7 V, V _O = 2.3 V, V _I = 0.7 V or 1.7 V		5		5		μA
I _{OZL}		V _{CC} = 2.7 V, V _O = 0.5 V, V _I = 0.7 V or 1.7 V		−5		−5		μA
I _{CC}		V _{CC} = 2.7 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	0.04	0.1	0.1		mA
			Outputs low	2.3	4.5	4.5		
			Outputs disabled	0.04	0.1	0.1		
C _i		V _{CC} = 2.5 V,	V _I = 2.5 V or 0	3.5				pF
C _o		V _{CC} = 2.5 V,	V _O = 2.5 V or 0	6				pF

(1) Product preview

(2) All typical values are at $V_{CC} = 2.5 \text{ V}$, $T_A = 25^\circ\text{C}$.

(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

(5) An external driver must source at least I_{BHLO} to switch this node from low to high.

(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.

(7) Current into an output in the high state when $V_O > V_{CC}$

(8) High-impedance state during power up or power down

Electrical Characteristics

over recommended operating free-air temperature range $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH16374 ⁽¹⁾			SN74ALVTH16374			UNIT	
				MIN	TYP ⁽²⁾	MAX	MIN	TYP ⁽²⁾	MAX		
V _{IK}		V _{CC} = 3 V, I _I = −18 mA		−1.2			−1.2			V	
V _{OH}		V _{CC} = 3 V to 3.6 V, I _{OH} = −100 μA		V _{CC} − 0.2			V _{CC} − 0.2			V	
		V _{CC} = 3 V I _{OH} = −24 mA		2							
		I _{OH} = −32 mA					2				
V _{OL}		V _{CC} = 3 V to 3.6 V, I _{OL} = 100 μA		0.2			0.2			V	
		V _{CC} = 3 V		I _{OL} = 16 mA					0.4		
				I _{OL} = 24 mA		0.5					
				I _{OL} = 32 mA					0.5		
				I _{OL} = 48 mA		0.55					
				I _{OL} = 64 mA					0.55		
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1			±1			μA	
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10			10				
	Data inputs	V _{CC} = 3.6 V V _I = 5.5 V		10			10				
		V _I = V _{CC}		1			1				
		V _I = 0		−5			−5				
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100			μA	
I _{BHL} ⁽³⁾		V _{CC} = 3 V, V _I = 0.8 V		75			75			μA	
I _{BHH} ⁽⁴⁾		V _{CC} = 3 V, V _I = 2 V		−75			−75			μA	
I _{BHLO} ⁽⁵⁾		V _{CC} = 3.6 V, V _I = 0 to V _{CC}		500			500			μA	
I _{BHHO} ⁽⁶⁾		V _{CC} = 3.6 V, V _I = 0 to V _{CC}		−500			−500			μA	
I _{EX} ⁽⁷⁾		V _{CC} = 3 V, V _O = 5.5 V		125			125			μA	
I _{OZ(PU/PD)} ⁽⁸⁾		V _{CC} ≤ 1.2 V, V _O = 0.5 V to V _{CC} , V _I = GND or V _{CC} , \overline{OE} = don't care		±100			±100			μA	
I _{OZH}		V _{CC} = 3.6 V, V _O = 3 V, V _I = 0.8 V or 27 V		5			5			μA	
I _{OZL}		V _{CC} = 3.6 V, V _O = 0.5 V, V _I = 0.8 V or 2 V		−5			−5			μA	
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.07	0.1	0.07		0.1	mA
				Outputs low		3.2	5	3.2		5	
				Outputs disabled		0.07	0.1	0.1			
ΔI _{CC} ⁽⁹⁾		V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.4			0.4			mA	
C _i		V _{CC} = 3.3 V, V _I = 3.3 V or 0		3.5			3.5			pF	
C _o		V _{CC} = 3.3 V, V _O = 3.3 V or 0		6			6			pF	

(1) Product preview

(2) All typical values are at $V_{CC} = 2.5 \text{ V}$, $T_A = 25^\circ\text{C}$.

(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

(5) An external driver must source at least I_{BHLO} to switch this node from low to high.

(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.

(7) Current into an output in the high state when $V_O > V_{CC}$

(8) High-impedance state during power up or power down

(9) This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54ALVTH16374, SN74ALVTH16374

2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

SCES068G–JUNE 1996–REVISED NOVEMBER 2006

Timing Requirements

over recommended operating free-air temperature range $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see [Figure 1](#))

			SN54ALVTH16374 ⁽¹⁾		SN74ALVTH16374		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		150		150		MHz
t _w	Pulse duration, CLK high or low		1.5		1.5		ns
t _{su}	Setup time, data before CLK↑	Data high	1.1		1		ns
		Data low	1.4		1.3		
t _h	Hold time, data after CLK↑	Data high	0.6		0.5		ns
		Data low	0.9		0.8		

(1) Product preview

Timing Requirements

over recommended operating free-air temperature range $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Figure 2](#))

			SN54ALVTH16374 ⁽¹⁾		SN74ALVTH16374		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		25		250		MHz
t _w	Pulse duration, CLK high or low		1.5		1.5		ns
t _{su}	Setup time, data before CLK↑	Data high	1.1		1		ns
		Data low	1.6		1.5		
t _h	Hold time, data after CLK↑	Data high	0.6		0.5		ns
		Data low	1.1		1		

(1) Product preview

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16374 ⁽¹⁾		SN74ALVTH16374		UNIT
			MIN	MAX	MIN	MAX	
f_{\max}			150		150		MHz
t_{PLH}	CLK	Q	1.4	3.9	1.5	3.8	ns
t_{PHL}			1.4	3.9	1.5	3.8	
t_{PZH}	\overline{OE}	Q	1	4.2	1	4.1	ns
t_{PZL}			1	3.8	1	3.7	
t_{PHZ}	\overline{OE}	Q	1.7	4.3	1.8	4.2	ns
t_{PLZ}			1	3.5	1	3.4	

(1) Product preview

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16374 ⁽¹⁾		SN74ALVTH16374		UNIT
			MIN	MAX	MIN	MAX	
f_{\max}			250		250		MHz
t_{PLH}	CLK	Q	1	3.4	1	3.2	ns
t_{PHL}			1	3.3	1	3.2	
t_{PZH}	\overline{OE}	Q	1	3.9	1	3.8	ns
t_{PZL}			1	3.4	1	3.3	
t_{PHZ}	\overline{OE}	Q	1	4.7	1	4.6	ns
t_{PLZ}			1	4.4	1	4.2	

(1) Product preview

SN54ALVTH16374, SN74ALVTH16374

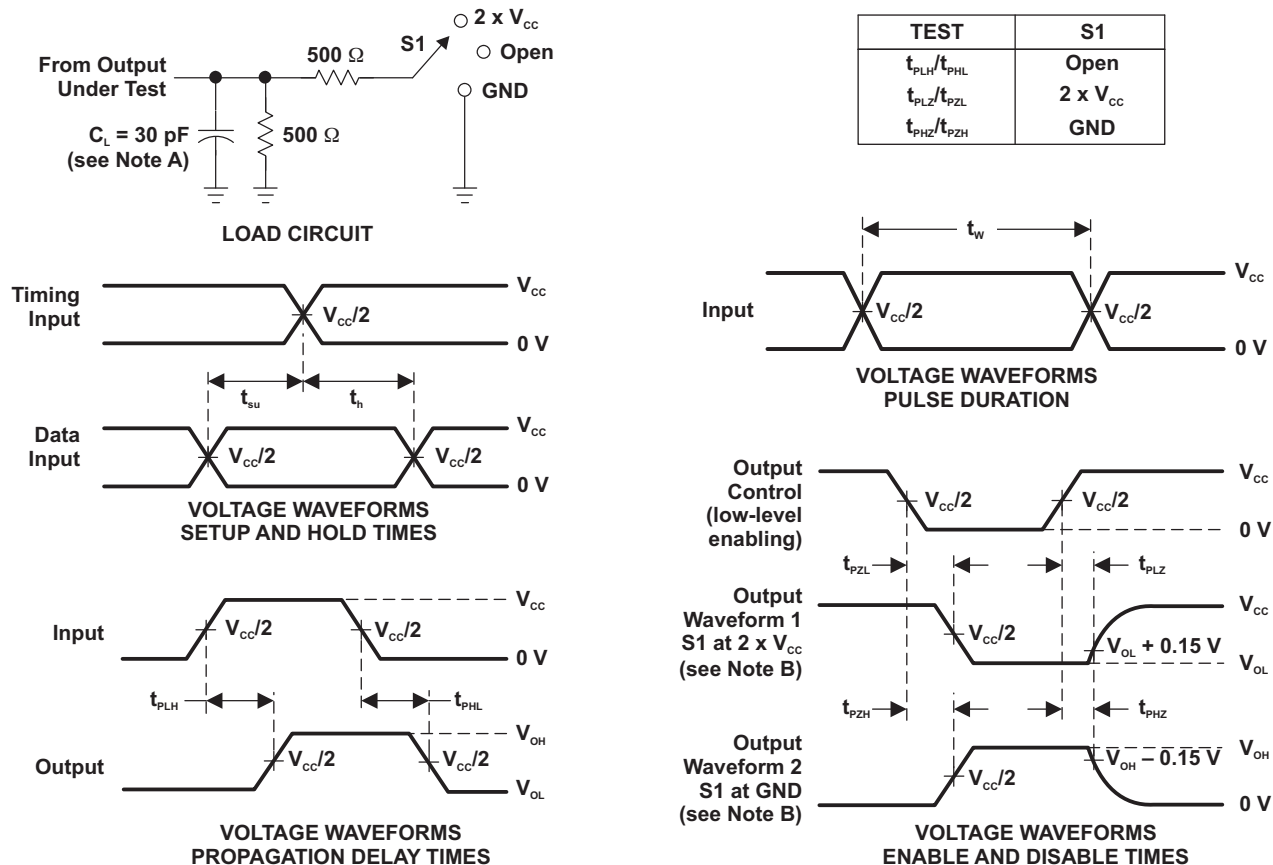
2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

SCES068G—JUNE 1996—REVISED NOVEMBER 2006

PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

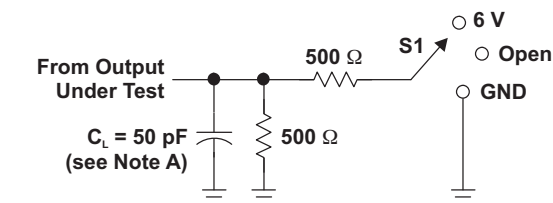


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.

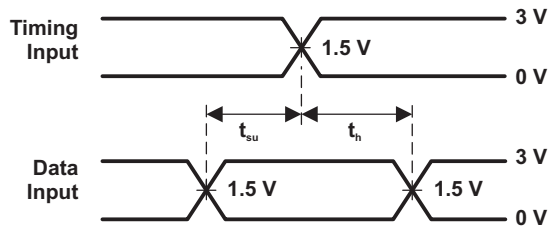
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

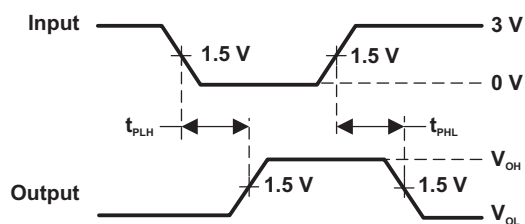
$$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$$



LOAD CIRCUIT

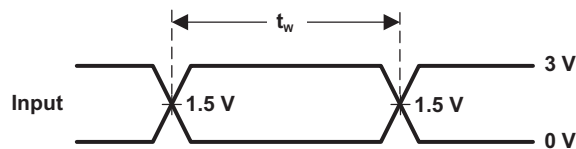


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

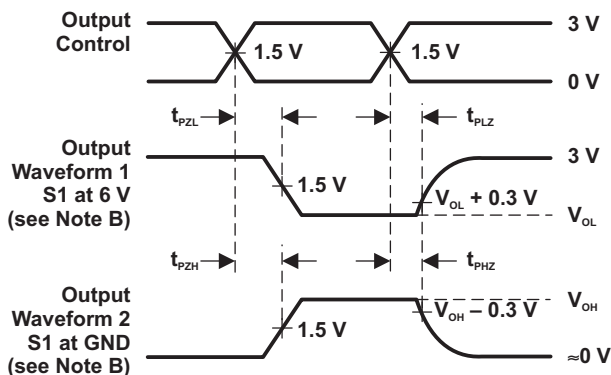


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVTH16374DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16374DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16374GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16374GRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16374VRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16374VRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16374ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74ALVTH16374DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16374DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16374GR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16374KR	NRND	BGA MICROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74ALVTH16374VR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the

accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ALVTH16374ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1
SN74ALVTH16374DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74ALVTH16374GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ALVTH16374KR	BGA MICROSTAR JUNIOR	GQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1
SN74ALVTH16374VR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ALVTH16374ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	346.0	346.0	33.0
SN74ALVTH16374DLR	SSOP	DL	48	1000	346.0	346.0	49.0
SN74ALVTH16374GR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74ALVTH16374KR	BGA MICROSTAR JUNIOR	GQL	56	1000	346.0	346.0	33.0
SN74ALVTH16374VR	TVSOP	DGV	48	2000	346.0	346.0	33.0

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

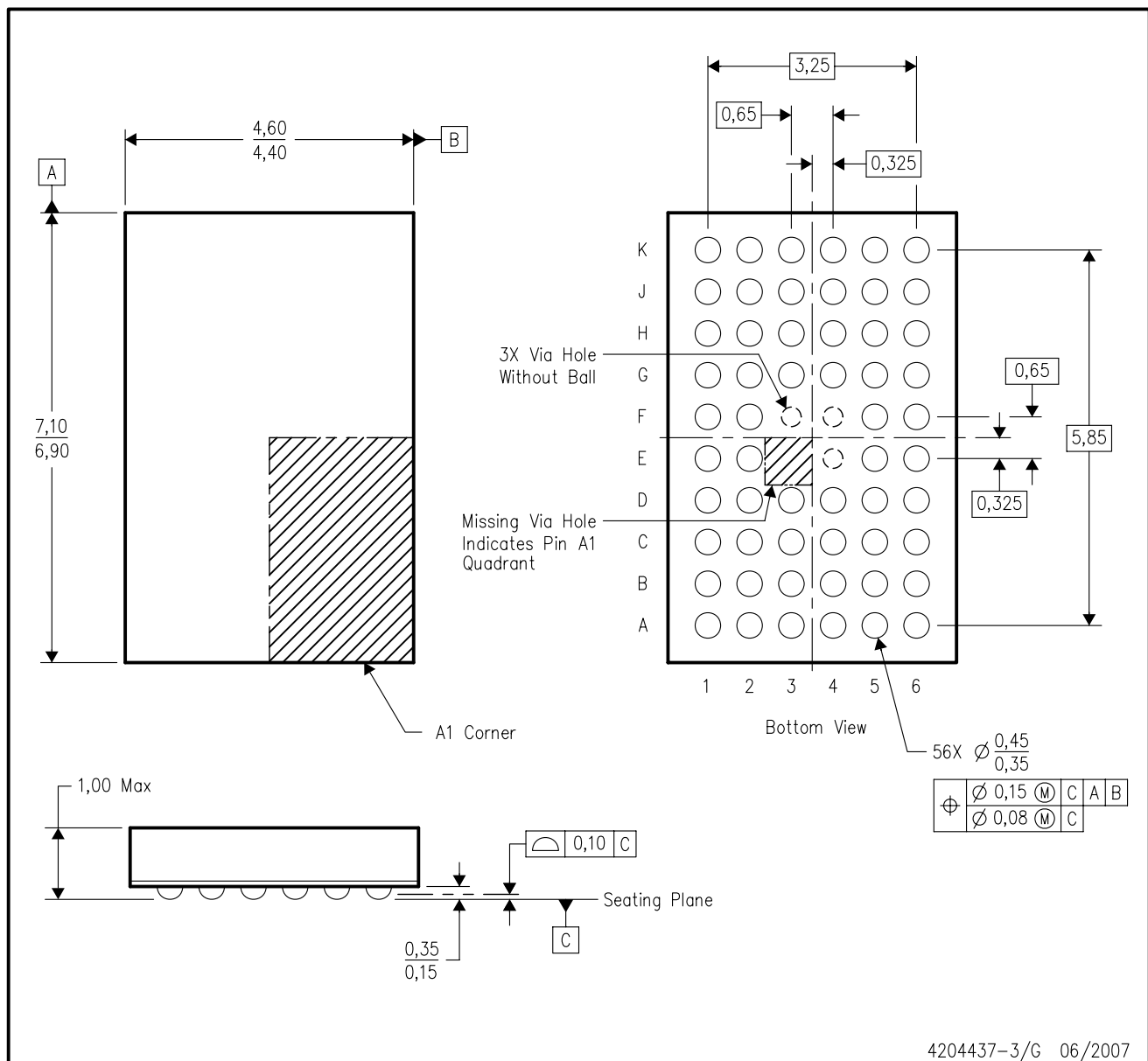


4200583-3/K 06/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



4204437-3/G 06/2007

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-285 variation BA-2.
 - This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated