

PNP SILICON POWER TRANSISTORS

.... designed for use in general purpose Power amplifier, vertical output application

FEATURES:

- * Collector-Emitter Voltage
 $V_{CEO} = 150V(\text{Min})$
- * DC Current Gain
 $hFE = 40-200 @ I_C = 400mA$
- * Complementary to PNP 2SB546A

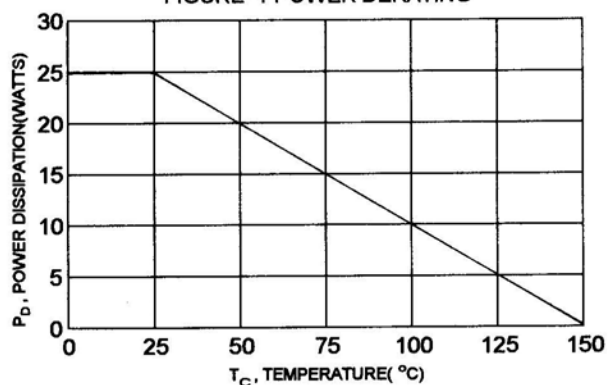
MAXIMUM RATINGS

Characteristic	Symbol	2SD401A	Unit
Collector-Emitter Voltage	V_{CEO}	150	V
Collector-Base Voltage	V_{CBO}	200	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Collector Current - Continuous - Peak	I_C I_{CM}	2.0 3.0	A
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	25 0.2	W W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

THERMAL CHARACTERISTICS

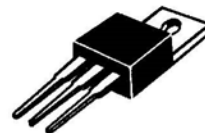
Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	$R_{\theta jc}$	5.0	$^\circ C/W$

FIGURE -1 POWER DERATING

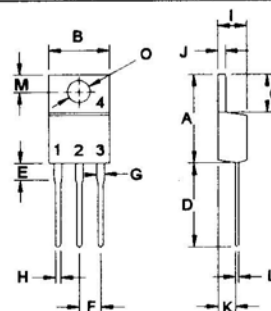


NPN 2SD401A

2 AMPERE
POWER
TRANSISTORS
150 VOLTS
25 WATTS



TO-220



PIN 1.BASE
2.COLLECTOR
3.EMITTER
4.COLLECTOR(CASE)

DIM	MILLIMETERS	
	MIN	MAX
A	14.68	16.00
B	9.78	10.42
C	5.02	6.60
D	13.00	14.62
E	3.10	4.19
F	2.41	2.67
G	1.10	1.67
H	0.69	1.01
I	3.21	4.98
J	1.14	1.40
K	2.20	3.30
L	0.28	0.61
M	2.48	3.00
O	3.50	4.00

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector Cutoff Current ($V_{CB} = 150\text{ V}$, $I_E = 0$)	I_{CBO}		50	μA
Emitter Cutoff Current ($V_{EB} = 4.0\text{ V}$, $I_C = 0$)	I_{EBO}		50	μA

ON CHARACTERISTICS (1)

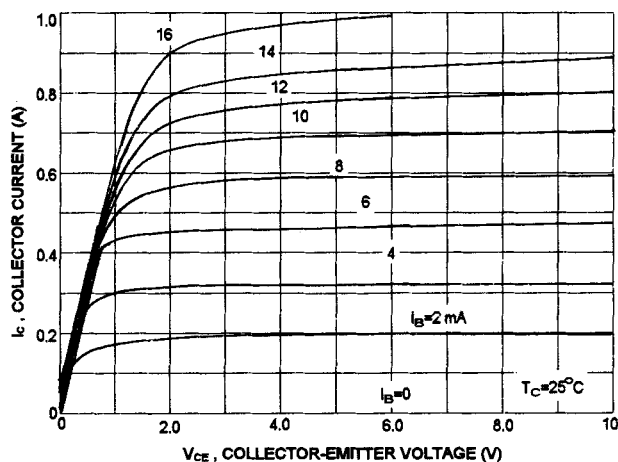
DC Current Gain * ($I_C = 0.4\text{ A}$, $V_{CE} = 10\text{ V}$)	$hFE(2)$	40	200	
Collector-Emitter Saturation Voltage ($I_C = 0.5\text{ A}$, $I_B = 50\text{ mA}$)	$V_{CE(sat)}$		1.0	V

DYNAMIC CHARACTERISTICS

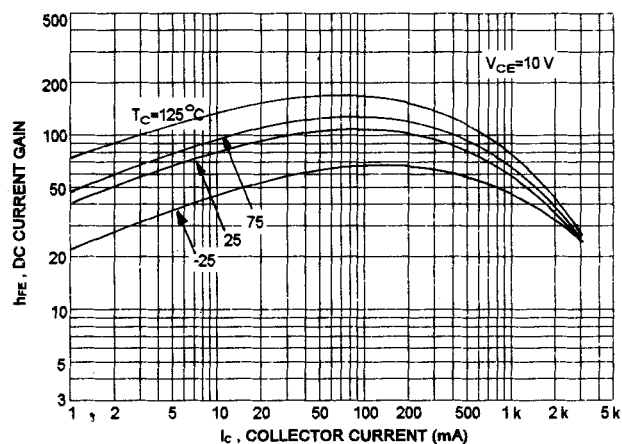
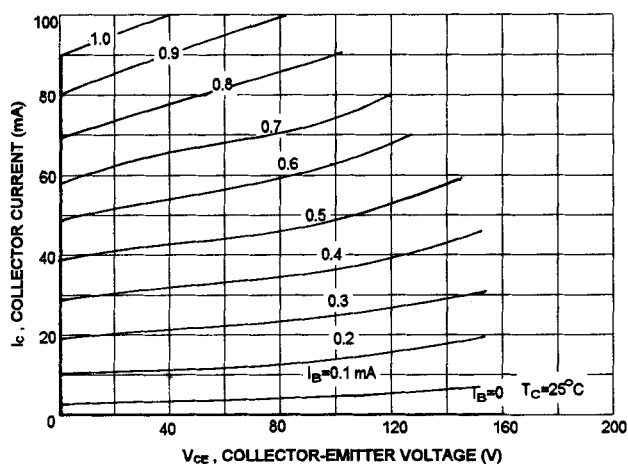
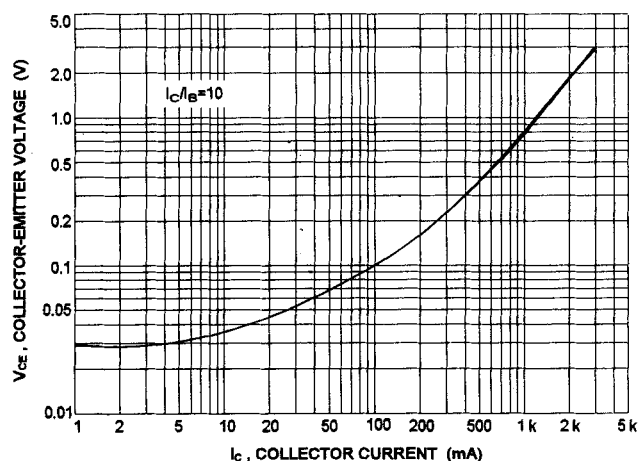
Current-Gain-Bandwidth Product ($I_C = 0.4\text{ A}$, $V_{CE} = 10\text{ V}$, $f = 1.0\text{ MHz}$)	f_T	5.0(typ)		MHz
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(1) Pulse Test: Pulse Width $\approx 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$ * $hFE(2)$ Classification:

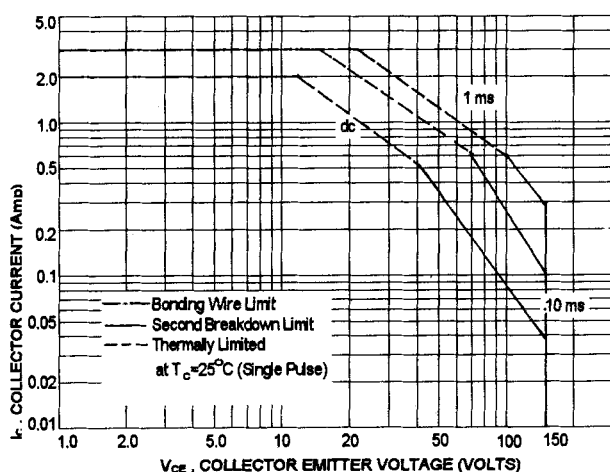
40	M	80	60	L	120	100	K	200
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$I_C - V_{CE}$ 

DC CURRENT GAIN

 $I_C - V_{CE}$  $V_{CE} - I_C$ 

ACTIVE-REGION SAFE OPERATING AREA (SOA)



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of SOA curve is based on $T_{J(PK)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(PK)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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