NCP5901

VR12 Compatible Synchronous Buck MOSFET Drivers

The NCP5901 is a high performance dual MOSFET gate driver optimized to drive the gates of both high−side and low−side power MOSFETs in a synchronous buck converter. It can drive up to 3 nF load with a 25 ns propagation delay and 20 ns transition time.

Adaptive anti−cross−conduction and power saving operation circuit can provide a low switching loss and high efficiency solution for notebook and desktop systems. Bidirectional EN pin can provide a fault signal to controller when the gate driver fault detect under OVP, UVLO occur. Also, an under−voltage lockout function guarantees the outputs are low when supply voltage is low.

Features

- Faster Rise and Fall Times
- Adaptive Anti−Cross−Conduction Circuit
- Pre OV function
- ZCD Detect
- Floating Top Driver Accommodates Boost Voltages of up to 35 V
- Output Disable Control Turns Off Both MOSFETs
- Under−voltage Lockout
- Power Saving Operation Under Light Load Conditions
- Direct Interface to NCP6151 and Other Compatible PWM Controllers
- Thermally Enhanced Package
- These are Pb−Free Devices

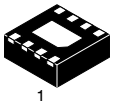
Typical Applications

- Power Solutions for Desktop Systems

ON Semiconductor®

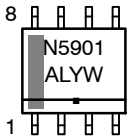
http://onsemi.com

SOIC−8 NB
D SUFFIX
CASE 751

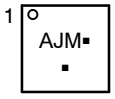


DFN8
MN SUFFIX
CASE 506AA

MARKING DIAGRAMS



N5901 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

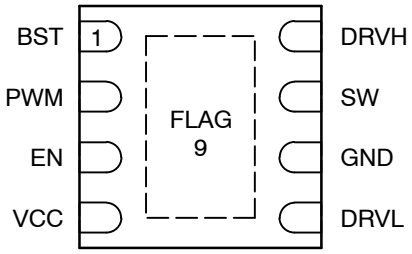


AJ = Specific Device Code
M = Date Code
▪ = Pb−Free Device

ORDERING INFORMATION

Device	Package	Shipping†
NCP5901MNTBG	DFN8 (Pb−Free)	3000 / Tape & Reel
NCP5901DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



(Top View)

Figure 1. Pin Diagram

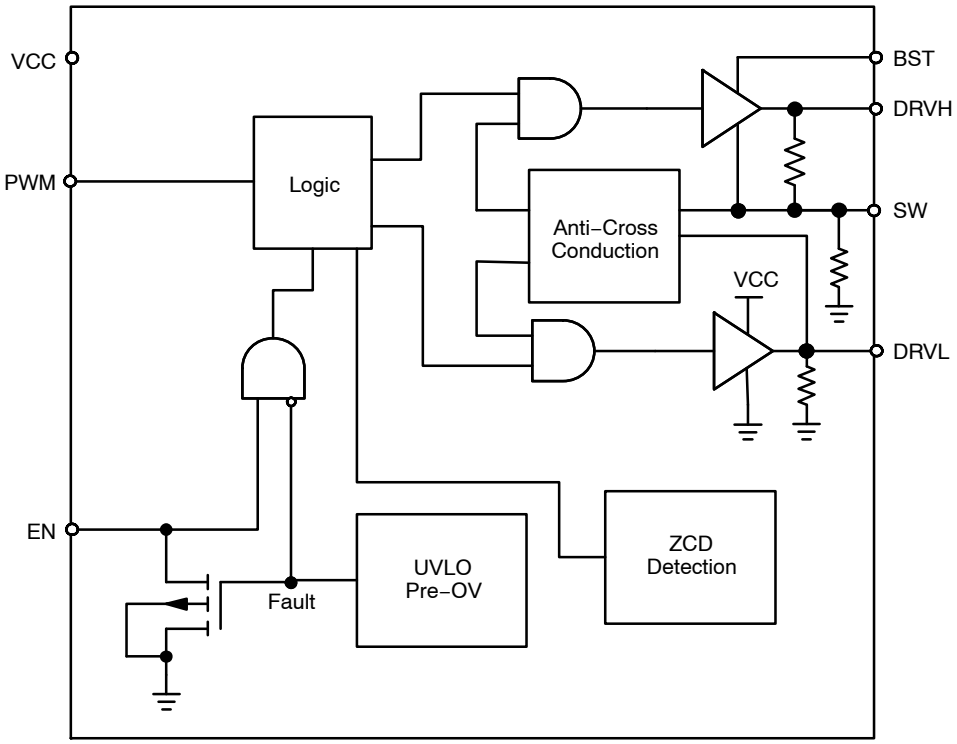


Figure 2. Block Diagram

Table 1. Pin Descriptions

Pin No.	Symbol	Description
1	BST	Floating bootstrap supply pin for high side gate driver. Connect the bootstrap capacitor between this pin and the SW pin.
2	PWM	Control input. The PWM signal has three distinctive states: Low = Low Side FET Enabled, Mid = Diode Emulation Enabled, High = High Side FET Enabled.
3	EN	Logic input. A logic high to enable the part and a logic low to disable the part.
4	VCC	Power supply input. Connect a bypass capacitor (0.1 μF) from this pin to ground.
5	DRVL	Low side gate drive output. Connect to the gate of low side MOSFET.
6	GND	Bias and reference ground. All signals are referenced to this node (QFN Flag).
7	SW	Switch node. Connect this pin to the source of the high side MOSFET and drain of the low side MOSFET.
8	DRVH	High side gate drive output. Connect to the gate of high side MOSFET.
9	FLAG	Thermal flag. There is no electrical connection to the IC. Connect to ground plane.

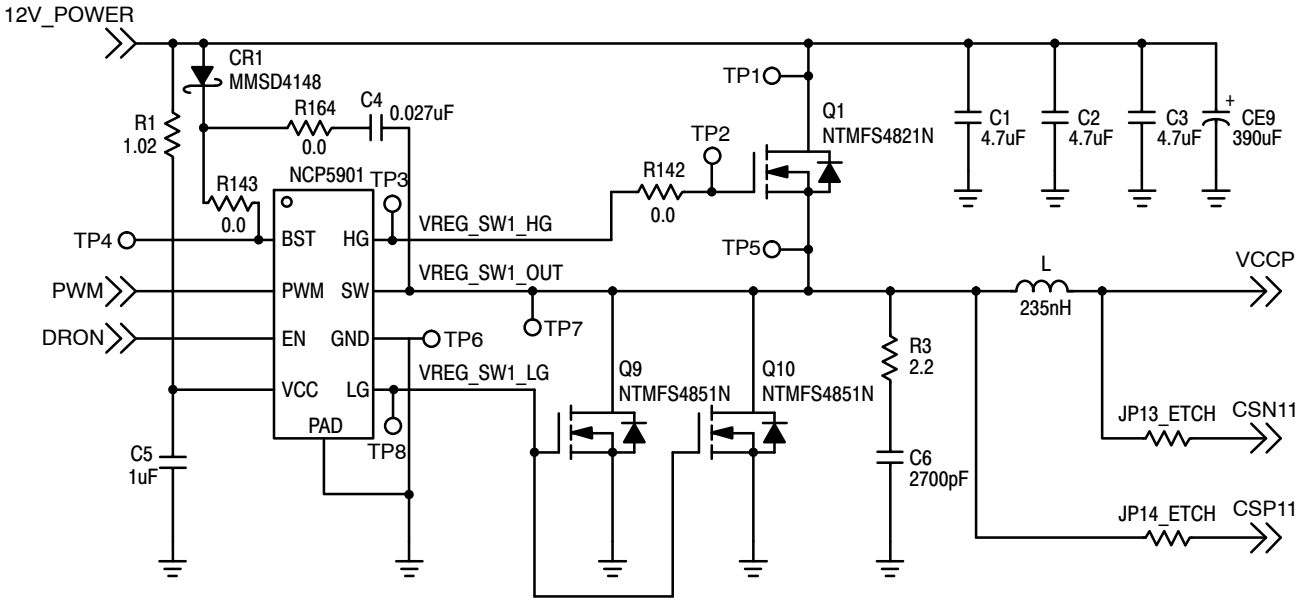


Figure 3. Application Circuit

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}
VCC	Main Supply Voltage Input	15 V	−0.3 V
BST	Bootstrap Supply Voltage	35 V wrt/ GND 40 V ≤ 50 ns wrt/ GND 15 V wrt/ SW	−0.3 V wrt/SW
SW	Switching Node (Bootstrap Supply Return)	35 V 40 V ≤ 50 ns	−5 V −10 V (200 ns)
DRVH	High Side Driver Output	BST+0.3 V	−0.3 V wrt/SW −2 V (<200 ns) wrt/SW
DRVL	Low Side Driver Output	VCC+0.3 V	−0.3 V DC −5 V (<200 ns)
PWM	DRVH and DRVL Control Input	6.5 V	−0.3 V
EN	Enable Pin	6.5 V	−0.3 V
GND	Ground	0 V	0 V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. THERMAL INFORMATION (All signals referenced to AGND unless noted otherwise)

Symbol	Parameter		Value	Unit
$R_{\theta JA}$	Thermal Characteristic	SOIC Package (Note 1) DFN Package (Note 1)	123 74	°C/W
T_J	Operating Junction Temperature Range (Note 2)		0 to 150	°C
T_A	Operating Ambient Temperature Range		−10 to +125	°C
T_{STG}	Maximum Storage Temperature Range		−55 to +150	°C
MSL	Moisture Sensitivity Level	SOIC Package DFN Package	1 1	

***** The maximum package power dissipation must be observed.
1. I in^2 Cu, 1 oz thickness.
2. Operation at −40°C to −10°C guaranteed by design, not production tested.

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −10°C < T_A < +125°C; 4.5 V < V_{CC} < 13.2 V, 4.5 V < BST−SWN < 13.2 V, 4.5 V < BST < 30 V, 0 V < SWN < 21 V)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
SUPPLY VOLTAGE					
VCC Operation Voltage		4.5		13.2	V
Power ON Reset Threshold			2.75	3.2	V
UNDERVOLTAGE LOCKOUT					
VCC Start Threshold		3.8	4.35	4.5	V
VCC UVLO Hysteresis		150	200	250	mV
Output Overvoltage Trip Threshold at Startup	Power Startup time, VCC > POR	2.1	2.25	2.4	V
SUPPLY CURRENT					
Normal Mode	Icc + Ibst, EN = 5 V, PWM = OSC, Fsw = 100 KHz, Cload = 3 nF for DRVH, 3 nF for DRVL		12.2		mA
Standby Current	Icc + Ibst, EN = GND		0.5	1.9	mA
Standby Current	I_{CC} + I_{BST}, EN = HIGH, PWM = LOW, No loading on DRVH & DRVL		2.1		mA
Standby Current	I_{CC} + I_{BST}, EN = HIGH, PWM = HIGH, No loading on DRVH & DRVL		2.2		mA
PWM INPUT					
PWM Input High		3.4			V
PWM Mid−State		1.3		2.7	V
PWM Input Low				0.7	V
ZCD Blanking Timer			250		ns
HIGH SIDE DRIVER (VCC = 12 V)					
Output Impedance, Sourcing Current	VBST − VSW = 12 V		2.0	3.5	Ω
Output Impedance, Sinking Current	VBST − VSW = 12 V		1.0	2.0	Ω
DRVH Rise Time tr_{DRVH}	V_{VCC} = 12 V, 3 nF load, VBST−VSW = 12 V		16	30	ns
DRVH Fall Time tf_{DRVH}	V_{VCC} = 12 V, 3 nF load, VBST−VSW = 12 V		11	25	ns
DRVH Turn−Off Propagation Delay $tpdh_{DRVH}$	C_{LOAD} = 3 nF	8.0		30	ns
DRVH Turn−On Propagation Delay $tpdl_{DRVH}$	C_{LOAD} = 3 nF			30	ns
SW Pull Down Resistance	SW to PGND		45		kΩ
DRVH Pull Down Resistance	DRVH to SW, BST−SW = 0 V		45		kΩ
HIGH SIDE DRIVER (VCC = 5 V)					
Output Impedance, Sourcing Current	VBST − VSW = 5 V		4.5		Ω
Output Impedance, Sinking Current	VBST − VSW = 5 V		2.9		Ω
DRVH Rise Time tr_{DRVH}	V_{VCC} = 5 V, 3 nF load, VBST − VSW = 5 V		30		ns
DRVH Fall Time tf_{DRVH}	V_{VCC} = 5 V, 3 nF load, VBST − VSW = 5 V		27		ns
DRVH Turn−Off Propagation Delay $tpdh_{DRVH}$	C_{LOAD} = 3 nF		20		ns
DRVH Turn−On Propagation Delay $tpdl_{DRVH}$	C_{LOAD} = 3 nF		27		ns
SW Pull Down Resistance	SW to PGND		45		kΩ
DRVH Pull Down Resistance	DRVH to SW, BST−SW = 0 V		45		kΩ

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −10°C < T_A < +125°C; 4.5 V < V_{CC} < 13.2 V, 4.5 V < BST−SWN < 13.2 V, 4.5 V < BST < 30 V, 0 V < SWN < 21 V)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
LOW SIDE DRIVER (VCC = 12 V)					
Output Impedance, Sourcing Current			2.0	3.5	Ω
Output Impedance, Sinking Current			0.8	1.8	Ω
DRVL Rise Time tr_{DRVL}	C_{LOAD} = 3 nF		16	35	ns
DRVL Fall Time tf_{DRVL}	C_{LOAD} = 3 nF		11	20	ns
DRVL Turn−Off Propagation Delay $tpdl_{DRVL}$	C_{LOAD} = 3 nF			35	ns
DRVL Turn−On Propagation Delay $tpdh_{DRVL}$	C_{LOAD} = 3 nF	8.0		30	ns
DRVL Pull Down Resistance	DRVL to PGND, VCC = PGND		45		kΩ
LOW SIDE DRIVER (VCC = 5 V)					
Output Impedance, Sourcing Current			4.5		Ω
Output Impedance, Sinking Current			2.4		Ω
DRVL Rise Time tr_{DRVL}	C_{LOAD} = 3 nF		30		ns
DRVL Fall Time tf_{DRVL}	C_{LOAD} = 3 nF		22		ns
DRVL Turn−Off Propagation Delay $tpdl_{DRVL}$	C_{LOAD} = 3 nF		27		ns
DRVL Turn−On Propagation Delay $tpdh_{DRVL}$	C_{LOAD} = 3 nF		12		ns
DRVL Pull Down Resistance	DRVL to PGND, VCC = PGND		45		kΩ
EN INPUT					
Input Voltage High		2.0			V
Input Voltage Low				1.0	V
Hysteresis			500		mV
Normal Mode Bias Current		−1		1	μA
Enable Pin Sink Current		4		30	mA
Propagation Delay Time			20	40	ns
SW Node					
SW Node Leakage Current				20	μA
Zero Cross Detection Threshold Voltage	SW to −20 mV, ramp slowly until BG goes off (Start in DCM mode) (Note 3)		−6		mV

Table 5. DECODER TRUTH TABLE

PWM INPUT	ZCD	DRVL	DRVH
PWM High	ZCD Reset	Low	High
PWM Mid	Positive current through the inductor	High	Low
PWM Mid	Zero current through the inductor	Low	Low
PWM Low	ZCD Reset	High	Low

3. Guaranteed by design; not production tested.

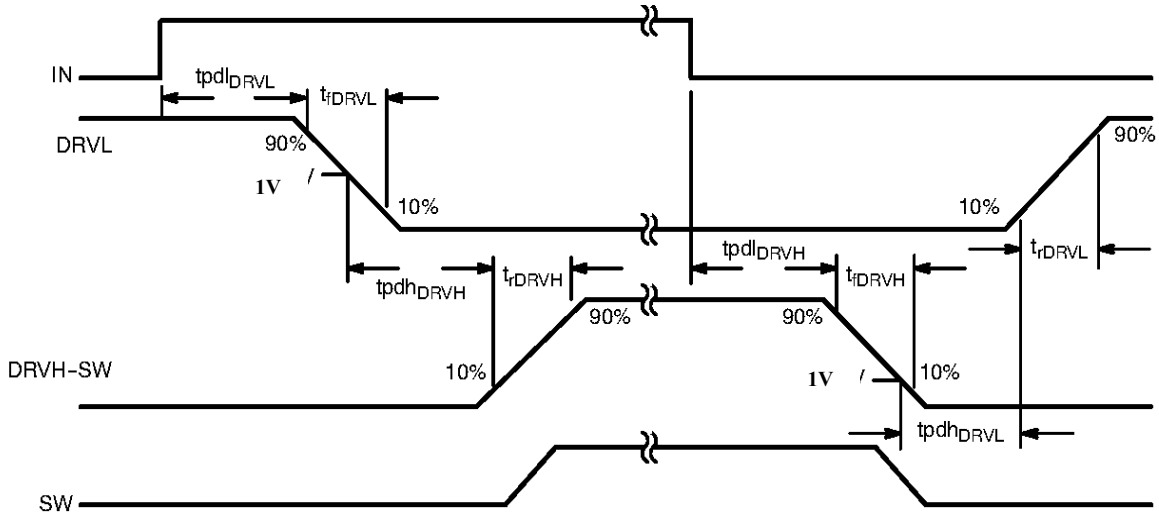


Figure 4.

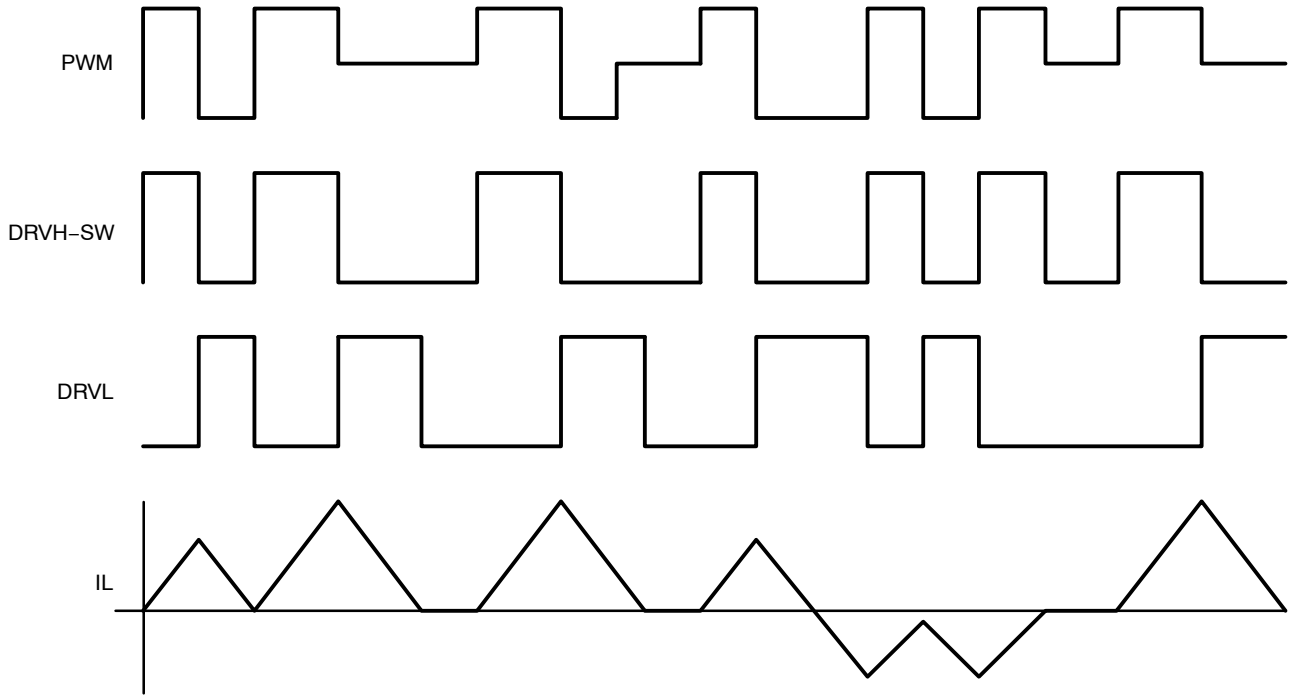


Figure 5. Timing Diagram

APPLICATIONS INFORMATION

The NCP5901 gate driver is a single phase MOSFET driver designed for driving N−channel MOSFETs in a synchronous buck converter topology. The NCP5901 is designed to work with ON Semiconductor's NCP6131 multi−phase controller. This gate driver is optimized for desktop applications.

Undervoltage Lockout

The DRVH and DRVL are held low until V_{CC} reaches 4.5 V during startup. The PWM signals will control the gate status when V_{CC} threshold is exceeded. If V_{CC} decreases to 250 mV below the threshold, the output gate will be forced low until input voltage V_{CC} rises above the startup threshold.

Power−On Reset

Power−On Reset feature is used to protect a gate driver avoid abnormal status driving the startup condition. When the initial soft−start voltage is higher than 2.75 V, the gate driver will monitor the switching node SW pin. If SW pin high than 2.25 V, bottom gate will be force to high for discharge the output capacitor. The fault mode will be latch and EN pin will force to be low, unless the driver is recycle. When input voltage is higher than 4.5 V, and EN goes high, the gate driver will normal operation, top gate driver DRVH and bottom gate driver will follow the PWM signal decode to a status.

Bi−directional EN Signal

Fault modes such as Power−On Reset and Undervoltage Lockout will de−assert the EN pin, which will pull down the DRON pin of controller as well. Thus the controller will be shut down consequently.

PWM Input and Zero Cross Detect (ZCD)

The PWM input, along with EN and ZCD, control the state of DRVH and DRVL.

When PWM is set high, DRVH will be set high after the adaptive non−overlap delay. When PWM is set low, DRVL will be set high after the adaptive non−overlap delay.

When the PWM is set to the mid state, DRVH will be set low, and after the adaptive non−overlap delay, DRVL will be set high. DRVL remains high during the ZCD blanking time. When the timer is expired, the SW pin will be monitored for zero cross detection. After the detection, the DRVL will be set low.

Adaptive Nonoverlap

The nonoverlap dead time control is used to avoid the shoot through damage the power MOSFETs. When the PWM signal pull high, DRVL will go low after a propagation delay, the controller will monitors the switching node (SWN) pin voltage and the gate voltage of the MOSFET to know the status of the MOSFET. When the low side MOSFET status is off an internal timer will delay turn on of the high–side MOSFET. When the PWM pull low, gate DRVH will go low after the propagation delay (tpd $_{DRVH}$).

The time to turn off the high side MOSFET is depending on the total gate charge of the high−side MOSFET. A timer will be triggered once the high side MOSFET is turn off to delay the turn on the low−side MOSFET.

Low−Side Driver Timeout

In normal operation, the DRVH signal tracks the PWM signal and turns off the Q1 high−side switch with a few 10 ns delay ($t_{pdlDRVH}$) following the falling edge of the input signal. When Q1is turned off, DRVL is allowed to go high, Q2 turns on, and the SW node voltage collapses to zero. But in a fault condition such as a high−side Q1 switch drain−source short circuit, the SW node cannot fall to zero, even when DRVH goes low. This driver has a timer circuit to address this scenario. Every time the PWM goes low, a DRVL on−time delay timer is triggered.

If the SW node voltage does not trigger a low−side turn−on, the DRVL on−time delay circuit does it instead, when it times out with $t_{SW(TO)}$ delay. If Q1 is still turned on, that is, its drain is shorted to the source, Q2 turns on and creates a direct short circuit across the VDCIN voltage rail. The crowbar action causes the fuse in the VDCIN current path to open. The opening of the fuse saves the load (CPU) from potential damage that the high−side switch short circuit could have caused.

Layout Guidelines

Layout for DC−DC converter is very important. The bootstrap and V_{CC} bypass capacitors should be placed as close as to the driver IC.

Connect GND pin to local ground plane. The ground plane can provide a good return path for gate drives and reduce the ground noise. The thermal slug should be tied to the ground plane for good heat dissipation. To minimize the ground loop for low side MOSFET, the driver GND pin should be close to the low−side MOSFET source pin. The gate drive trace should be routed to minimize the length, the minimum width is 20 mils.

Gate Driver Power Loss Calculation

The gate driver power loss consists of the gate drive loss and quiescent power loss.

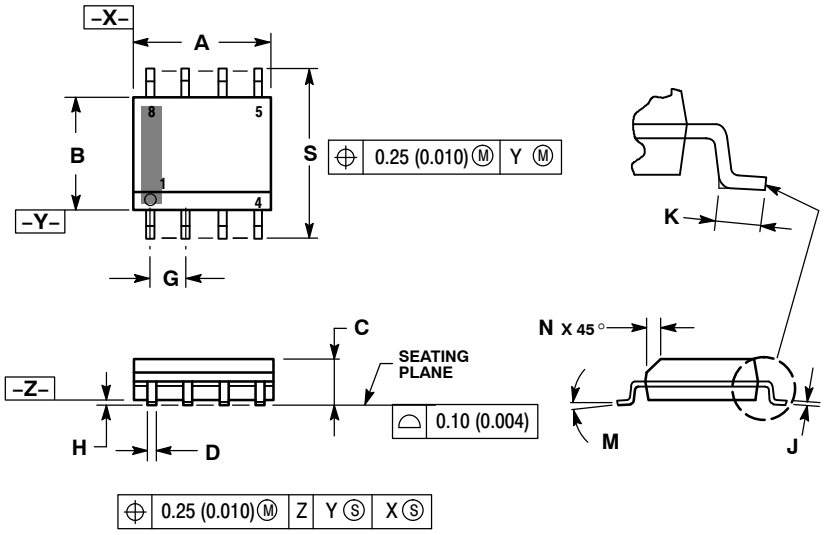
The equation below can be used to calculate the power dissipation of the gate driver. Where Q_{GMF} is the total gate charge for each main MOSFET and Q_{GSF} is the total gate charge for each synchronous MOSFET.

$$P_{DRV} = [\frac{f_{SW}}{2 \times n} \times (n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF}) + I_{CC}] \times V_{CC}$$

Also shown is the standby dissipation factor ($I_{CC} \cdot V_{CC}$) of the driver.

PACKAGE DIMENSIONS

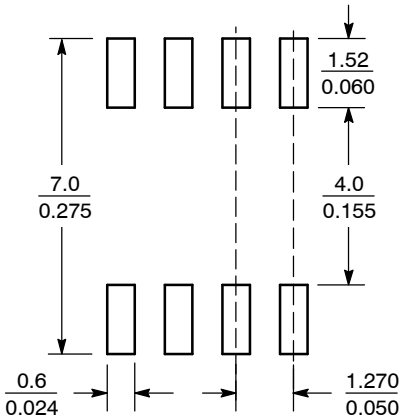
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

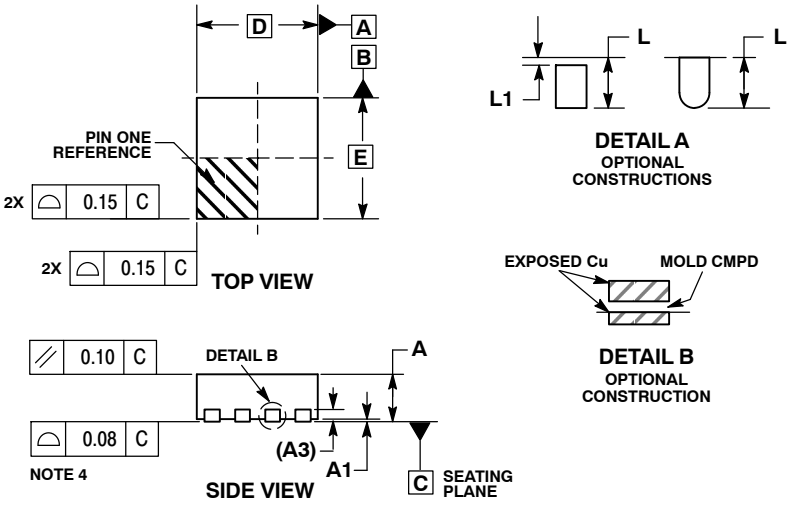


SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

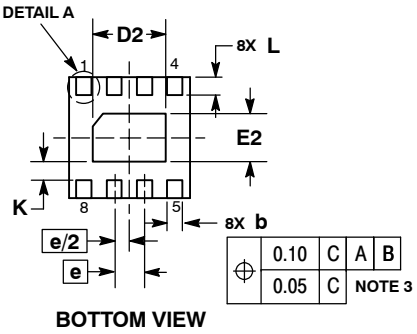
PACKAGE DIMENSIONS

DFN8 2x2
CASE 506AA
ISSUE E

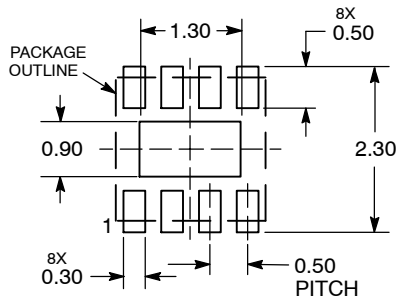


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.30 REF	
L	0.25	0.35
L1	---	0.10



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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Email: orderlit@onsemi.com

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