

- **EPIC™ (Enhanced-Performance Implanted CMOS) 2- μ Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model**
($C = 200$ pF, $R = 0$)
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) 300-mil DIPs**

description

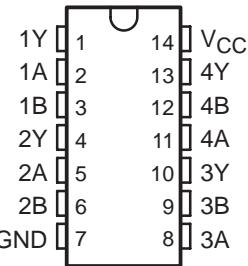
These quadruple 2-input positive-NOR gates are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV02 perform Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

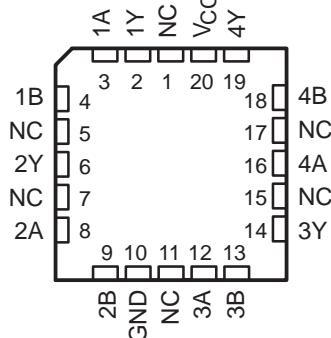
The SN74LV02 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LV02 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV02 is characterized for operation from -40°C to 85°C .

SN54LV02 . . . J OR W PACKAGE
SN74LV02 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H



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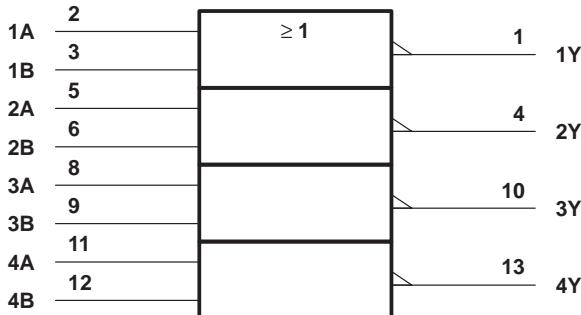


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SN54LV02, SN74LV02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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logic symbol†



logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, DB, J, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range, T_{stg}	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. This value is limited to 7 V maximum.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

SN54LV02, SN74LV02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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recommended operating conditions (see Note 4)

				SN54LV02	SN74LV02	UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	5.5	2.7	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2	2	2	V
		V _{CC} = 4.5 V to 5.5 V	3.15	3.15	3.15	
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V	0.8	0.8	0.8	V
		V _{CC} = 4.5 V to 5.5 V	1.65	1.65	1.65	
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V to 3.6 V	-6	-6	-6	mA
		V _{CC} = 4.5 V to 5.5 V	-12	-12	-12	
I _{OL}	Low-level output current	V _{CC} = 2.7 V to 3.6 V	6	6	6	mA
		V _{CC} = 4.5 V to 5.5 V	12	12	12	
Δt/Δv	Input transition rise or fall rate	0	100	0	100	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	SN54LV02			SN74LV02			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} – 0.2			V _{CC} – 0.2			V	
	I _{OH} = -6 mA	3 V	2.4			2.4				
	I _{OH} = -12 mA	4.5 V	3.6			3.6				
V _{OL}	I _{OL} = 100 μA	MIN to MAX	0.2			0.2			V	
	I _{OL} = 6 mA	3 V	0.4			0.4				
	I _{OL} = 12 mA	4.5 V	0.55			0.55				
I _I	V _I = V _{CC} or GND	3.6 V	±1			±1			μA	
		5.5 V	±1			±1				
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	20			20			μA	
		5.5 V	20			20				
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	500			500			μA	
C _I	V _I = V _{CC} or GND	3.3 V	2.5			2.5			pF	
		5 V	2.5			2.5				

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV02						UNIT	
			V _{CC} = 5 V ± 0.5 V			V _{CC} = 3.3 V ± 0.3 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
t _{pd}	A	Y	5	10	10	8	13	16	ns	

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SN54LV02, SN74LV02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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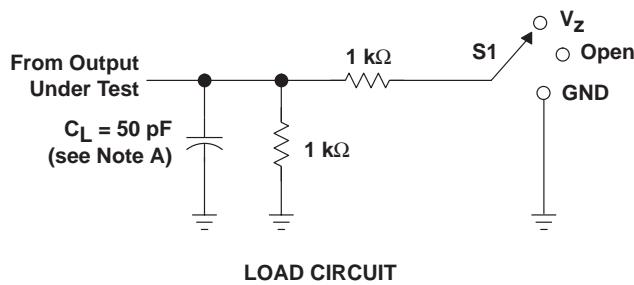
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV02						UNIT	
			V _{CC} = 5 V ± 0.5 V			V _{CC} = 3.3 V ± 0.3 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
t_{pd}	A	Y	5	10		8	13	16	ns	

operating characteristics, $T_A = 25^\circ\text{C}$

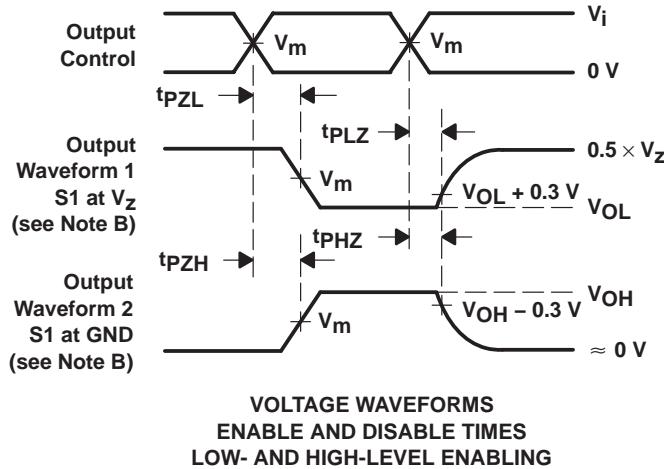
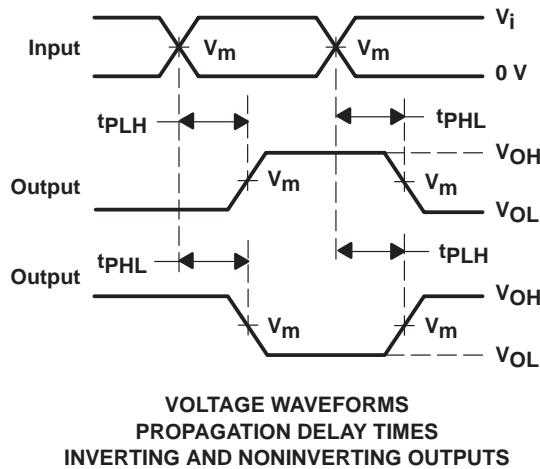
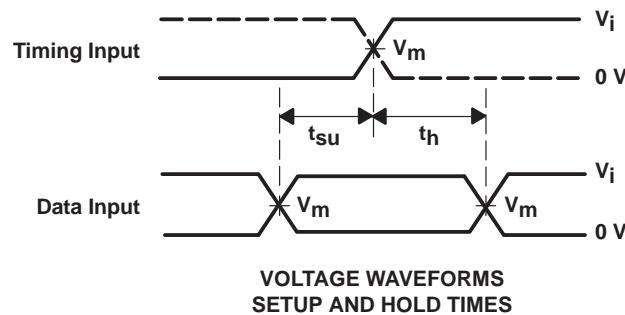
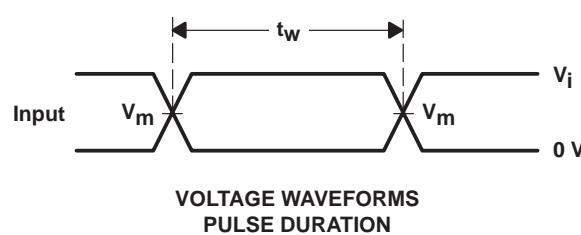
PARAMETER	TEST CONDITIONS	V _{CC}	TYP	UNIT
		3.3 V	16	pF
		5 V	20	
C_{pd} Power dissipation capacitance per gate	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$			

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_Z
t_{PHZ}/t_{PZH}	GND

WAVEFORM CONDITION	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	$V_{CC} = 2.7 \text{ V}$ to 3.6 V
V_m	$0.5 \times V_{CC}$	1.5 V
V_i	V_{CC}	2.7 V
V_Z	$2 \times V_{CC}$	6 V



NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_f \leq 2.5 \text{ ns}$, $t_r \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LV02D	OBsolete	SOIC	D	14		TBD	Call TI	Call TI
SN74LV02DBLE	OBsolete	SSOP	DB	14		TBD	Call TI	Call TI
SN74LV02DR	OBsolete	SOIC	D	14		TBD	Call TI	Call TI
SN74LV02PWLE	OBsolete	TSSOP	PW	14		TBD	Call TI	Call TI
SN74LV02PWR	OBsolete	TSSOP	PW	14		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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