

SN54LV02, SN74LV02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS183B – FEBRUARY 1993 – REVISED APRIL 1996

- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) 300-mil DIPs**

description

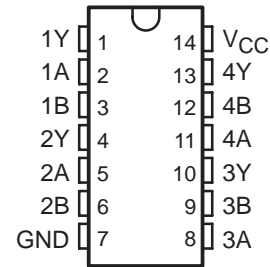
These quadruple 2-input positive-NOR gates are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV02 perform Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

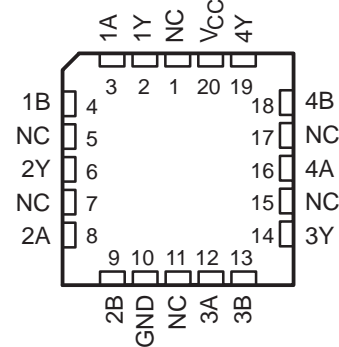
The SN74LV02 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LV02 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV02 is characterized for operation from -40°C to 85°C .

SN54LV02 . . . J OR W PACKAGE
SN74LV02 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | L |
| X | H | L |
| L | L | H |



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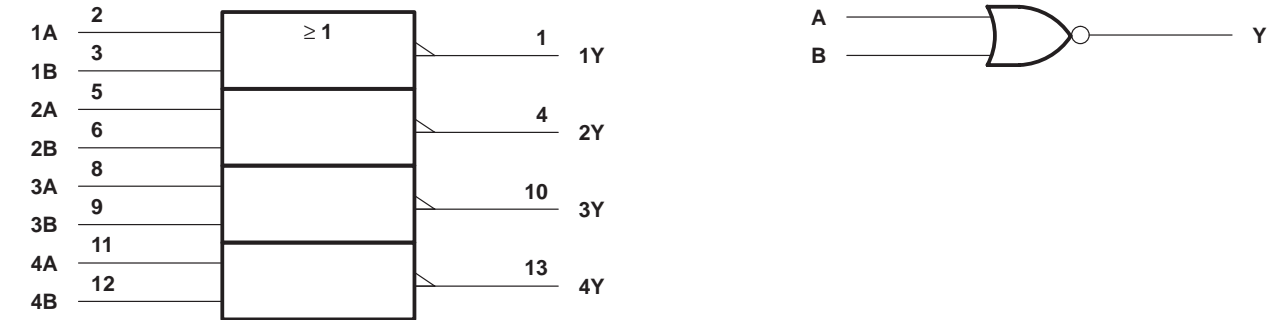
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SN54LV02, SN74LV02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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logic symbol†

logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, DB, J, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|--|--|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, V_O (see Notes 1 and 2) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ± 50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 25 mA |
| Continuous current through V_{CC} or GND | ± 50 mA |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): D package | 1.25 W |
| DB or PW package | 0.5 W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

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recommended operating conditions (see Note 4)

| | | | SN54LV02 | | SN74LV02 | | UNIT |
|---------------------|------------------------------------|---|----------|----------|----------|----------|------|
| | | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | | 2.7 | 5.5 | 2.7 | 5.5 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 2 | | 2 | | V |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 3.15 | | 3.15 | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | | 0.8 | | 0.8 | V |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | 1.65 | | 1.65 | |
| V_I | Input voltage | | 0 | V_{CC} | 0 | V_{CC} | V |
| V_O | Output voltage | | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | | -6 | | -6 | mA |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | -12 | | -12 | |
| I_{OL} | Low-level output current | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | | 6 | | 6 | mA |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | 12 | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 0 | 100 | 0 | 100 | ns/V |
| T_A | Operating free-air temperature | | -55 | 125 | -40 | 85 | °C |

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} [†] | SN54LV02 | | | SN74LV02 | | | UNIT |
|------------------|---|------------------------------|-----------------------|-----|-----|-----------------------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{OH} | I _{OH} = −100 μA | MIN to MAX | V _{CC} − 0.2 | | | V _{CC} − 0.2 | | | V |
| | I _{OH} = −6 mA | 3 V | 2.4 | | | 2.4 | | | |
| | I _{OH} = −12 mA | 4.5 V | 3.6 | | | 3.6 | | | |
| V _{OL} | I _{OL} = 100 μA | MIN to MAX | 0.2 | | | 0.2 | | | V |
| | I _{OL} = 6 mA | 3 V | 0.4 | | | 0.4 | | | |
| | I _{OL} = 12 mA | 4.5 V | 0.55 | | | 0.55 | | | |
| I _I | V _I = V _{CC} or GND | 3.6 V | ±1 | | | ±1 | | | μA |
| | | 5.5 V | ±1 | | | ±1 | | | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | 20 | | | 20 | | | μA |
| | | 5.5 V | 20 | | | 20 | | | |
| ΔI _{CC} | One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND | 3 V to 3.6 V | 500 | | | 500 | | | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | 2.5 | | | 2.5 | | | pF |
| | | 5 V | 2.5 | | | 2.5 | | | |

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LV02 | | | | | | UNIT | | |
|-----------------|-----------------|----------------|-------------------------------|-----|-----|---------------------------------|-----|-----|------|-------------------------|-----|
| | | | V _{CC} = 5 V ± 0.5 V | | | V _{CC} = 3.3 V ± 0.3 V | | | | V _{CC} = 2.7 V | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | MIN | MAX |
| t _{pd} | A | Y | | 5 | 10 | | 8 | 13 | | 16 | ns |

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LV02 | | | | | | | | UNIT |
|-----------------|-----------------|----------------|-------------------------------|-----|-----|---------------------------------|-----|-----|-------------------------|-----|------|
| | | | V _{CC} = 5 V ± 0.5 V | | | V _{CC} = 3.3 V ± 0.3 V | | | V _{CC} = 2.7 V | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | MAX | |
| t _{pd} | A | Y | 510 | | | 813 | | | 16 | | ns |

operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | V_{CC} | TYP | UNIT |
|-----------|--|-----------------------------|----------|-----|------|
| C_{pd} | Power dissipation capacitance per gate | $C_L = 50$ pF, $f = 10$ MHz | 3.3 V | 16 | pF |
| | | | 5 V | 20 | |



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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LV02D | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI |
| SN74LV02DBLE | OBSOLETE | SSOP | DB | 14 | | TBD | Call TI | Call TI |
| SN74LV02DR | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI |
| SN74LV02PWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI |
| SN74LV02PWR | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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