

P-channel 20 V, 0.087 Ω typ., 3 A STripFET™ H7 Power MOSFET in a SOT23-6L package

Datasheet - production data

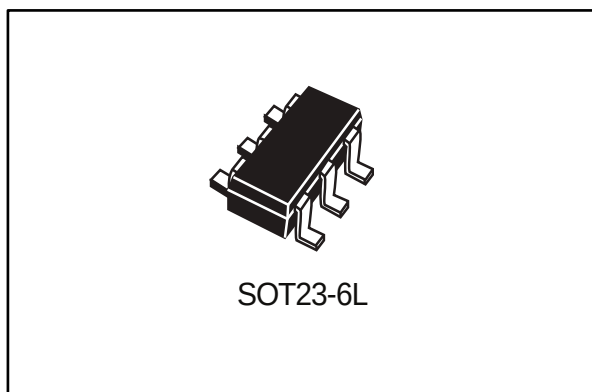
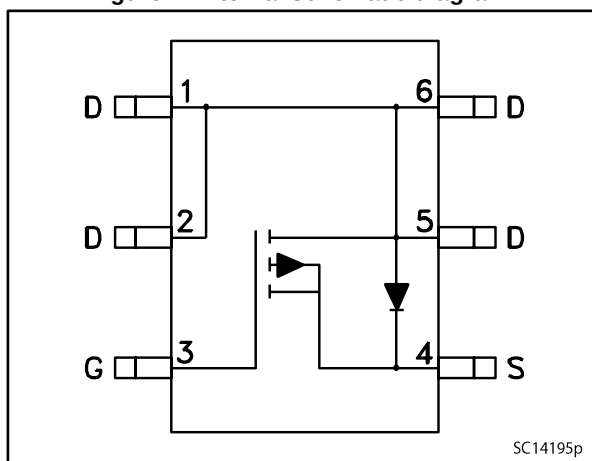


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STT3P2UH7	20 V	0.1 Ω @ 4.5	3 A

- Very low on-resistance
- Very low capacitance and gate charge
- High avalanche ruggedness

Applications

- Switching applications

Description

This P-channel Power MOSFET utilizes the STripFET H7 technology with a trench gate structure combined with extremely low on-resistance. The device also offers ultra-low capacitances for higher switching frequency operations.

Table 1: Device summary

Order code	Marking	Package	Packaging
STT3P2UH7	3L2U	SOT23-6L	Tape and reel



For the P-channel Power MOSFET, current and voltage polarities are reversed.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	20	V
V_{GS}	Gate-source voltage	± 8	V
I_D	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	3	A
I_D	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	1.9	A
$I_{DM}^{(1)}$	Drain current (pulsed)	12	A
P_{TOT}	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	1.6	W
T_{stg}	Storage temperature range	- 55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max, single operation	78	$^{\circ}\text{C/W}$

Notes:

⁽¹⁾When mounted on 1inch² FR-4 board, 2 oz Cu



For the P-channel Power MOSFET, current and voltage polarities are reversed.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250 μA, V _{GS} = 0	20			V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 20 V, V _{GS} = 0			1	μA
I _{GSS}	Gate-body leakage current	V _{GS} = ± 8 V, V _{DS} = 0			10	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.4		1	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 4.5 V, I _D = 1.5 A		0.087	0.1	Ω
		V _{GS} = 2.5 V, I _D = 1.5 A		0.11	0.13	Ω
		V _{GS} = 1.8 V, I _D = 1.5 A		0.145	0.18	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 10 V, f = 1 MHz, V _{GS} = 0	-	510	-	pF
C _{oss}	Output capacitance		-	66	-	pF
C _{rss}	Reverse transfer capacitance		-	44	-	pF
Q _g	Total gate charge	V _{DD} = 10 V, I _D = 3 A, V _{GS} = 4.5 V (see Figure 14: "Gate charge test circuit")	-	4.8	-	nC
Q _{gs}	Gate-source charge		-	0.7	-	nC
Q _{gd}	Gate-drain charge		-	0.8	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 10 V, I _D = 1.5 A, R _G = 4.7 Ω, V _{GS} = 4.5 V (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	9	-	ns
t _r	Rise time		-	21	-	ns
t _{d(off)}	Turn-off delay time		-	40	-	ns
t _f	Fall time		-	19	-	ns



For the P-channel Power MOSFET, current and voltage polarities are reversed.

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 1\text{ A}$, $V_{GS} = 0$	-	-	1	V
t_{rr}	Reverse recovery time	$V_{DD} = 10\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $I_{SD} = 1\text{ A}$ $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	12.5		ns
Q_{rr}	Reverse recovery charge		-	5		nC
I_{RRM}	Reverse recovery current		-	0.8		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%.



For the P-channel Power MOSFET, current and voltage polarities are reversed.

2.1 Electrical characteristics (curves)



For the P-channel Power MOSFET, current and voltage polarities are reversed.

Figure 2: Safe operating area

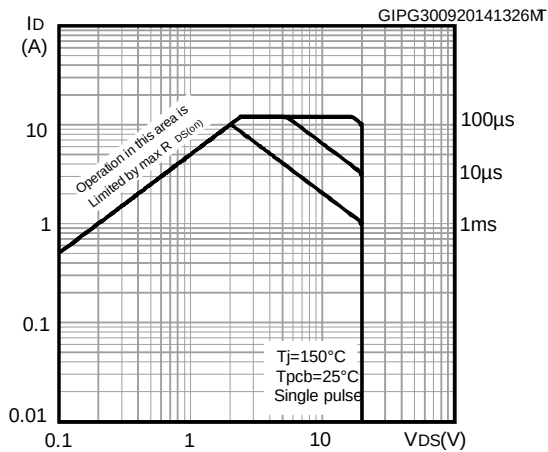


Figure 3: Thermal impedance

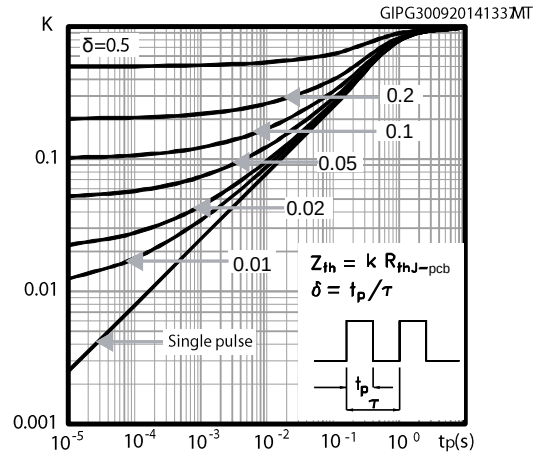


Figure 4: Output characteristics

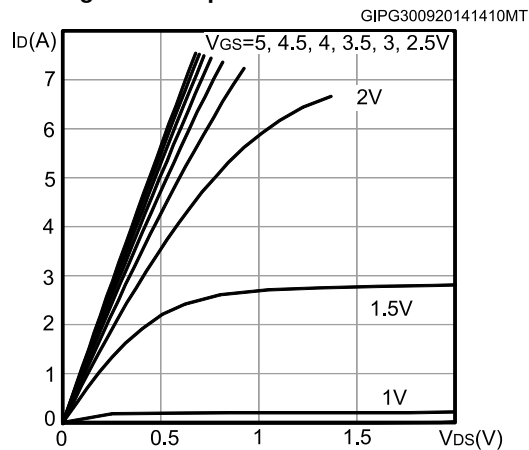


Figure 5: Transfer characteristics

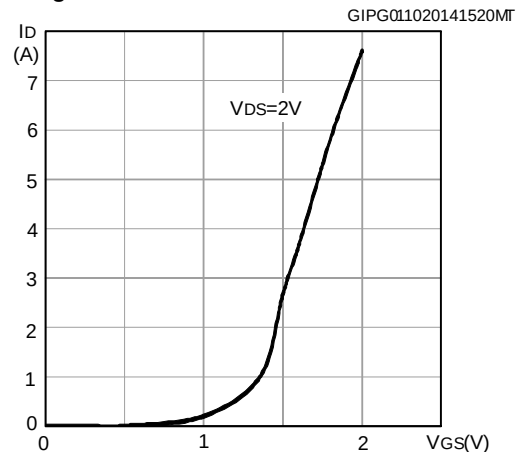


Figure 6: Gate charge vs gate-source voltage

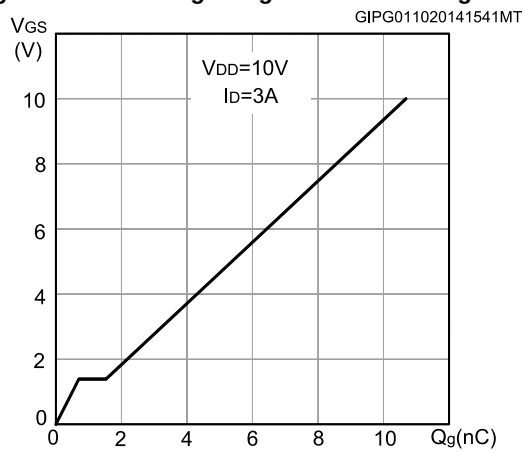


Figure 7: Static drain-source on-resistance

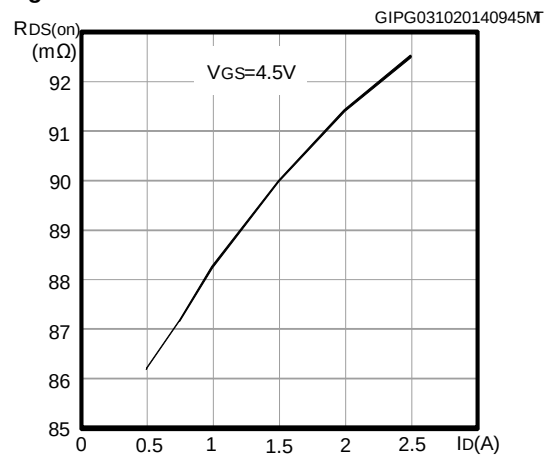


Figure 8: Capacitance variations

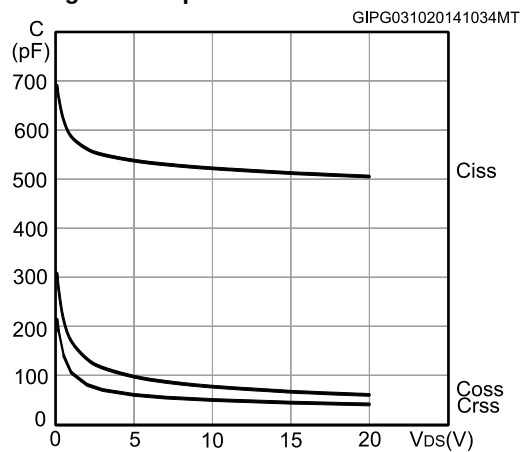


Figure 9: Normalized gate threshold voltage vs temperature

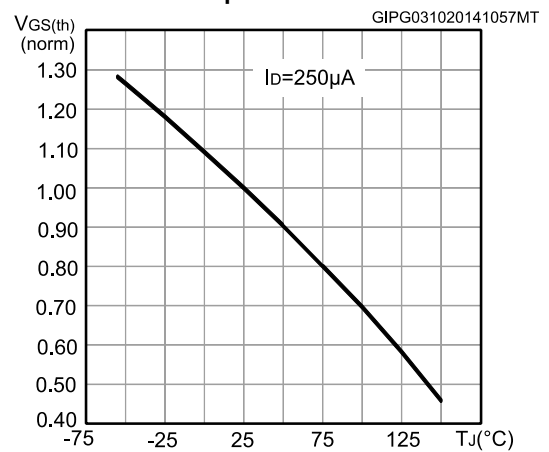


Figure 10: Normalized on-resistance vs temperature

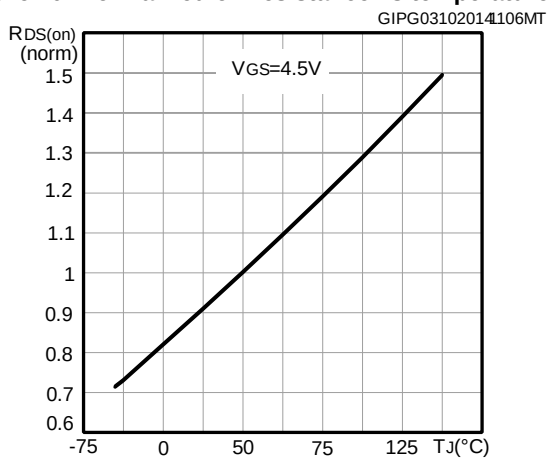


Figure 11: Normalized V(BR)DSS vs temperature

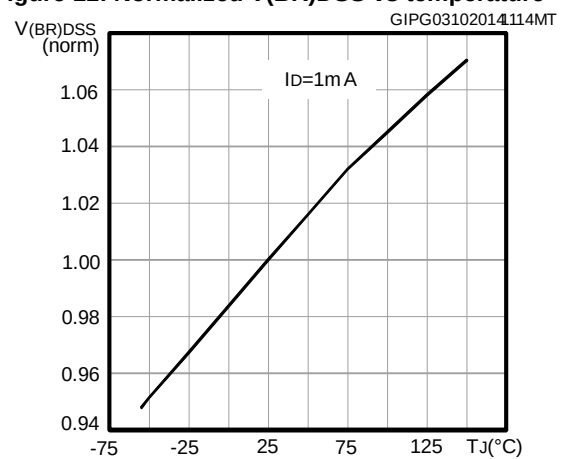
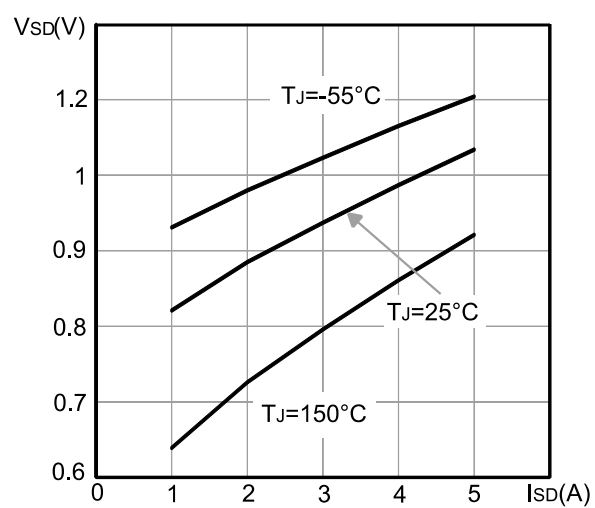


Figure 12: Source-drain diode forward characteristics

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3 Test circuits

Figure 13: Switching times test circuit for resistive load

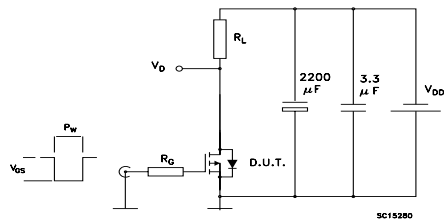


Figure 14: Gate charge test circuit

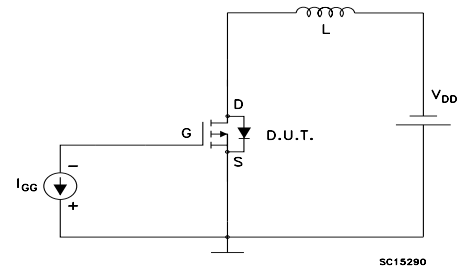
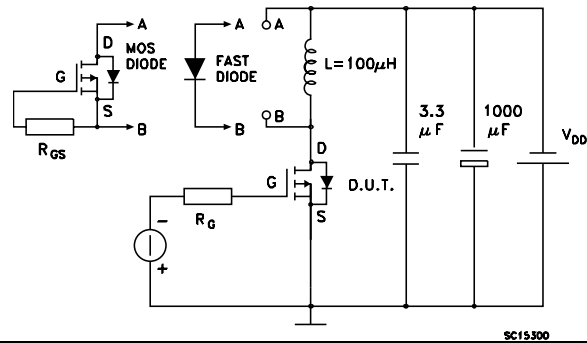


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 SOT23-6L package mechanical data

Figure 16: SOT23-6L package drawing

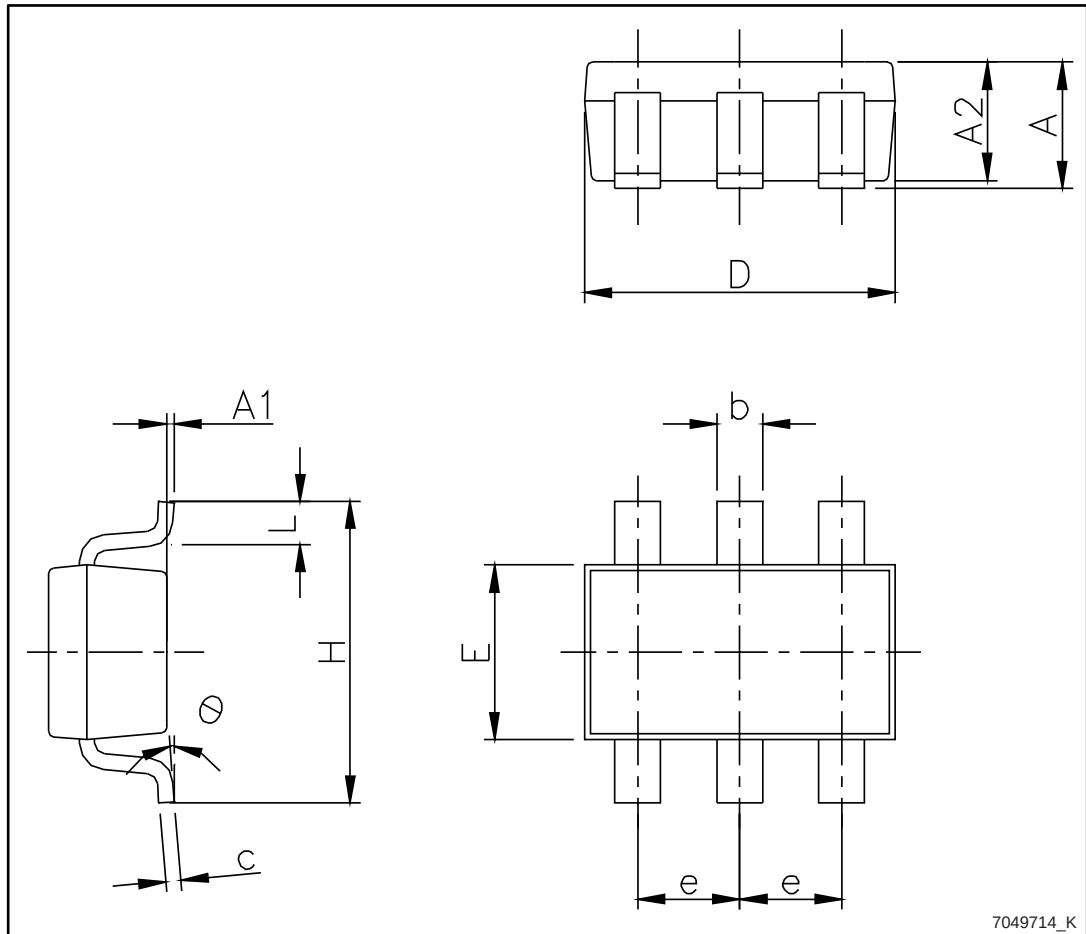
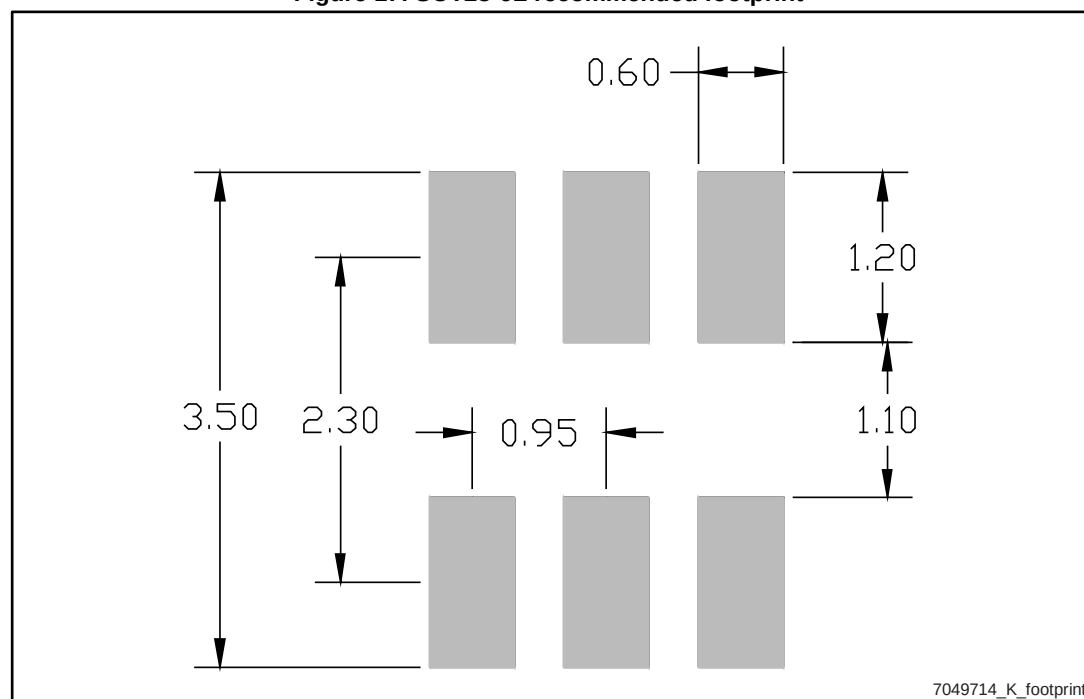


Table 8: SOT23-6L package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.25
A1	0.00		0.15
A2	1.00	1.10	1.20
b	0.36		0.50
C	0.14		0.20
D	2.826	2.926	3.026
E	1.526	1.626	1.726
e	0.90	0.95	1.00
H	2.60	2.80	3.00
L	0.35	0.45	0.60
θ	0°		8°

Figure 17: SOT23-6L recommended footprint



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
18-Jul-2013	1	First release.
03-Oct-2014	2	Document status promoted from target data to production data. Updated title, features and description in cover page. Updated <i>Section 2: "Electrical characteristics"</i> and <i>Section 4.1: "SOT23-6L package mechanical data"</i> . Minor text changes.
12-Sep-2016	3	Updated Table 2: "Absolute maximum ratings" . Minor text changes.

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