REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R106-96. – sbr	96-04-16	M. A. Frye
B	Changes in accordance with NOR 5962-R255-97. – drw	97-03-31	Raymond Monnin
C	Change the limit of bipolar zero error test, table I, sheet 5. Editorial changes throughout. - drw	01-09-20	Raymond Monnin

REV																				
SHEET																				
REV	C	C																		
SHEET	15	16																		

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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DRAWING APPROVAL DATE
96-03-27

REVISION LEVEL
C

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, LINEAR, 8-CHANNEL, 12-BIT SERIAL, DATA ACQUISITION SYSTEM, MONOLITHIC SILICON

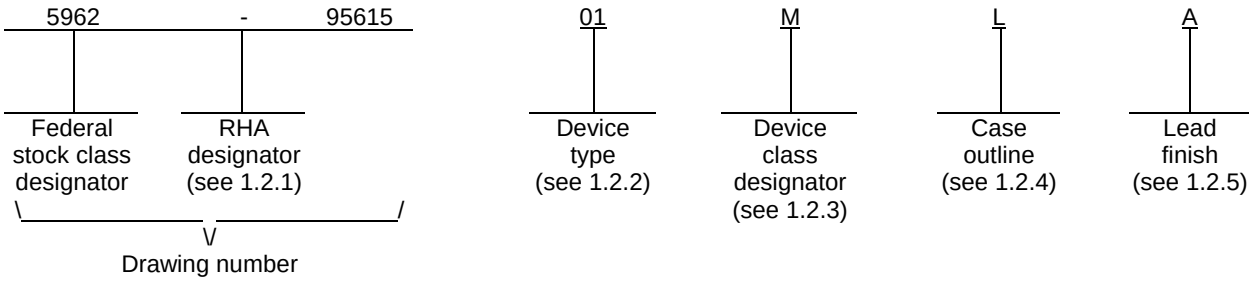
SIZE	CAGE CODE	
A	**67268**	**5962-95615**

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD7890-10	8-channel, 12-bit serial, data acquisition system

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

V_{DD} to AGND	-0.3 V dc to +7 V dc
V_{DD} to DGND	-0.3 V dc to +7 V dc
Analog input voltage to AGND	±17 V dc
Reference input voltage to AGND	-0.3 V dc to V_{DD} + 0.3 V dc
Digital input voltage to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
Digital output voltage to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
Junction temperature (T_J)	+150°C
Power dissipation (P_D)	450 mW
Thermal resistance, junction-to-ambient (θ_{JA})	70°C/W
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Ambient operating temperature range	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Ideal input/output table. The ideal input/output table shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Signal to noise + distortion ratio	SNR	f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 100 kHz V_{DD} = +4.75 V dc	1, 2, 3	01	70		dB
Total harmonic distortion	THD	f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 100 kHz V_{DD} = +4.75 V dc	1, 2, 3	01		77	dB
Peak harmonic or spurious distortion	PHN	f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 100 kHz	1, 2, 3	01		78	dB
Channel-to-channel isolation	CI	f_{IN} = 10 kHz sine wave, V_{DD} = +4.75 V dc	1, 2, 3	01		80	dB
Resolution	RES		1, 2, 3	01		12	Bits
Minimum resolution for which no missing codes are guaranteed	MRES		1, 2, 3	01		12	Bits
Relative accuracy	RA		1, 2, 3	01		±1	LSB
Differential nonlinearity	DNL		1, 2, 3	01		±1	LSB
Positive full-scale error	PFSE		1, 2, 3	01		±2.5	LSB
Full-scale error match 2/	FSE		1, 2, 3	01		2	LSB
Negative full-scale error	NFSE	V_{DD} = +4.75 V dc	1, 2, 3	01		±2	LSB
Bipolar zero error	BZE		1, 2, 3	01		±5	LSB
Bipolar zero error match	BZEM		1, 2, 3	01		2	LSB
Input voltage range	V_{IN}		1, 2, 3	01	-10	+10	V
Input resistance	R_{IN}		1, 2, 3	01	20		kΩ
Mux out output voltage range	V_{OUT}		1, 2, 3	01	0	2.5	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Mux out output resistance	R_{OUT}		1, 2, 3	01	3	5	kΩ
SHA IN input voltage range	V_{SIN}		1, 2, 3	01	0	2.5	V
SHA IN input current	I_{SIN}	V_{SIN} = 2.49 V	1, 2, 3	01	-50	+50	nA
REF IN input voltage range	V_{RIN}		1, 2, 3	01	2.375	2.625	V
Input impedance	R_{RIN}	Resistor connected to internal reference node	1, 2, 3	01	1.6		kΩ
REF OUT voltage	V_{ROUT}		1	01	2.49	2.510	V
			2, 3		2.475	2.525	
Logic input high voltage	V_{INH}	V_{DD} = 5 V ±5%	1, 2, 3	01	2.4		V
Input low voltage	V_{INL}	V_{DD} = 5 V ±5%	1, 2, 3	01		0.8	V
Input current	I_{IN}	V_{IN} = 0 V to V_{DD}	1, 2, 3	01	-10	+10	µA
Output high voltage	V_{OH}	I_{SOURCE} = 200 µA, V_{DD} = 4.75 V	1, 2, 3	01	4		V
Output low voltage	V_{OL}	I_{SINK} = 1.6 mA, V_{DD} = 4.75 V	1, 2, 3	01		0.4	V
Conversion time 3/	t_{CONV}	f_{CLKIN} = 2.5 MHz, V_{DD} = 4.75 V, MUX OUT connected to SHA IN	9, 10, 11	01		5.9	µs
Supply voltage	V_{DD}	±5% for specified performance	1, 2, 3	01		5	V
Supply current 4/	I_{DD}	Logic inputs = 0 V or V_{DD}	1, 2, 3	01		10	mA
Power dissipation	P_D		1, 2, 3	01		50	mW

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/, 3/, 5/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Master clock frequency 6/	f_{CLKIN}		9, 10, 11	01	0.1	2.5	MHz
Master clock input low time	t_{CLKINL}		9, 10, 11	01	0.3 x t_{CLKIN}		ns
Master clock input high time	t_{CLKINH}		9, 10, 11	01	0.3 x t_{CLKIN}		ns
Digital output rise time 7/	t_R		9, 10, 11	01		25	ns
Digital output fall time 7/	t_F		9, 10, 11	01		25	ns
Conversion time	$t_{CONVERT}$		9, 10, 11	01		5.9	µs
$\overline{\text{CONVST}}$ pulse width	t_{CST}		9, 10, 11	01	100		ns
$\overline{\text{RFS}}$ low to SCLK falling edge	t_1		9, 10, 11	01		t_{CLKINH} + 50	ns
$\overline{\text{RFS}}$ low to valid delay 8/	t_2		9, 10, 11	01		25	ns
SCLK high pulse width	t_3		9, 10, 11	01		t_{CLKINH}	ns
SCLK low pulse width	t_4		9, 10, 11	01		t_{CLKINL}	ns
SCLK rising edge to data valid delay 8/	t_5		9, 10, 11	01		20	ns
SCLK rising edge to $\overline{\text{RFS}}$ delay	t_6		9, 10, 11	01		40	ns
Bus relinquish time after rising edge of SCLK 9/	t_7		9, 10, 11	01		50	ns
$\overline{\text{TFS}}$ low to SCLK falling edge	t_8		9, 10, 11	01	0	t_{CLKIN} + 50	ns
Data valid to TFS falling edge setup time (A2 address bit)	t_9		9, 10, 11	01	0		ns
Data valid to SCLK falling edge setup time	t_{10}		9, 10, 11	01	20		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/, 3/, 5/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data valid to SCLK falling edge hold time	t_{11}		9, 10, 11	01	10		ns
$\overline{\text{TFS}}$ to SCLK falling edge hold time	t_{12}		9, 10, 11	01	20		ns
$\overline{\text{RFS}}$ low to SCLK falling edge setup time	t_{13}		9, 10, 11	01	20		ns
$\overline{\text{RFS}}$ low to data valid delay 8/	t_{14}		9, 10, 11	01		40	ns
SCLK high pulse width	t_{15}		9, 10, 11	01	50		ns
SCLK low pulse width	t_{16}		9, 10, 11	01	50		ns
SCLK rising edge to data valid delay 8/	t_{17}		9, 10, 11	01		35	ns
$\overline{\text{RFS}}$ to SCLK falling edge hold time	t_{18}		9, 10, 11	01	20		ns
Bus relinquish time after rising edge of RFS	t_{19}		9, 10, 11	01		50	ns
Bus relinquish time after rising edge of SCLK 9/	t_{19A}		9, 10, 11	01		90	ns
$\overline{\text{TFS}}$ low to SCLK falling edge setup time	t_{20}		9, 10, 11	01	20		ns
Data valid to SCLK falling edge setup time	t_{21}		9, 10, 11	01	10		ns
Data valid to SCLK falling edge hold time	t_{22}		9, 10, 11	01	15		ns
$\overline{\text{TFS}}$ low to SCLK falling edge hold time	t_{23}		9, 10, 11	01	40		ns

1/ V_{DD} = +5.25 V, AGND = DGND = 0 V, REF IN = +2.5 V, f_{CLKIN} = 2.5 MHz external, MUX OUT connected to SHA IN.
2/ Full-scale error match applied to both positive and negative full scale.
3/ Subgroups 9, 10, and 11 are tested initially and after any changes which may affect these parameters. See figures 3 and 4.
4/ Analog inputs must be at 0 V to achieve correct power-down current.
5/ All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% 0f 5 V) and timed from a voltage level of 1.6 V. Tested initially and after any design changes which may affect these parameters.
6/ Production tested with f_{CLKIN} at 2.5 MHz. It is guaranteed by characterization to operate at 100 kHz.
7/ Specified using 10% and 90% points on waveform of interest.
8/ These numbers are measured with the load circuit of figure 3 and defined as the time required for the output to cross 0.8 V or 2.4 V.
9/ These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of figure 3. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

Device type	01
Case outlines	J and L
Terminal number	Terminal symbol
1	AGND
2	SMODE
3	DGND
4	C_{EXT}
5	$\overline{CONVST}$
6	CLK IN
7	SCLK
8	$\overline{TFS}$
9	$\overline{RFS}$
10	DATA OUT
11	DATA IN
12	V_{DD}
13	MUX OUT
14	SHA IN
15	AGND
16	V_{IN1}
17	V_{IN2}
18	V_{IN3}
19	V_{IN4}
20	V_{IN5}
21	V_{IN6}
22	V_{IN7}
23	V_{IN8}
24	REF OUT/REF IN

FIGURE 1. Terminal connections.

Analog Input	Digital output code transition
+FSR/2 – 1 LSB (9.995117 V)	011 . . . 110 to 011 . . . 111
+FSR/2 – 2 LSBs (9.990234 V)	011 . . . 101 to 011 . . . 110
+FSR/2 – 3 LSBs (9.985352 V)	011 . . . 100 to 011 . . . 101
AGND + 1 LSB (0.004883 V)	000 . . . 000 to 000 . . . 000
AGND (0.000000 V)	111 . . . 111 to 000 . . . 000
AGND – 1 LSB (0.004883 V)	111 . . . 110 to 111 . . . 111
-FSR/2 + 3 LSBs (-9.985352 V)	100 . . . 010 to 100 . . . 011
-FSR/3 + 2 LSBs (-9.990234 V)	100 . . . 001 to 100 . . . 010
-FSR/2 + 1 LSB (-9.995117 V)	100 . . . 000 to 000 . . . 000

FIGURE 2. Ideal in/output code table.

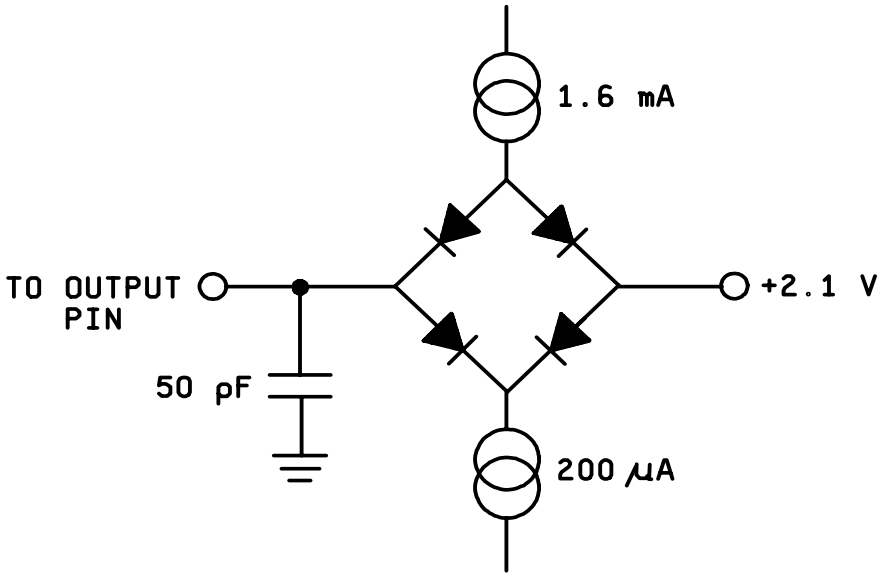
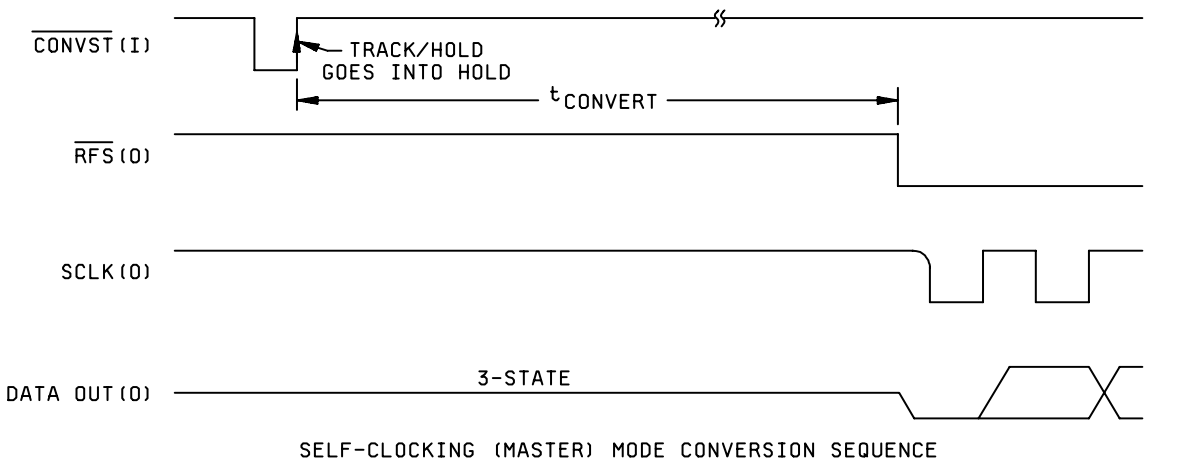
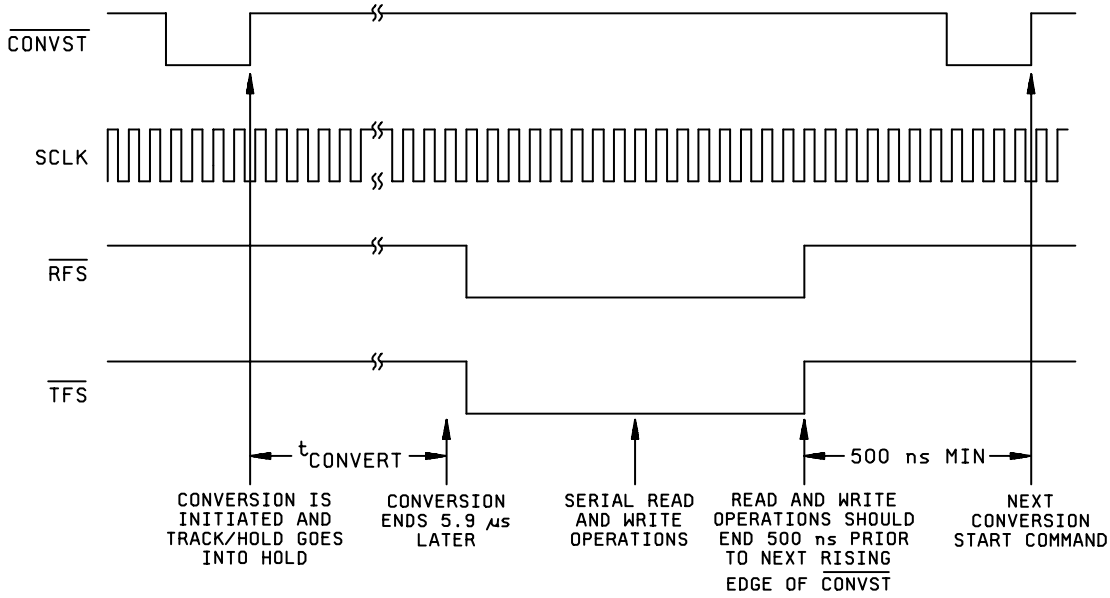


FIGURE 3. Load circuit for access time and bus relinquish time.

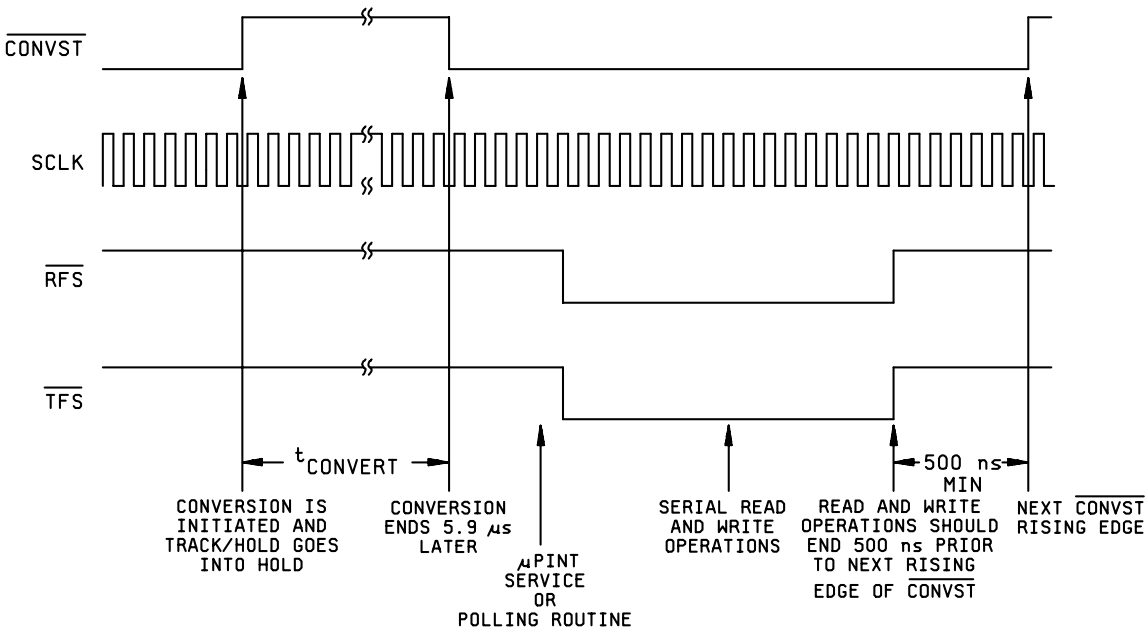


SELF-CLOCKING (MASTER) MODE CONVERSION SEQUENCE

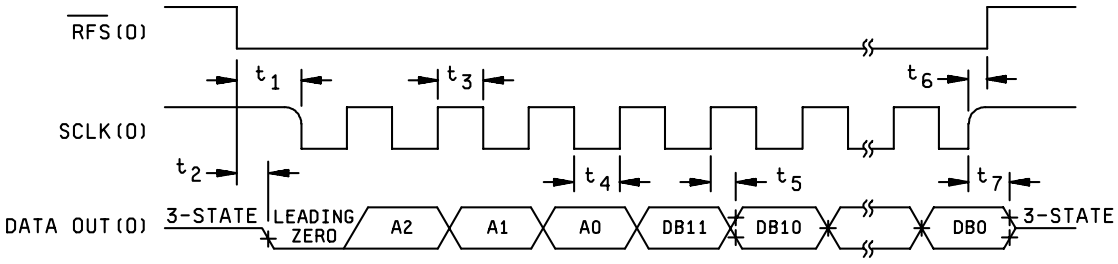


EXTERNAL CLOCKING (SLAVE) MODE TIMING SEQUENCE FOR OPTIMUM PERFORMANCE

FIGURE 4. Timing waveforms.

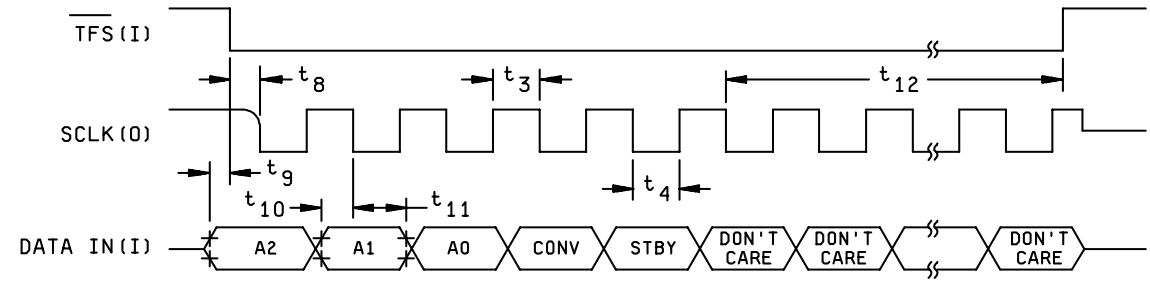


CONVST USED STATUS SIGNAL IN EXTERNAL CLOCKING MODE

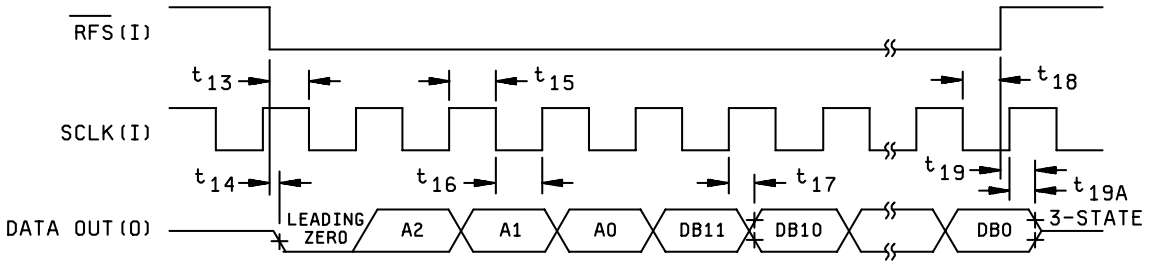


SELF-CLOCKING (MASTER) MODE OUTPUT REGISTER READ

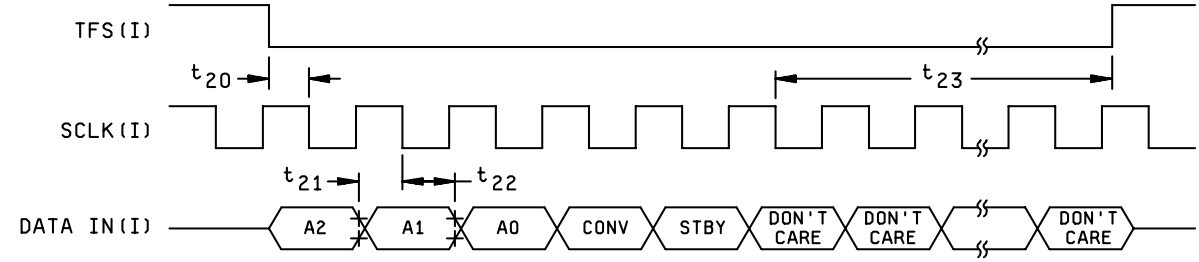
FIGURE 4. Timing waveforms - continued.



SELF-CLOCKING (MASTER) MODE CONTROL REGISTER WRITE



EXTERNAL CLOCKING (SLAVE) MODE OUTPUT REGISTER READ



EXTERNAL CLOCKING (SLAVE) MODE CONTROL REGISTER WRITE

FIGURE 4. Timing waveforms - continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 9, 10, 11 are tested initially and after any design changes which may affect the parameters in those subgroups.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 2, 3	1, 2, 3	1, 2, 3
Final electrical parameters (see 4.2)	1, 2, 3, 1/, 2/ 9, 10, 11	1, 2, 3, 1/, 2/ 9, 10, 11	1, 2, 3, 1/, 2/ 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 2/ 9, 10, 11	1, 2, 3, 2/ 9, 10, 11	1, 2, 3, 2/ 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	- - -	- - -	- - -

1/ PDA applies to subgroup 1.
2/ Subgroups 9, 10, 11 are tested initially and after any design changes which may affect the parameters in those subgroups.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-09-20

Approved sources of supply for SMD 5962-95615 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9561501MLA	24355	AD7890SQ-10/QML
5962-9561501MJA	3/	

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: Bay F-1 Raheen Ind. Estate Limerick, Ireland