

5V Low Power Subscriber DTMF Receiver

January 1997

Features

- No Front End Band Splitting Filters Required
- Single Low Tolerance 5V Supply
- Three-State Outputs for Microprocessor Based Systems
- Detects all 16 Standard DTMF Digits
- Uses Inexpensive 3.579545MHz Crystal
- Excellent Speech Immunity
- Output in 4-Bit Hexadecimal Code
- Excellent Latch-Up Immunity

Ordering Information

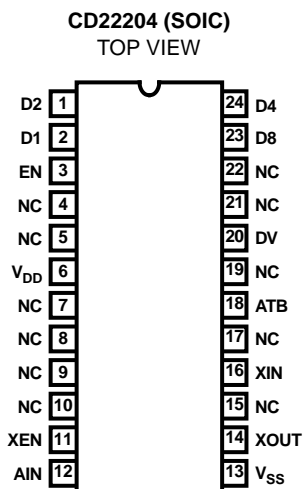
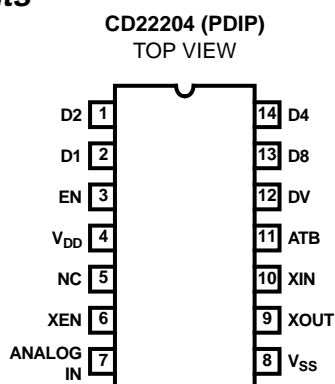
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22204E	0 to 70	14 Ld PDIP	E14.3
CD22204M	0 to 70	24 Ld Plastic SOIC	M24.3

Description

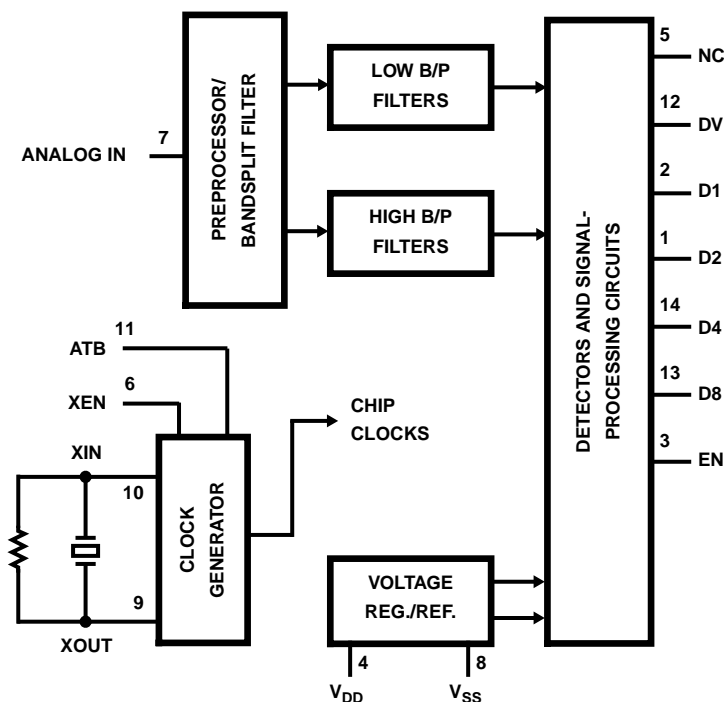
The CD22204 complete dual tone multiple frequency (DTMF) receiver detects a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.579545MHz TV "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is possible through the use of the Alternate Time Base (ATB) output of a crystal connected CD22204 receiver to drive the time bases of up to 10 additional receivers. This is a monolithic integrated circuit fabricated with low power, complementary symmetry CMOS processing. It only requires a single power supply.

The CD22204 employs state-of-the-art "switched-capacitor" filter technology, resulting in approximately 40 poles of filtering and digital circuitry on the same CMOS chip. The analog input is preprocessed by 60Hz reject and bandsplitting filters and then zero-cross detected to provide AGC. Eight bandpass filters detect the individual tones. Digital processing is used to measure the tone and pause durations and provides the correctly coded and timed digital outputs. The outputs interface directly to standard CMOS circuitry and are three-state enabled to facilitate bus oriented architectures.

Pinouts



Functional Diagram



NOTE: Pin numbers are for PDIP.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{DD}) (Referenced to V_{SS} Terminal) 7V
 Power Dissipation

$T_A = 25^\circ\text{C}$ (Derate above $T_A = 25^\circ\text{C}$ at $6.25\text{mW}/^\circ\text{C}$) 65mW
 Input Voltage Range

All Inputs Except Analog In ($V_{DD} 0.5\text{V}$) to -0.5V
 Analog in Voltage Range ($V_{DD} 0.5\text{V}$) to ($V_{DD} -10\text{V}$)
 DC Current into any Input or Output $\pm 20\text{mA}$

Thermal Information

Maximum Junction Temperature 175°C
 Maximum Junction Temperature (Plastic) 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C

Operating Conditions

Temperature Range 0°C to 70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

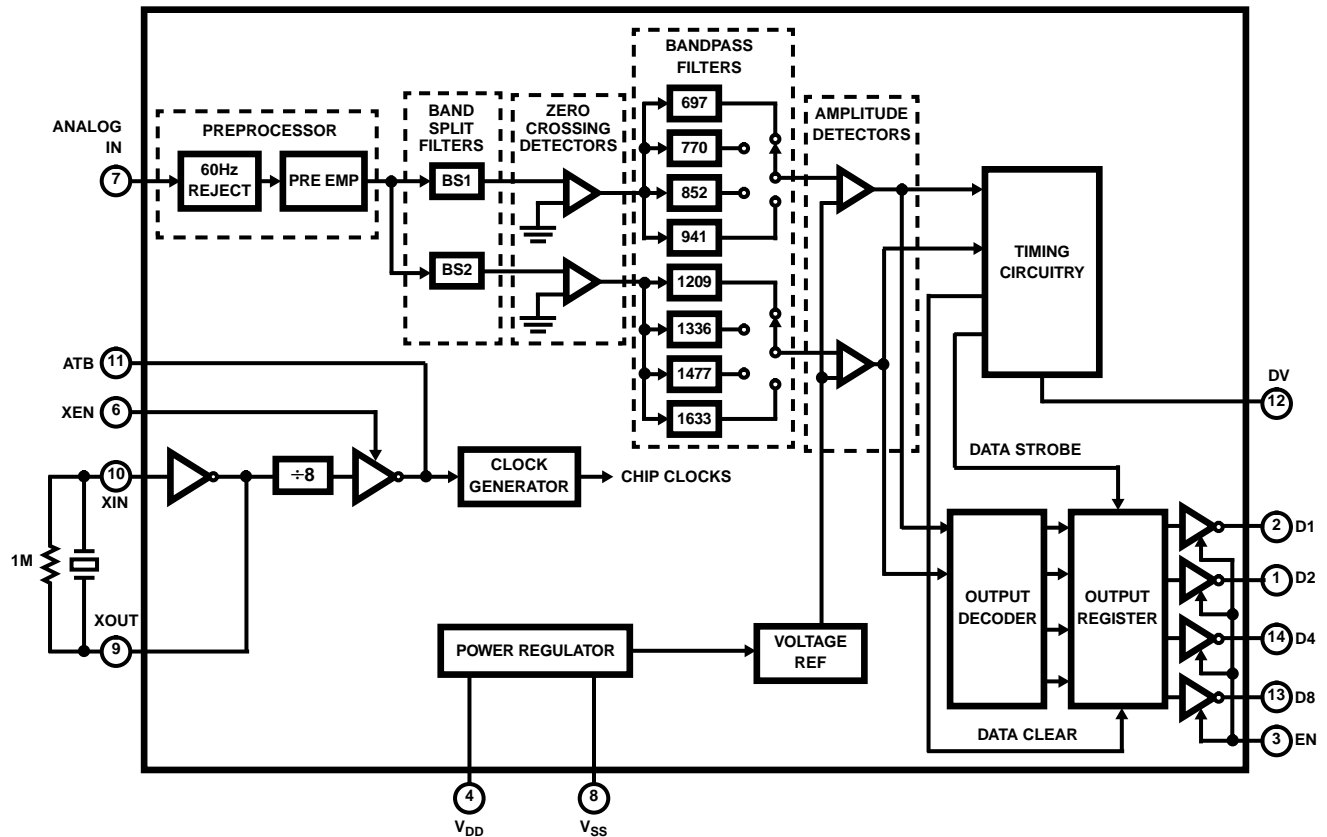
Electrical Specifications $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		$\pm(1.5 + 2\text{Hz})$	± 2.3	± 3.5	% of f_O
Amplitude for Detection	Each Tone	-32 (Note 3)	-	-2	dBm Referenced to 600Ω
Minimum Acceptable Twist	$\text{Twist} = \frac{\text{High Tone}}{\text{Low Tone}}$	-8	-	+4	dB
60Hz Tolerance		-	-	0.8	V_{RMS}
Dial Tone Tolerance	"Precise" Dial Tone	-	-	0	dB Referenced to Lower Amplitude Tone
Talk Off	MITEL Tape #CM7291	-	2	-	Hits
Digital Outputs (except XOUT)	"0" Level, $400\mu\text{A}$ Load	0	-	0.5	V
	"1" Level, $200\mu\text{A}$ Load	$V_{DD} - 0.5$	-	V_{DD}	V
Digital Inputs	"0" Level	0	-	$0.3V_{DD}$	V
	"1" Level	$0.7V_{DD}$	-	V_{DD}	V
Supply Current	$T_A = 25^\circ\text{C}$	-	10	20	mA
Noise Tolerance	MITEL Tape #CM7291 (Note 2)	-	-	-12	dB Referenced to Lowest Amplitude Tone
Input Impedance	$V_{DD} \geq V_{IN} \geq (V_{DD} - 10)$	$100\text{k}\Omega//15\text{pF}$	$300\text{k}\Omega$	-	

NOTES:

- Unused inputs must be connected to V_{DD} or V_{SS} as appropriate.
- Bandwidth limited (3kHz) Gaussian noise.
- Lower minimum available, please contact sales office.
 $(-32\text{dBm} = 19.45\text{mV}_{RMS}$, $-2\text{dBm} = 0.615\text{mV}_{RMS}$)

Functional Block Diagram



NOTE: Pin numbers are for plastic DIP.

System Functions

Analog In

The Analog In pin accepts the analog input. It is internally biased so that the input signal may be either AC or DC coupled, as long as it does not exceed the positive supply voltage. Proper input coupling is illustrated below.

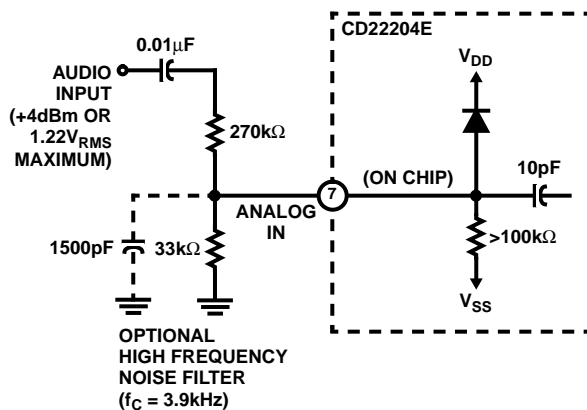


FIGURE 1. ANALOG IN

The CD22204 is designed to accept sinusoidal input waveforms, but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics that are at least 20dB below the fundamental.

Crystal Oscillator

The CD22204 contains an on-board inverter with sufficient gain to provide oscillation when connected to a low cost television "color-burst" (3.579545MHz) crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1MΩ resistor is also connected between these pins in this mode. ATB is a clock frequency output. Other CD22204 devices may use the same frequency reference by tying their ATB pins to the ATB output of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low, respectively. Up to ten devices may be run from a single crystal connected CD22204 as shown in Figure 2.

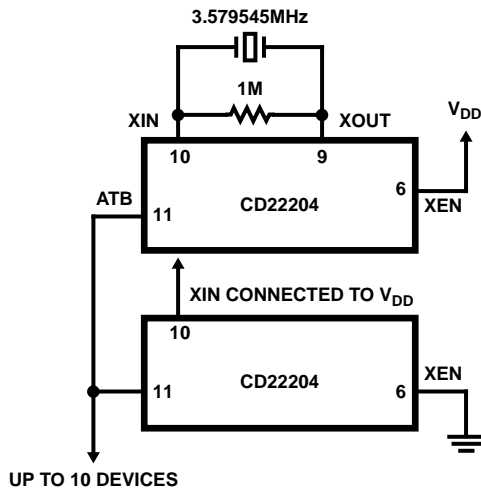


FIGURE 2. CRYSTAL OSCILLATOR

Outputs D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the hexadecimal code corresponding to the detected digit. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed. The table below describes the hexadecimal codes.

TABLE 1. OUTPUT CODES

DIGIT	D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

DV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs.

N/C Pin

This pin has no internal connection and should be left floating.

DTMF Dialing Matrix

	COL 0 1209Hz	COL 1 1336Hz	COL 2 1477Hz	COL 3 1633Hz
ROW 0 697Hz	[1]	[2]	[3]	[A]
ROW 1 770Hz	[4]	[5]	[6]	[B]
ROW 2 852Hz	[7]	[8]	[9]	[C]
ROW 3 941Hz	[*]	[0]	[#]	[D]

NOTE: Column 3 is for special applications and is not normally used in telephone dialing.

Digital Inputs and Outputs

All digital inputs and outputs of the DTMF receivers are represented by the schematic below. Only the "analog in" pin is different, and is described above. Care must be exercised not to exceed the voltage or current ratings on these pins as listed in the "maximum ratings" section.

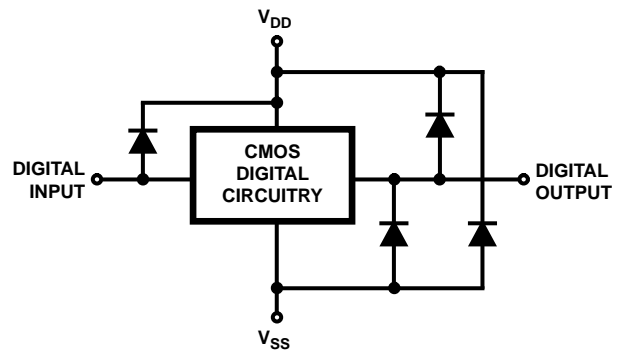


FIGURE 3. DIGITAL INPUTS AND OUTPUTS

Input Filter

The CD22204 will tolerate total input noise of a maximum of 12dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band limiting make special circuitry at the input to these receivers unnecessary. However, noise near the 56kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present above 28kHz, the simple RC filter shown below may be used to band limit the incoming signal. The cut off frequency is 3.9kHz.

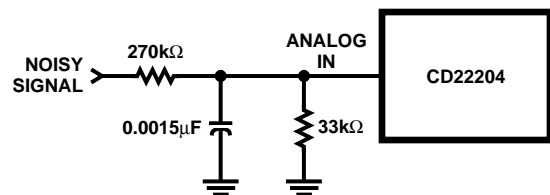


FIGURE 4. FILTER FOR USE IN EXTREME HIGH FREQUENCY INPUT NOISE ENVIRONMENT

Noise will also be reduced by placing a grounded trace around XIN and XOUT pins on the circuit board layout when using a crystal. It is important to note that XOUT is not intended to drive an additional device. XIN may be driven externally; in this case, leave XOUT floating.

Timing Waveforms

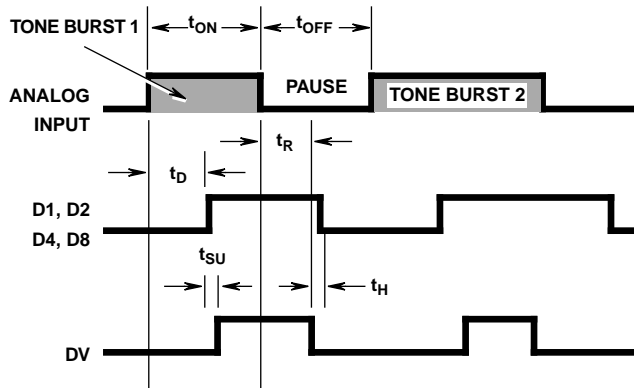


FIGURE 5.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Tone Time					
For Detection	t_{ON}	40	-	-	ms
For Rejection	t_{ON}	-	-	20	ms
Pause Time					
For Detection	t_{OFF}	40	-	-	ms
For Rejection	t_{OFF}	-	-	20	ms
Detect Time	t_D	25	-	46	ms
Release Time	t_R	35	-	50	ms
Data Setup Time	t_{SU}	7	-	-	μ s
Data Hold Time	t_H	4.2	-	5	ms
Output Enable Time $C_L = 50\text{pF}$, $R_L = 1\text{k}\Omega$	-	-	200	300	ns
Output Disable Time $C_L = 35\text{pF}$, $R_L = 500\Omega$	-	-	150	200	ns
Output Rise Time $C_L = 50\text{pF}$	-	-	200	300	ns
Output Fall Time $C_L = 50\text{pF}$	-	-	160	250	ns

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Harris Semiconductor products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Harris is believed to be accurate and reliable. However, no responsibility is assumed by Harris or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Harris or its subsidiaries.

Sales Office Headquarters

For general information regarding Harris Semiconductor and its products, call **1-800-4-HARRIS**

NORTH AMERICA

Harris Semiconductor
P. O. Box 883, Mail Stop 53-210
Melbourne, FL 32902
TEL: 1-800-442-7747
(407) 729-4984
FAX: (407) 729-5321

EUROPE

Harris Semiconductor
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Harris Semiconductor PTE Ltd.
No. 1 Tannery Road
Cencon 1, #09-01
Singapore 1334
TEL: (65) 748-4200
FAX: (65) 748-0400

