Isolated Power Supply IC for Automotive

1 Channel Step-up Switching Regulator Controller

BD9031FV-C

●General Description

The BD9031FV-C is a 1 channel isolated and step-up switching regulator (controller).
BD9031FV-C features a wide range of integrated safety functions, e.g. input undervoltage protection, output overvoltage protection, output undervoltage protection, overcurrent protection and thermal shutdown.

●Features

- Maximum supply voltage 35V
- Accurate reference voltage ±1.5%
- Adjustable frequency: 20kHz to 600kHz
- Integrated EN functionality
- Current mode control
- Input undervoltage protection (UVLO)
- Overheating protection (TSD)
- Output overvoltage protection (OVP)
- Output undervoltage protection (UVP)
- Overcurrent protection (OCP)
- SSOP-B16 package

●Application

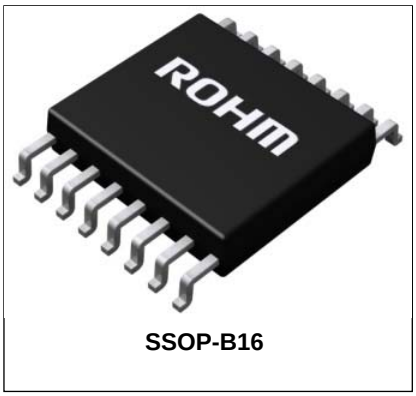
- Automotive isolated power supplies

●Key specification

- Operating supply voltage range: 4.5V to 30V
- Switching frequency: 20kHz to 600kHz
- Pch FET ON resistance: 6Ω (typ.)
- Nch FET ON resistance: 0.84 Ω (typ.)
- Standby current: 0μA (typ.)
- Operating temperature range: -40°C to +125°C

●Packages

	W (typ.) x D (typ.) x H (max.)
SSOP-B16	5.00mm x 6.40mm x 1.35mm



SSOP-B16

●Typical Application Circuits

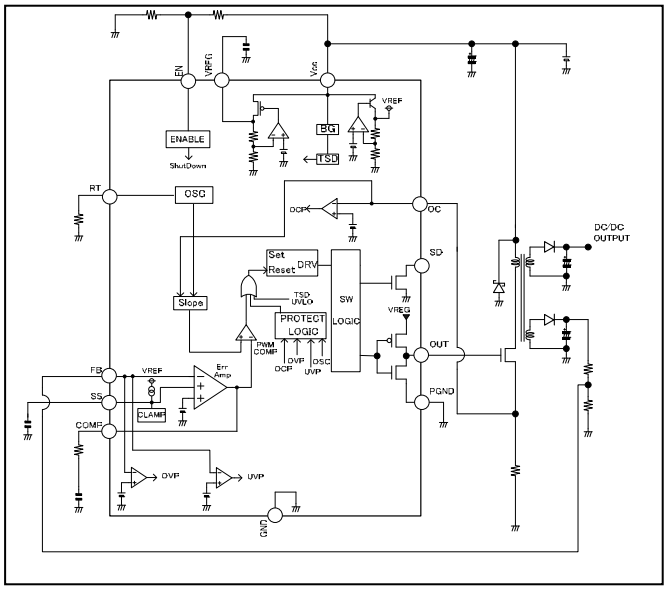


Figure 1. Block Diagram and Typical Application Circuit

●**Pin Configuration**

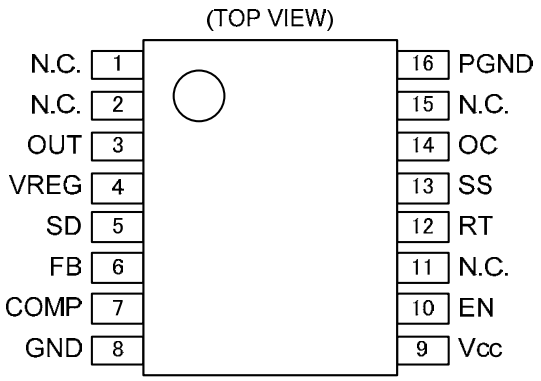


Figure 2. Pin Configuration

●**Pin Description**

Pin No.	Pin Name	Function
1	N.C.	Not connected
2	N.C.	Not connected
3	OUT	Gate driver output pin
4	VREG	Regulator output for FET driver pin
5	SD	Transistor driver pin for shutdown
6	FB	Error amplifier inverted input pin
7	COMP	Error amplifier output pin
8	GND	Ground pin
9	Vcc	Power supply pin
10	EN	EN functionality pin
11	N.C.	Not connected
12	RT	Frequency setting pin
13	SS	Soft start setting pin
14	OC	Overcurrent detection pin
15	N.C.	Not connected
16	PGND	Power ground pin

●**Block Diagram**

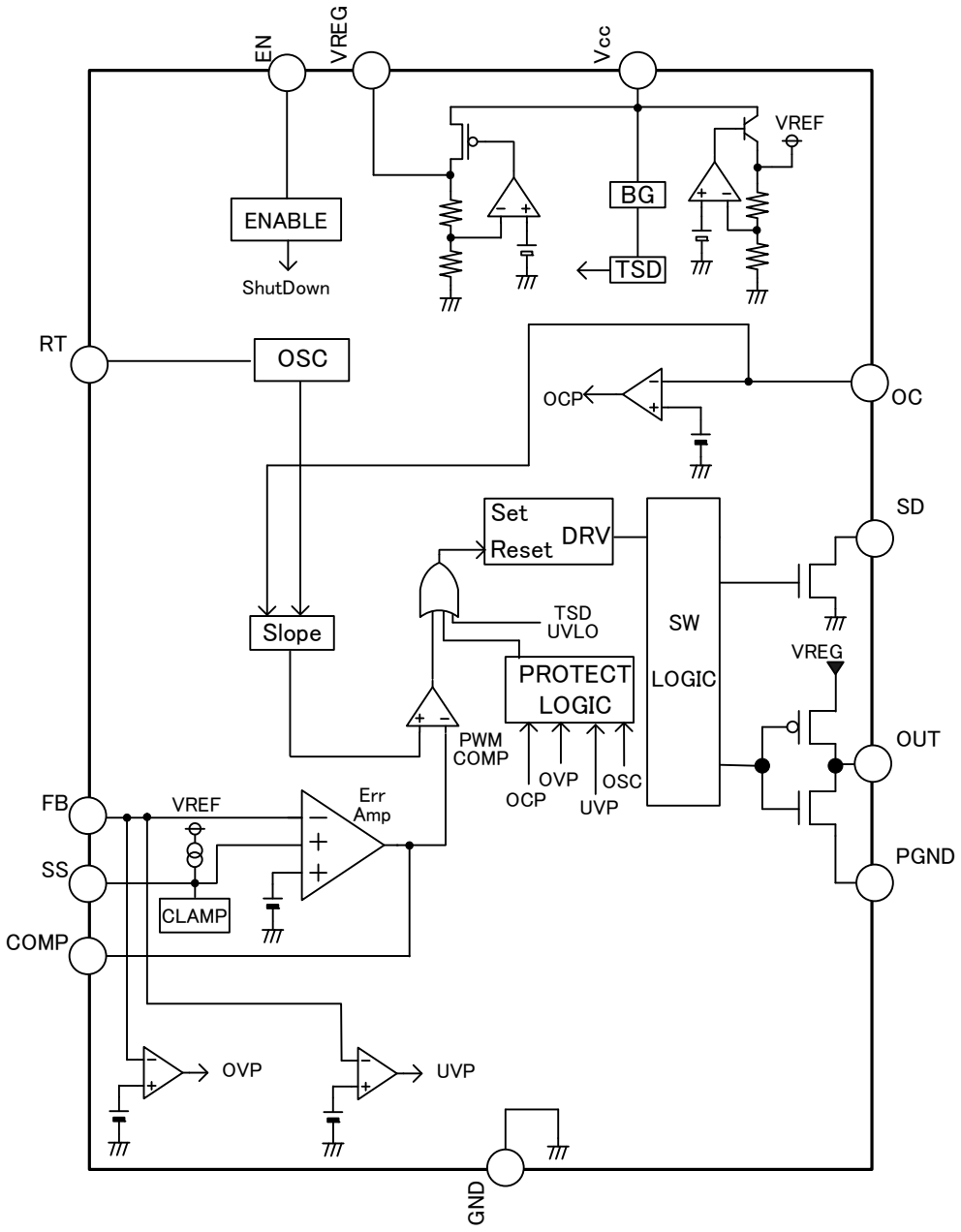


Figure 3. Block Diagram

●Explanation of Block Operations

- VREF
  3.0V Regulator block for internal supply.

- VREG
  Voltage supply block for DC/DC driver.

- TSD
  Thermal protection block that turns off the IC if the internal temperature reaches 175°C (typ.).

- UVLO
  Undervoltage-lockout block.

- OVP
  Overvoltage protection block that turns off the IC if FB exceeds 0.92V (typ.).
  If the protection function is activated, the output is turned off and the Soft Start pin and COMP pin voltages are discharged for a fixed period dependent on the oscillation frequency.

- UVP
  Undervoltage protection block that turns off the IC if FB drops below 0.60V (typ.).
  If the protection function is activated, the output is turned off and the Soft Start pin and COMP pin voltages are discharged for a fixed period dependent on the oscillation frequency.

- Error amplifier (ERR)
  Block that compares the output feedback voltage to the reference voltage and outputs the difference to the COMP pin, which voltage is used to determine the switching duty cycle.

- Oscillator (OSC)
  Block that generates the oscillation frequency.

- Slope
  Block that generates a triangle wave from the clock generated in the oscillator block and sends it to the PWM comparator.

- PWM
  Block that compares the output COMP pin voltage of the error amplifier with the triangle wave of the slope and determines the switching duty. The switching duty is limited by the internally set maximum duty ratio and cannot become 100%.

- DRV
  DC/DC driver block with the PWM signal as input and that drives the output MOS.

- Soft start
  Block that limits the current at time of startup and gradually increases the output voltage thereby preventing an overshoot of the output voltage and inrush current.

- OCP
  Overcurrent protection block. The overcurrent protection level is determined by the value of the resistor placed in between theOC pin and GND. Overcurrent is detected when the OC pin voltage exceeds 0.2V (typ.). The overcurrent detection function is performed every switching pulse cycle. When overcurrent is detected 256 times consecutively, the overcurrent protection is activated and the IC is shut down. Thus, even if the OC pin reaches or exceeds the overcurrent detection level caused by a DC voltage, the overcurrent protection is not activated since it is only a one time detection.
  If the protection function is activated the output is turned and the Soft Start pin and COMP pin are discharged for a fixed period depending on the oscillator frequency.

- SD
  Transistor driver block for turning off the IC when a protection function is activated (Nch open drain).

●**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Rating	Unit
Voltage	Vcc	-0.3 to 35*1	V
VREG Voltage	VREG	7	V
EN Voltage	VEN	Vcc	V
OC Voltage	VOC	V_{REG}	V
SD Voltage	VSD	Vcc	V
Power Dissipation	Pd	870*2	mW
Operating Temperature Range	Top	-40 to +125	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	150	°C

*1 Pd should not be exceeded.
*2 7.0mW/°C reduction when Ta≧25°C if mounted on a glass epoxy board of 70mm×70mm×1.6mm

●**Operating Conditions** (Ta=-40°C to +125°C)

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Voltage	Vcc	4.5	14	30	V
Oscillation frequency	FOSC	20	—	600	kHz

●**Electrical Characteristics**

(Unless otherwise specified: 4.5≦Vcc≦30V, -40°C ≦T_{op}≦125°C, current flowing from the IC is defined +)

Parameter	Symbol	Ratings			Unit	Conditions
		Min.	Typ.	Max.		
Output block						
Output voltage H1	VOUTH1	4.5	5.0	5.5	V	5≦Vcc≦30V IOUT=0A(open)
Output voltage H2	VOUTH2	4.0	4.5	-	V	Vcc＝4.5V IOUT=0A(open)
Output voltage L	VOUTL	0	-	0.3	V	IOUT=0A(open)
MOS on resistor (source)	Ron_source	3	6	12	Ω	Isource=10mA
MOS on resistor (sink)	Ron_sink	0.46	0.84	1.80	Ω	Isink=-10mA
Oscillator block						
Oscillation frequency	fsw	360	400	440	kHz	RT=72kΩ
Soft start block						
Output range	VSSout	1.8	2.2	2.6	V	
Startup charge current	Istr	7.5	10.0	12.5	μA	SS=0V
Shut-off discharge current	Istp	-8.0	-3.0	-0.6	mA	
Error amp. block						
Threshold voltage	Veth	0.788	0.800	0.812	V	FB=COMP
Input bias current	IIB	-1	-	1	μA	FB=1.0V
Output sink current	Icompsink	-150	-75	-20	μA	FB=1.0V　COMP=0.8V
Output source current	Icompsource	20	75	150	μA	FB=0.6V　COMP=0.8V
EN block						
Threshold voltage	VEN	1.00	2.15	2.70	V	
Input bias current	IEN	8	16	32	μA	EN=3V
UVLO block						
UVLO operating voltage	VUVLO	3.3	3.6	3.9	V	VREG SWEEP DOWN
Hysteresis voltage	VULOhys	200	400	600	mV	VREG SWEEP UP
Overvoltage protection block						
Overvoltage detection threshold	Vovth	0.90	0.92	0.94	V	
FB open detection block						
Undervoltage detection threshold	Vopth	0.57	0.60	0.63	V	
Overcurrent protection block						
Overcurrent detection threshold	Vocth	0.16	0.20	0.24	V	
Hibernation period adjustment block						
Max on DUTY	Donmax	77	87	97	%	
Transistor driver block for shutdown						
Pin voltage (normal operation)	Vsdl	0	-	0.8	V	Normally ” L ” Isdsink=-1mA
Leakage current	Isdleak	-	-	10	μA	Vsd=30V
Entire chip						
Average current consumption	ICC	-	3	6	mA	Switching　off

○This product is not designed to be radiation resistant.

● **Characteristics Data (reference data)**

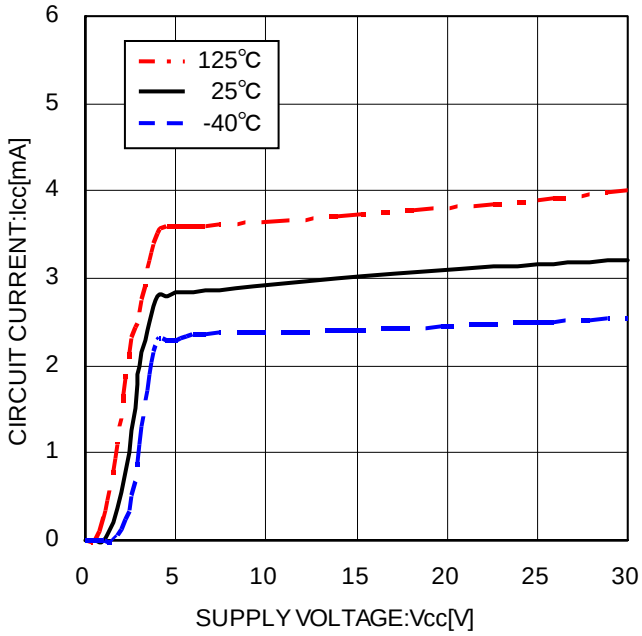


Figure 4. Average current consumption

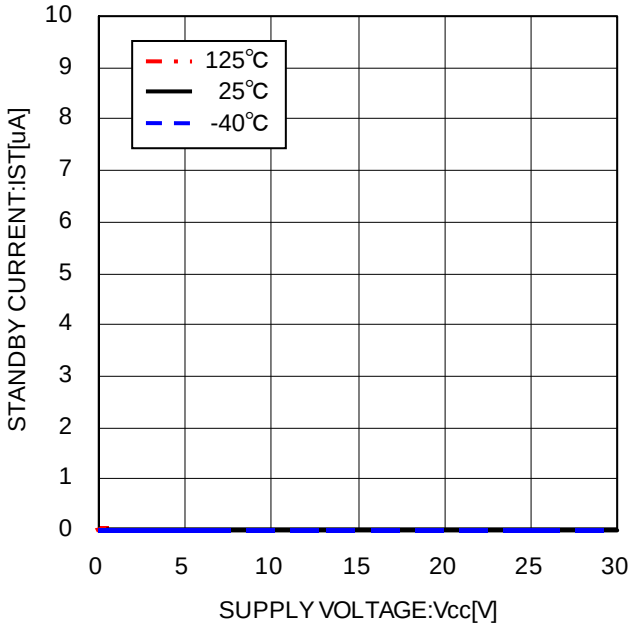


Figure 5. Standby current

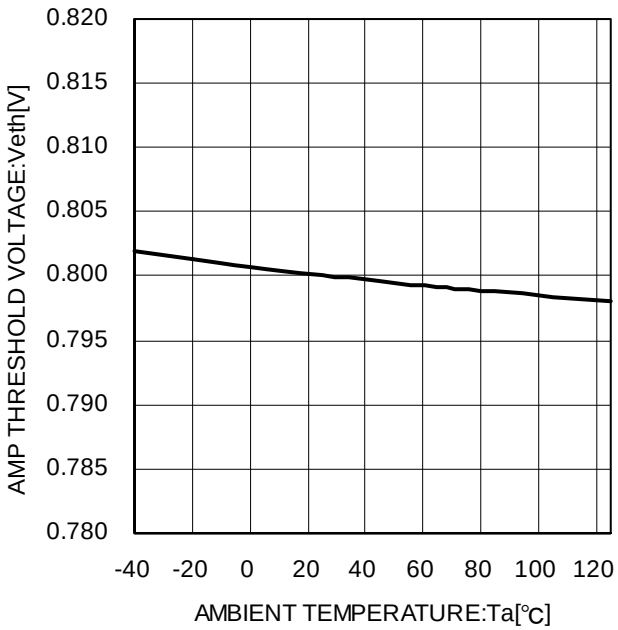


Figure 6. Error amp threshold voltage vs. temperature characteristics

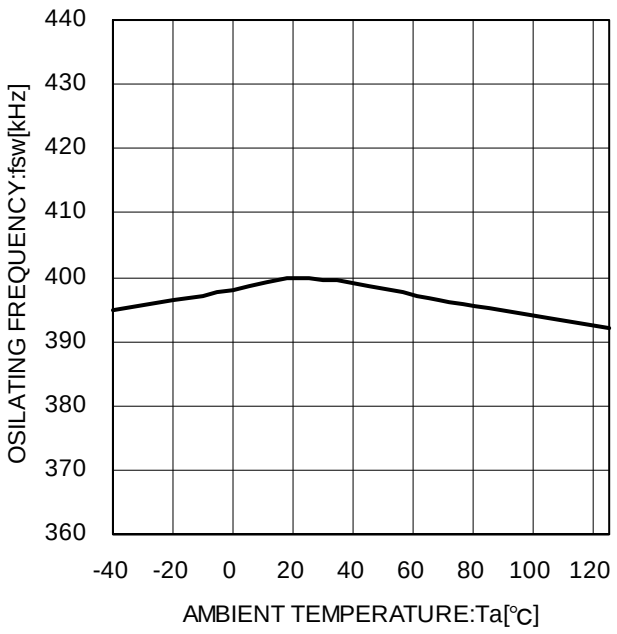


Figure 7. Oscillation frequency vs. temperature characteristics

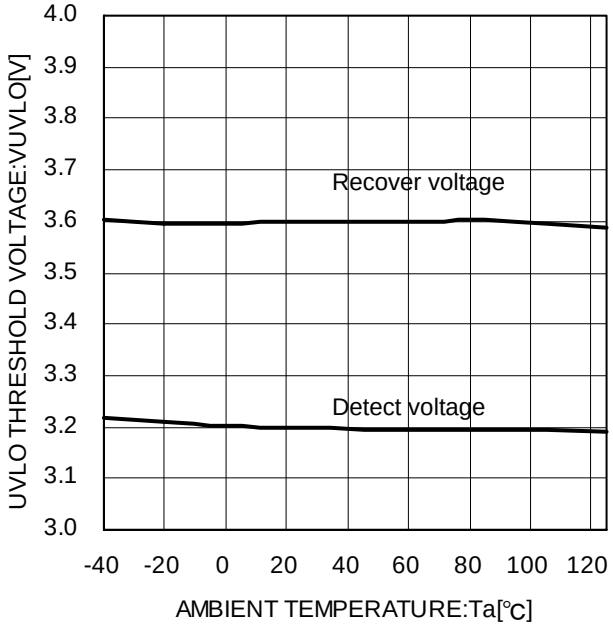


Figure 8. UVLO operating/return voltage vs. temperature characteristics

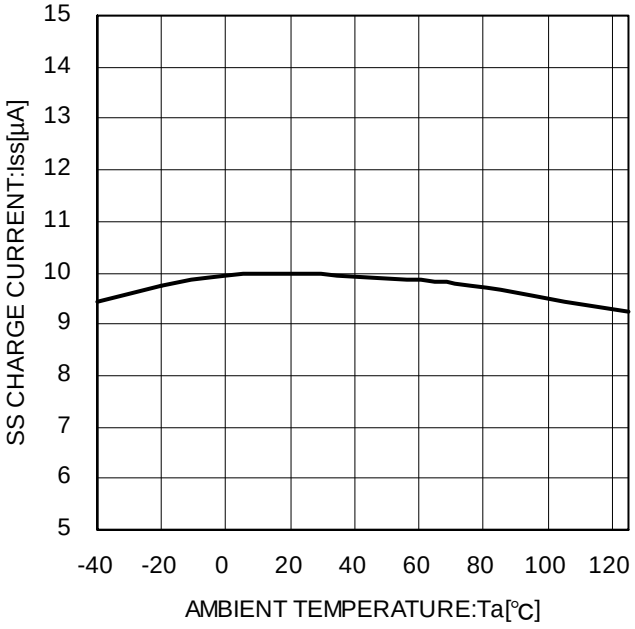


Figure 9. Soft start startup charge vs. temperature characteristics

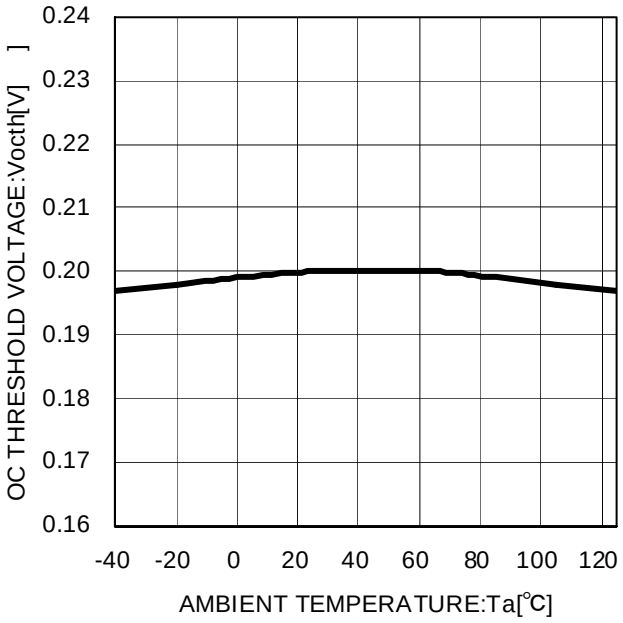


Figure 10. Overcurrent threshold voltage vs. temperature characteristics

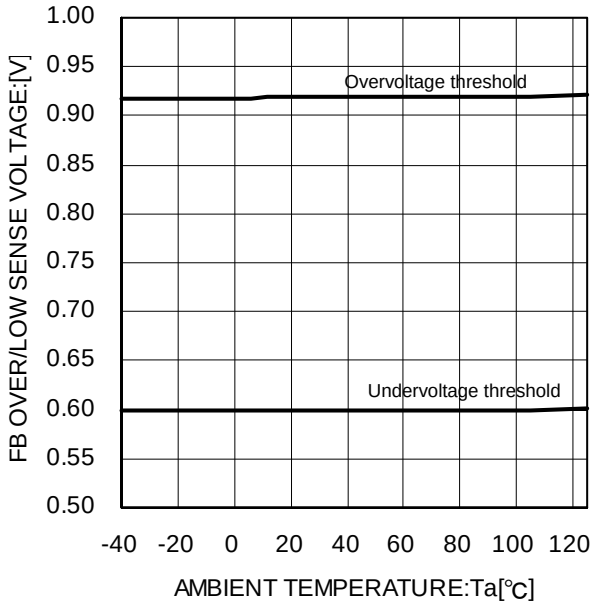


Figure 11. FB pin overvoltage/undervoltage threshold voltage vs. temperature characteristics

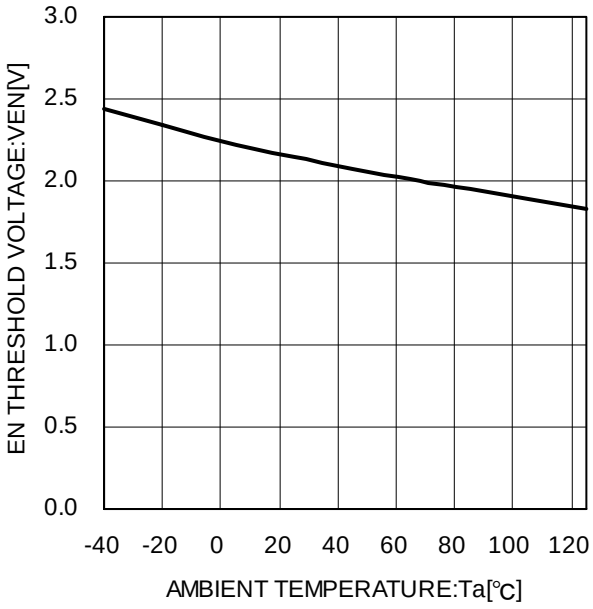


Figure 12. EN threshold voltage vs. temperature characteristics

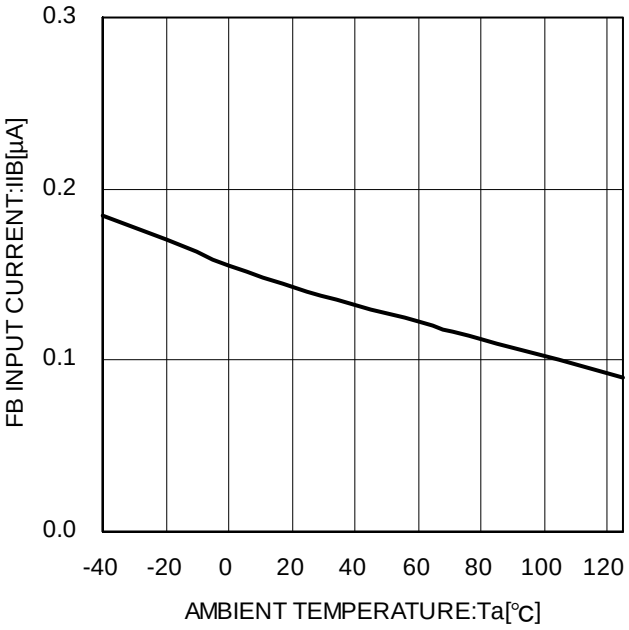


Figure 13. FB pin input bias current vs. temperature characteristics

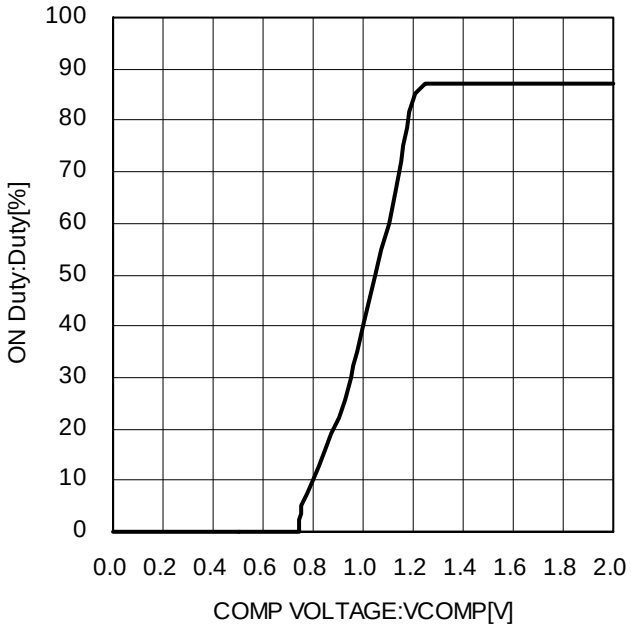


Figure 14. ON Duty characteristics

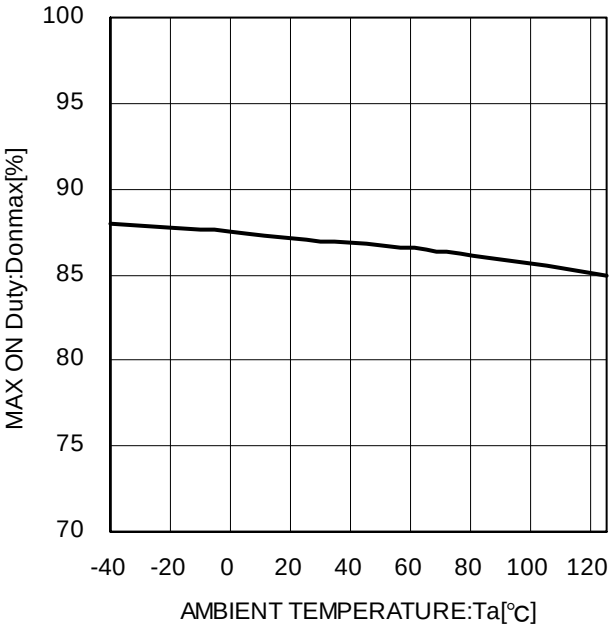


Figure 15. Max. ON duty vs. temperature characteristics

●**Timing chart**

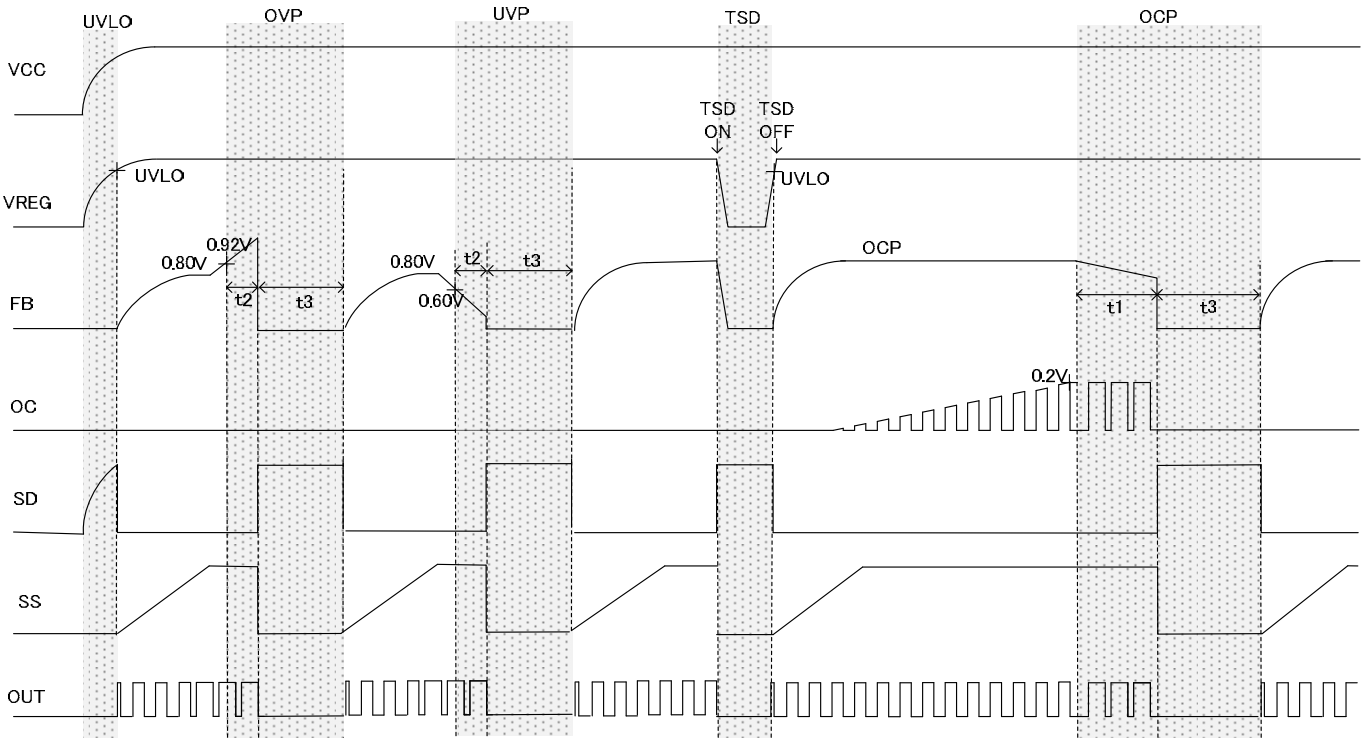


Figure 16. Timing chart

■Detection Time

The IC will be shut down if the time resulting from the following equation is exceeded.

After OCP detection, t1 = 1/f × 256clk (s)

Time needed for the OC pin output pulse to synchronize with the switching frequency and for the OCP block to perform 256 consecutive detections.

After OVP or UVP detection: t2 = 1/f × 4clk (s)

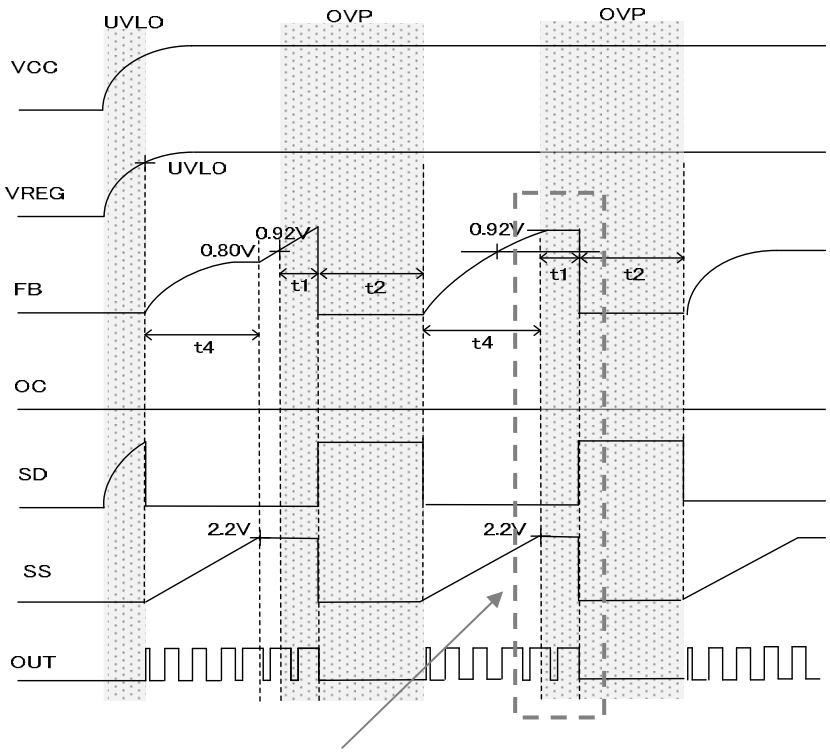
■Release Time

The output is turned off and the Soft start and COMP voltages are discharged during the time resulting from the following equation.

OVP or UVP or OCP, t3 = 1/f × 1024clk (s)

f: Oscillator frequency (kHz)

●Overvoltage Protection (OVP) Timing chart



This chart shows the overvoltage detection start time after startup. This start time can be calculated as follows:

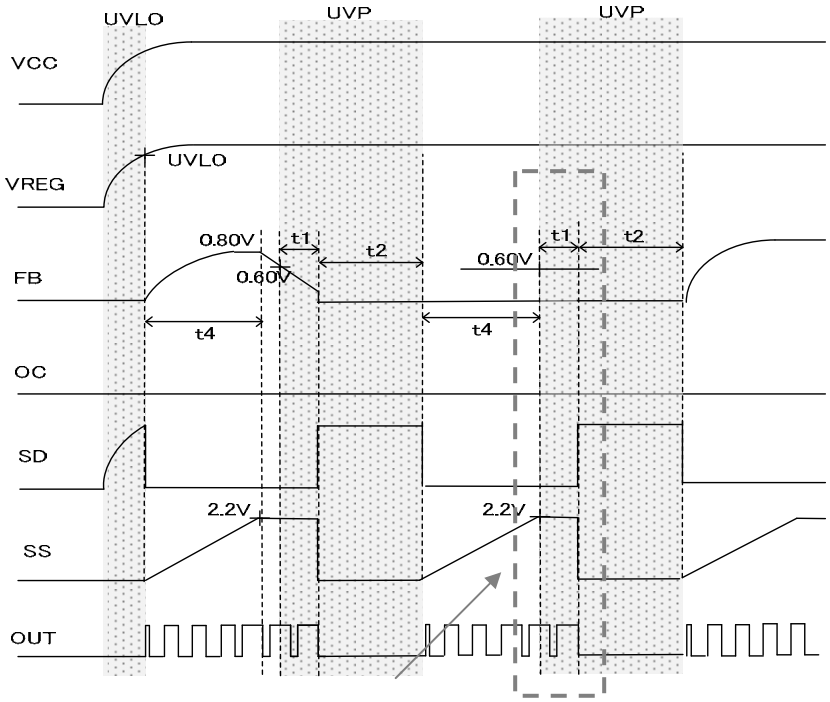
$t4=2.2V\ (typ.) \times C_{ss} /10\mu A\ (typ.)$ (s)

2.2V (typ.):soft start output range
C_{SS}: SS pin external capacitor
10μA(typ.): soft start charge current

The Over-voltage is detected after the soft start voltage reaches 2.2V (typ.).

Figure 17. Overvoltage protection (OVP) timing chart

●Undervoltage Protection (UVP) Timing chart



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2.2V (typ.): soft start output range
C_{SS}: SS pin external capacitor
10μA(typ.): soft start charge current

Under-voltage is detected after the soft start voltage reaches 2.2V (typ.).

Figure 18. Undervoltage protection (UVP) timing chart

●**Reference data**

Non-isolated type application

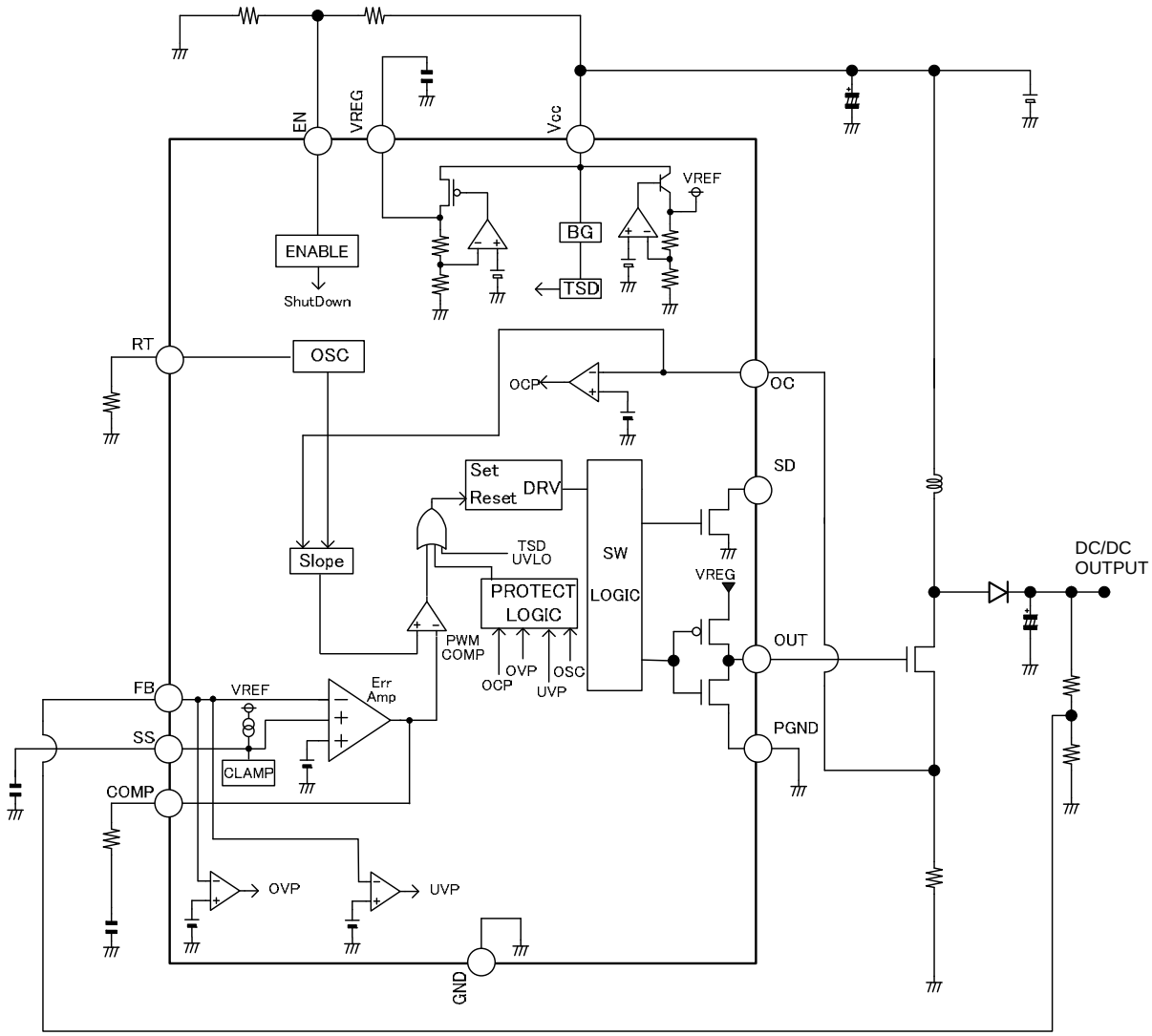


Figure 19. Non-isolated type application circuit example

Flyback type application

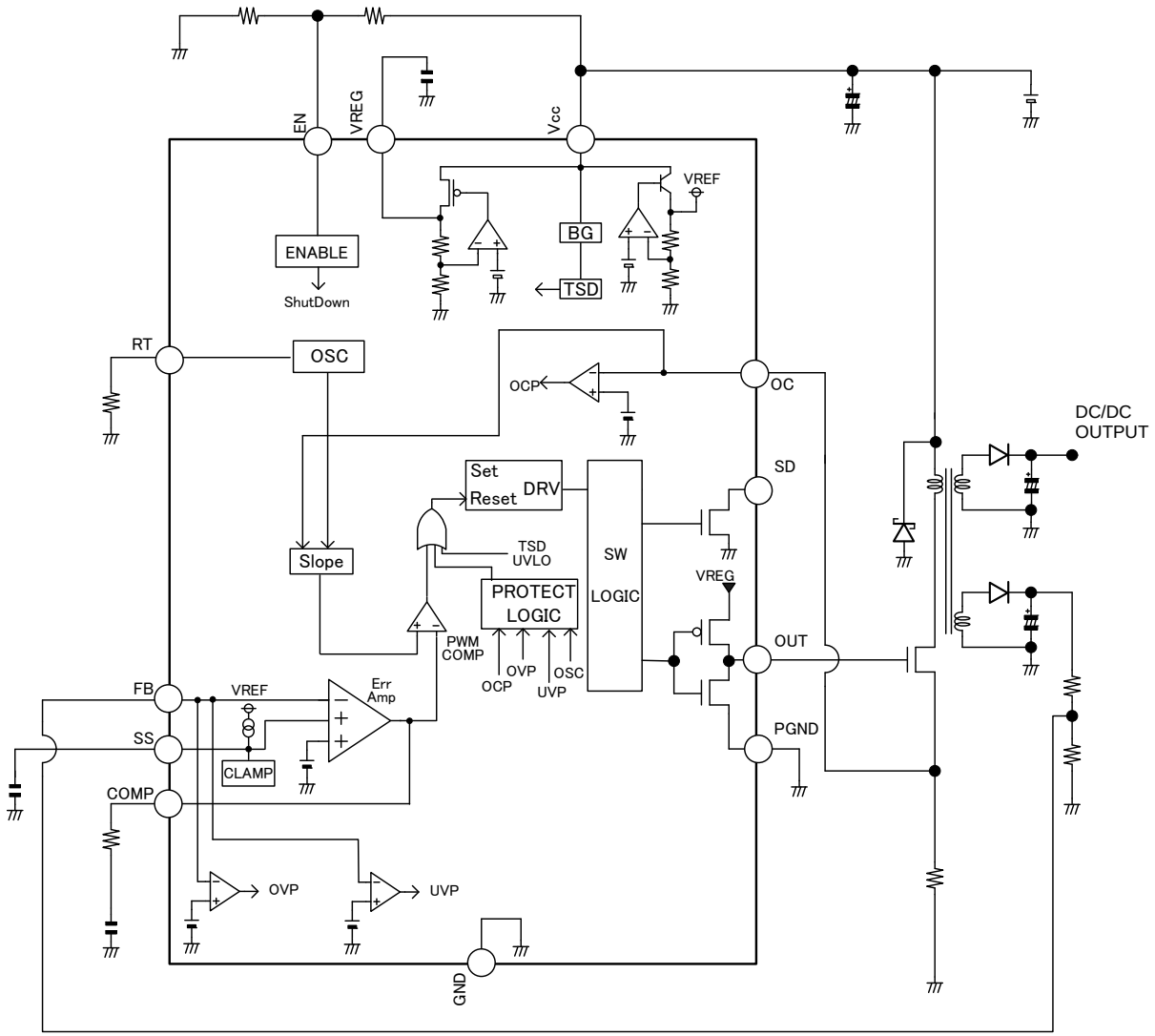


Figure 20. Flyback type application circuit example

Non-isolated application using SD

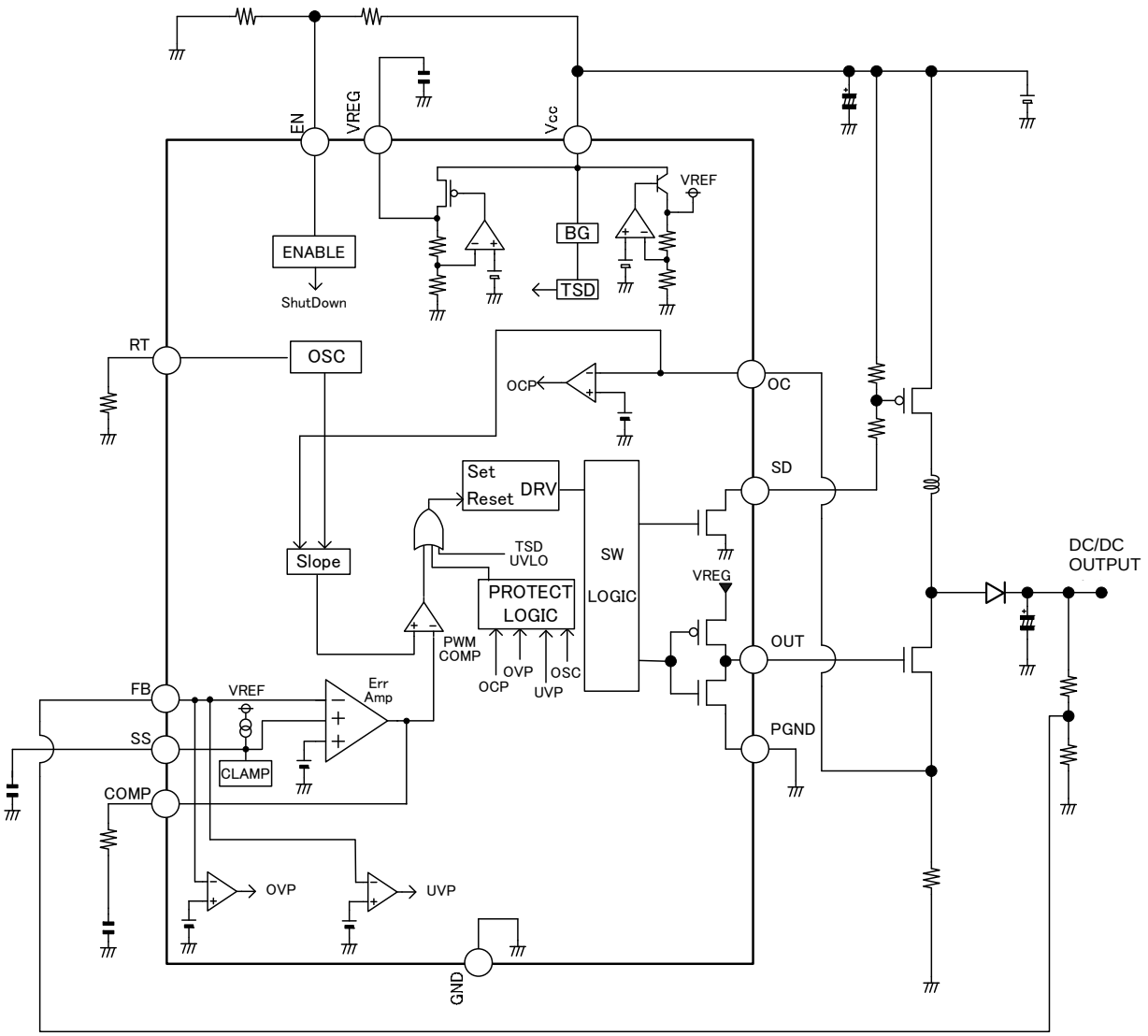


Figure 21. Non-isolated application using SD circuit example

There are many factors (e.g.PCB layout, external parts, etc.) that can affect the characteristics.
Therefore, please validate and confirm performance and functionality using lactual applications.

●Selection of External Components

(1) Setting the output L value (step-up DC/DC)

Though a coil is used for the following explanation, a transformer can also be used for the same explanation.
The rated current (ILR) of the output coil (L) is determined by the maximum input current IINMAX

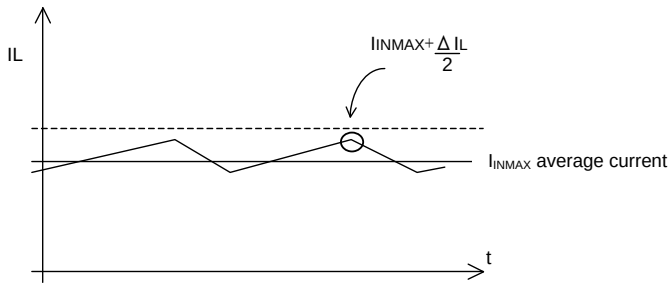


Figure 22. Coil current waveform (step-up DC/DC)

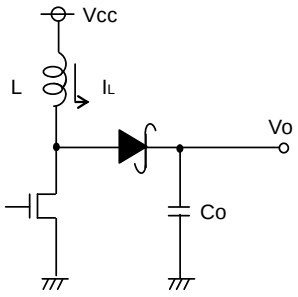


Figure 23. Output application circuit example (step-up DC/DC)

Please ensure that IINMAX + ΔIL / 2 does not reach the rated current ILR. In this case ΔIL can be calculated using the formula below.

$$\Delta IL = \frac{1}{L} Vcc \times \frac{Vo-Vcc}{Vo} \times \frac{1}{f} \quad (A)$$ f: switching frequency

Also, coil L has a variation of about 30% so please allow for a sufficient margin. If the coil current exceeds the coil rated current ILR, this might lead to damages to the IC internal components.

(2) Setting the output capacitor

Select the output capacitor considering the acceptable ripple voltage (Vpp).
The following equation is used to determine the output ripple voltage.

$$\Delta VPP = I_{LMAX} \times R_{ESR} + \frac{1}{fCo} \times \frac{Vcc}{Vo} \times \left(I_{LMAX} - \frac{\Delta I_L}{2}\right) \quad (V) \quad \text{(step-up DC/DC)}$$

(3) Setting the input capacitor

The input capacitor serves to lower the output impedance of the power source connected to the input pin. Increased power supply output impedance can cause input voltage instability and may negatively impact oscillation and ripple rejection characteristics. Therefore, it is necessary to place an input capacitor in close proximity to the Vcc and GND pins.
A low-ESR capacitor with a value between 10μF and 100mΩ is recommended. Selecting a capacitor with a value outside of the recommended range will lead to an excessive ripple voltage being superimposed on the input voltage and may cause the IC to malfunction.
Also, be certain to ascertain the operating temperature, load range and MOSFET conditions for the application in which the capacitor will be used, since capacitor performance is heavily dependent on the application's input power characteristics, substrate wiring and MOSFET gate drain capacity

(4) Setting the output voltage

The output voltage is determined by the equation below. Select a combination of R1 and R2 to obtain the required voltage.
Note that a small resistance value leads to a drop in power efficiency and that a large resistance value leads, due to the error amp output drain current of 0.13μA (typ.), to an increase of the offset voltage

$$Vout = 0.8 \times \frac{R1 + R2}{R2}$$

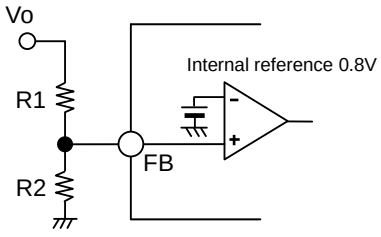


Figure 22. Output voltage setting circuit diagram

(5) Setting the oscillation frequency

The internal oscillation frequency is determined by the resistance value connected to RT.

The setting range is 20kHz to 600kHz. The correlation between the resistance value and the oscillation frequency is as shown in figure 23. A setting outside of the range shown below may cause the switching to stop after which operation is nolonger guaranteed.

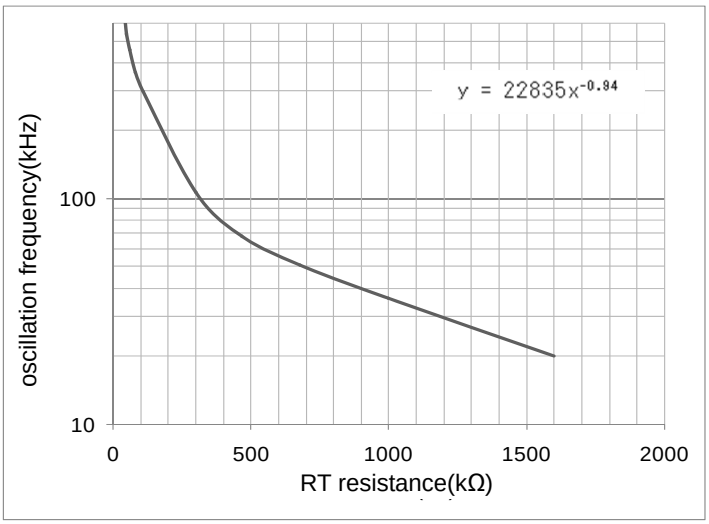


Figure 23. RT resistance vs. oscillation frequency

(6) Soft start delay time

In order to limit the current during startup the soft start pin needs to be connected to a capacitor. By connecting the capacitor output voltage overshoots and inrush currents can be prevented.

The delay time is dependent on the capacitor value connected to the soft start pin and can be calculated using the formula below. (We recommend a capacitor with a value in the range of 0.01 to 0.47μF.)

T_{SS} (typ.) = (C_{SS} X 0.8V (typ.)) / 10μA (typ.) (s) (C_{SS}: Soft Start pin external capacitor)

Note 0.8V: Initial soft start voltage that Vo outputs
10μA: Soft start charge current

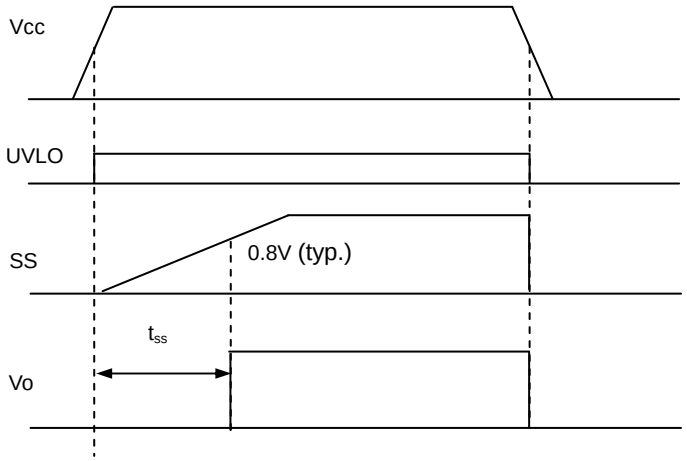


Figure 24. Soft start operating timing chart

(7) Overcurrent protection

The overcurrent protection value is determined by the resistance (Roc) connected between OC and GND and the OC pin

voltage and can be calculated by using the formula below.

$Roc \times Io > Vocth$ ※Vocth = voltage between OC and GND

e.g.) Setting the overcurrent protection at 2A

$$Roc \times 2A = Vocth$$

$$Roc = \frac{Vocth}{2A}$$

Based on that the overcurrent detection threshold =0.2V (typ.)

$$Roc = \frac{0.2}{2A} = 0.1\Omega$$

(3) Setting the phase compensation circuit

Negative feedback stability conditions are as follows:

- At time of unity gain (0dB) the phase delay should be 135° or less. (i.e. the phase margin is 45° or higher)
- As the DC/DC converter application is sampled according to the switching frequency, GBW (frequency at 0-dB gain) of the overall system should be set to 1/10 or less of the switching frequency.

Thus, as the response is determined by the limitation of fc (GBW), it is necessary to increase the switching frequency in order to raise the response.

The phase compensation is set by the capacitors and resistors serially connected to the COMP pin. Achieving stability by using the phase compensation is done by cancelling the 2 poles (error amp pole and power stage pole) of the regulation loop by use of fz1.

$$fp1 = \frac{G_{EA}}{2\pi \times C_1 \times A_{VE}}$$

$$fp2 = \frac{1}{2\pi \times C_O \times R_{LOAD}}$$

$$fz = \frac{1}{2\pi \times C_1 \times R_1}$$

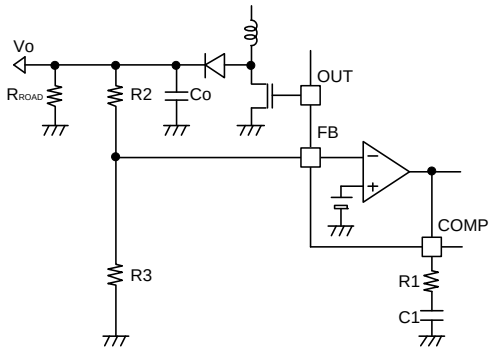
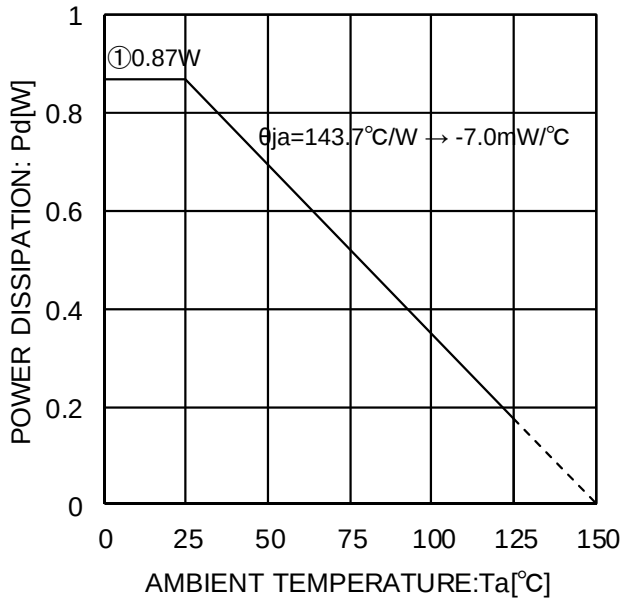


Figure 25. Phase compensation application circuit example

In the formula above, GEA is the error amp transconductance (400μA/V) and AVE is the error amp voltage gain (200V/V) This setting is obtained by using a simplified calculation, therefore, adjustment on the actual application may be required. Also as these characteristics are influenced by the substrate layout, load conditions, etc. verification and confirmation with the actual application at time of mass production design is recommended.

●**Heat dissipation**

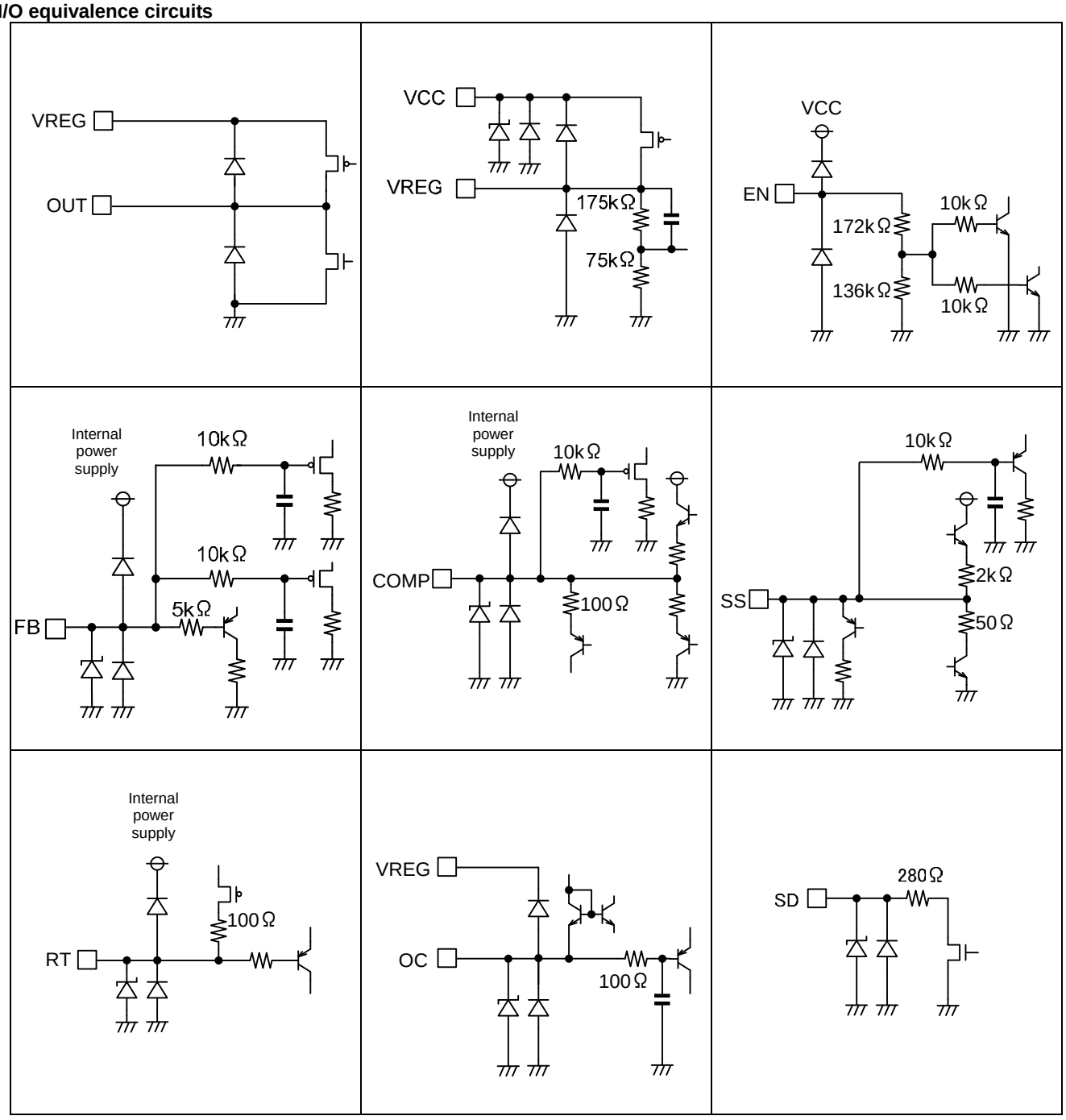


① IC mounted on a ROHM standard board
(70mm × 70mm × 1.6mm glass epoxy board)

Figure 26. SSOP-B16 Power dissipation heat attenuation characteristics

Figure 26. shows the power dissipation and heat attenuation characteristics of the SSOP-B16 package. Even if the ambient temperature Ta is at room temperature (25°C), it can be that the chip (juncture) temperature becomes very high. Therefore, please be sure to operate the IC within the power dissipation range.

● **I/O equivalence circuits**



●Operational Notes

1) Absolute maximum ratings
Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters, can result in destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.

2) Electrical characteristics
The electrical characteristics given in this specification may be influenced by conditions such as temperature, supply voltage and external components. Transient characteristics should be sufficiently verified.

3) GND electric potential
Keep the GND terminal potential at the lowest (minimum) potential under any operating condition. Furthermore, excluding the GND pin, the voltages of all pins should never drop below that of GND.

4) GND wiring pattern
When both a small-signal GND and a high current GND are present, single-point grounding (at the set standard point) is recommended. This must be done in order to separate the small-signal and high current paths and to ensure that voltage changes stemming from the wiring resistance and high current do not cause any voltage change in the small-signal GND. Similarly, care must be taken to avoid any changes in the ground paths of externally connected components.

5) Inter-pin shorting and mounting errors
Ensure that when mounting the IC on the PCB the direction and position are correct. Incorrect mounting may result in damaging the IC. Also, shorts caused by dust entering between the output, input and GND pin may result in damaging the IC.
Note: the overcurrent protection is not activated when the drain-source pin of the external FET is shorted.

6) Operation in strong electromagnetic fields
Use caution when operating in the presence of strong electromagnetic fields, as this may cause the IC to malfunction.

7) Testing on application boards
The IC needs to be discharged after each test process. Because when using an application board for testing, connecting a capacitor to a low-impedance pin may cause stress to the IC. As a protection from static electricity, ensure that the assembly setup is grounded and take sufficient caution with transportation and storage. Also, make sure to turn off the power supply when connecting and disconnecting the inspection equipment.

8) Power dissipation
Should, by any chance, the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The power dissipation value noted in this specification under absolute maximum ratings is the value in case of a 70mm×70mm×1.6mm glass epoxy board. In case this value is exceeded please take appropriate measures such as increasing the board size.

9) Thermal design
The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed for in the thermal design.

10) Vcc pin
Please be sure to insert a capacitor between Vcc and GND. Select the value of the capacitor based on the line of the power smoothing circuit and input pin (Vcc). The capacitance setting may vary according to the application. Therefore its value should be verified in actual application with a sufficient margin in place. It is recommended to use a capacitor with good voltage and temperature characteristics.

11) Capacitor connected to the VREG pin
In order to prevent oscillation, a capacitor needs to be placed between the output pin and GND pin. It is recommended to use a capacitor with a capacitance of 4.7μF or higher. Electrolytic, tantalum and ceramic capacitors can be used. When selecting the capacitor ensure that the capacitance of 4.7μF or higher is maintained at the intended applied voltage and temperature range. Due to changes in temperature the capacitor's capacitance can fluctuate possibly resulting in oscillation.
When selecting a ceramic type capacitor, we recommend using X5R, X7R or better with excellent temperature and DC-biasing characteristics and high voltage tolerance.
Also, in case of rapidly changing input voltage and load current, select the capacitance in accordance with verifying that the actual application meets with the required specification.

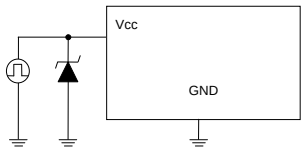
12) EN pin
In case of connecting a resistor to the EN pin, as shown in figures 19 to 21, please ensure a setting in which the EN pin voltage is higher than the ON voltage (2.7V).

13) SD pin
In case of using a SD pin, as shown in figure 21., please sufficiently consider the operating voltage of the external PchMOS when setting the resistance value.

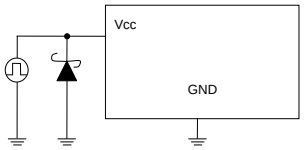
14) Thermal shutdown (TSD)
This IC incorporates an integrated thermal shutdown circuit to prevent heat damage to the IC. Normal operation should be within the power dissipation rating, if however the rating is exceeded for a continued period, the junction temperature (Tj) will rise and the TSD circuit will be activated and turn all output pins OFF. After the Tj falls below the TSD threshold the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

15) Based on the application the Vcc and other pin voltages might be reversed, possibly resulting in circuit internal damage or damage to components. For example, while the external capacitor is charged, Vcc shorts to GND. Using reverse polarity diodes in series or a bypass diode between all pins and the Vcc pin is therefore recommended.

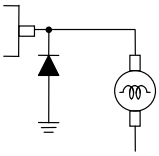
16) Applying a positive surge to the Vcc pin
In case surges exceeding 35V will be applied to the Vcc pin, please place a power zener diode between Vcc and GND as shown in the figure below.



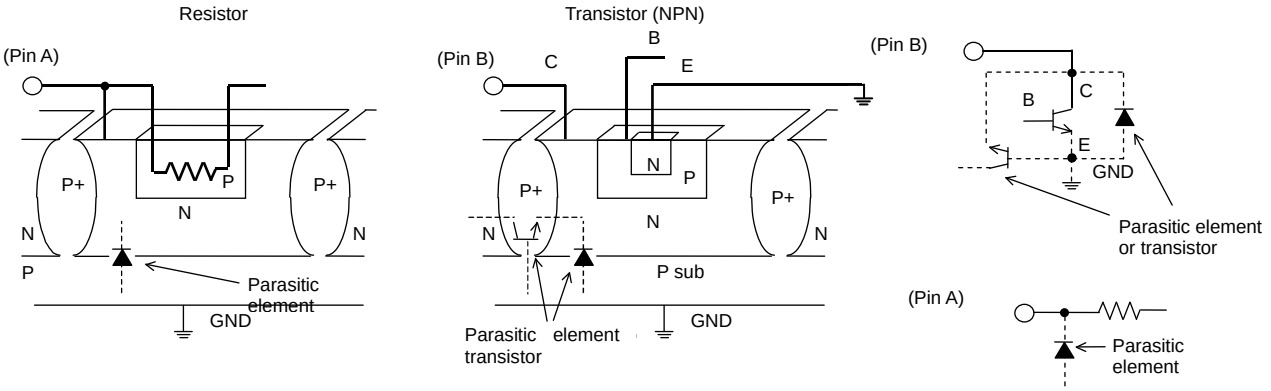
17) Applying a negative surge to the Vcc pin
If the possibility exists that the Vcc voltage will be lower than that of the GND pin, please place a Shottky diode between Vcc and GND as shown in the figure below.



18) Placing a protection diode
If the possibility exists that a large inductive load is connected to the output pin resulting in back-EMF at time of startup and shutdown, a protection diode should be place as shown in the figure below.



19) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, in case a resistor and a transistor are connected to the pins as shown in the figure below then:
○ The P/N junction functions as a parasitic diode when GND > pin A for the resistor, or GND > pin B for the transistor.
○ Also, when GND > pin B for the transistor (NPN), the parasitic diode described above combines with the N layer of the other adjacent elements to operate as a parasitic NPN transistor.
Parasitic diodes inevitably occur in the structure of the IC. Their influence can result in mutual interference between circuits and can cause malfunctions and, in turn, physical damage to or destruction of the chip. Therefore, the input pin voltage should not be lower than the (P substrate) GND in order to prevent the parasitic diodes to conduct.



Note concerning this document
The Japanese version of this document is the official specification. This translation should be seen as a reference to aid reading the official specification. In case of any discrepancies between the two versions, the offical version always takes precedence.

●**Ordering Information**

B D 9 0 3 1 F V - C	E 2

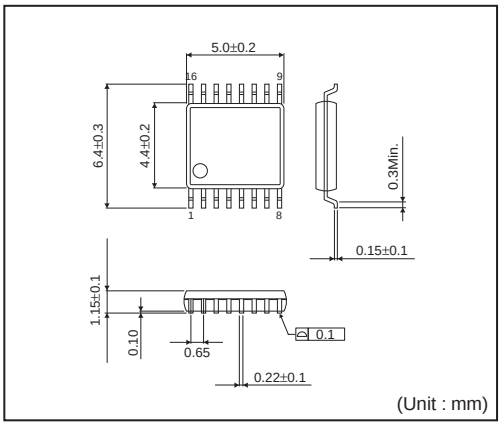
Part Number

Package
FV: SSOP-B16

Taping
E2: reel-wound embossed tamping

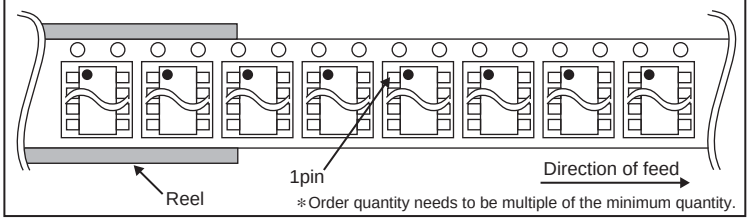
●**Physical Dimension Tape and Reel Information**

SSOP-B16



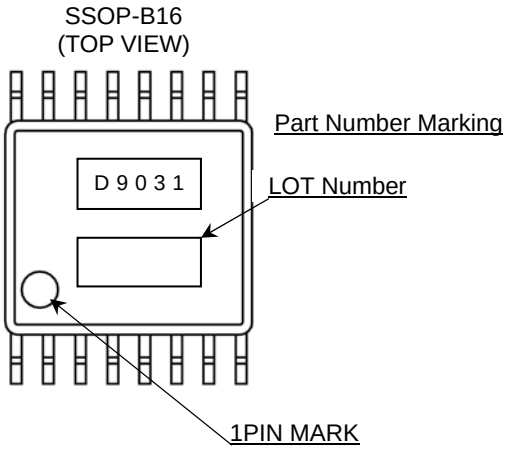
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●**Marking Diagram**



●**Revision History**

Date	Revision	Changes
27/MAR/2012	001	Initial draft
05/NOV/2012	002	P.10 Change Timing chart and the explanation of detection time and release time. P.11 Add the overvoltage protection (OVP) Timing chart and the under voltage protection (UVP) Timing chart

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CLASSⅢ	CLASSⅢ	CLASSⅡb	Ⅲ類
CLASSⅣ		CLASSⅢ	

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   ③潮風、Cl_2、H_2S、NH_3、SO_2、NO_2 等の腐食性ガスの多い場所でのご使用
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