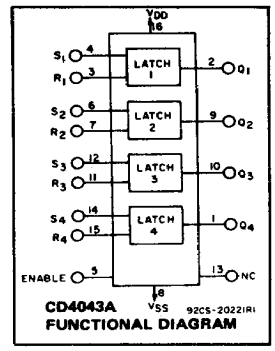
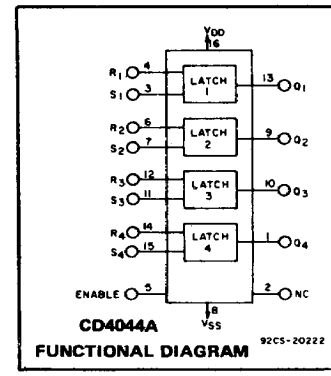
CMOS Quad 3-State R/S Latches

Quad NOR R/S Latch – CD4043A
Quad NAND R/S Latch – CD4044A

The RCA-CD4043A types are quad cross-coupled 3-state CMOS NOR latches and the CD4044A types are quad cross-coupled 3-state CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs. The logic operation of the latches is summarized in the truth table shown in Fig. 1.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).





Applications:

- **Holding register in multi-register system**
- **Four bits of independent storage with output ENABLE**
- **Strobed register**
- **General digital logic**

Features:

- **3-Level outputs with common output ENABLE**
- **Separate SET and RESET inputs for each latch**
- **NOR and NAND configurations**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
  PACKAGE TYPE E . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  (Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
  FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
  FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
  FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
  FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package Temperature Range	–	3	12	3	12	V
Set or Reset Pulse Width, t_W	5 10	200 100	– –	225 110	– –	ns

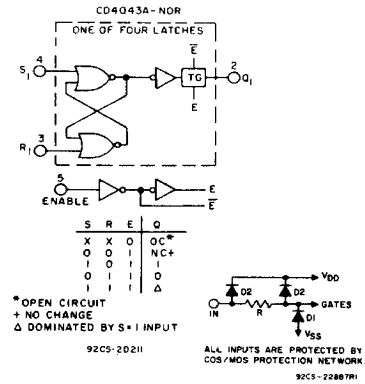


Fig. 1 – Logic diagrams and truth tables.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.005	2	120	20	0.02	20	280	
	–	–	15	25	0.25	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.;								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	–	5	0.25	0.5	0.2	0.19	0.12	0.5	0.1	0.09	mA
	0.5	–	10	0.61	1	0.5	0.35	0.3	1	0.25	0.22	
p-Channel (Source), I_DP Min.	4.5	–	5	-0.22	-0.5	-0.175	-0.12	-0.11	-0.5	-0.09	-0.08	
	9.5	–	10	-0.5	-1	-0.4	-0.28	-0.24	-1	-0.2	-0.18	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$; Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS D, F, K, H Packages Typ.	LIMITS D, F, K, H Packages Max.	LIMITS E Package Typ.	LIMITS E Package Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} SET or RESET to Q	5	175	350	175	400	ns
	10	75	175	75	200	
3-State Propagation Delay Time: ENABLE to Q t_{PHZ}, t_{PZH}	5	100	200	100	200	ns
	10	50	100	50	100	
t_{PLZ}, t_{PZL}	5	80	160	80	160	ns
	10	40	80	40	80	
Transition Time: t_{THL}, t_{PLH}	5	100	200	100	250	ns
	10	50	100	50	125	
Minimum SET or RESET Pulse Width, t_W	5	80	200	80	225	ns
	10	40	100	40	110	
Average Input Capacitance, C_I (Any Input)	–	5	–	5	–	pF

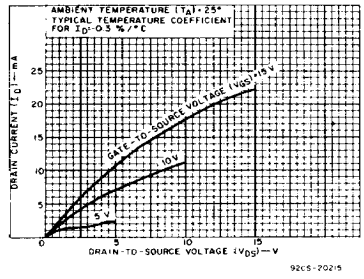


Fig. 2 — Typical output n-channel drain characteristics.

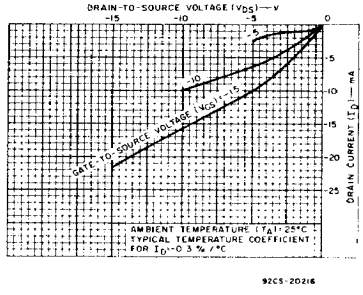


Fig. 3 — Typical output p-channel drain characteristics.

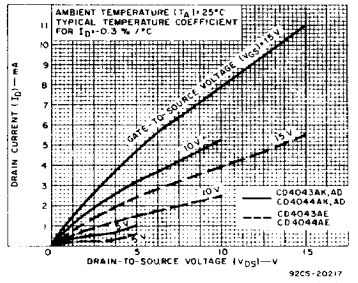


Fig. 4 — Minimum n-channel drain characteristics.

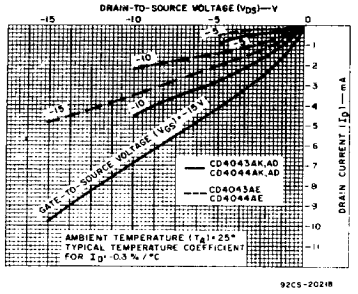


Fig. 5 — Minimum p-channel drain characteristics.

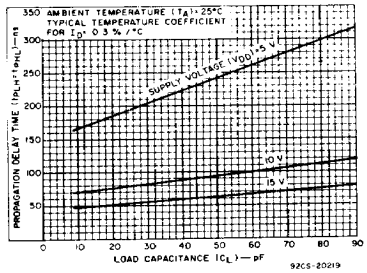


Fig. 6 — Typical propagation delay time vs. C_L.

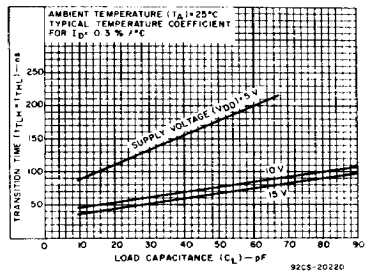


Fig. 7 — Typical transition time vs. C_L.

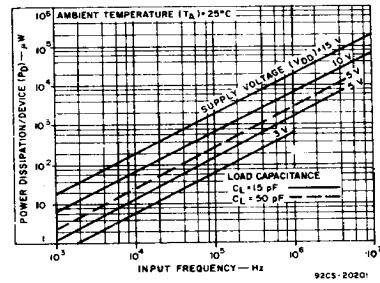


Fig. 8 — Typical dissipation characteristics.

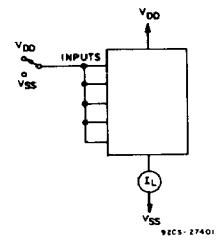


Fig. 9 — Quiescent device current test circuit.

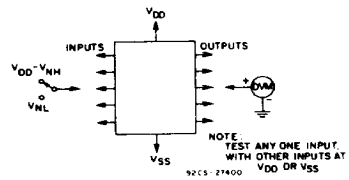


Fig. 10 — Noise immunity test circuit.

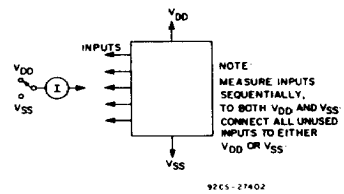


Fig. 11 — Input leakage current test circuit.

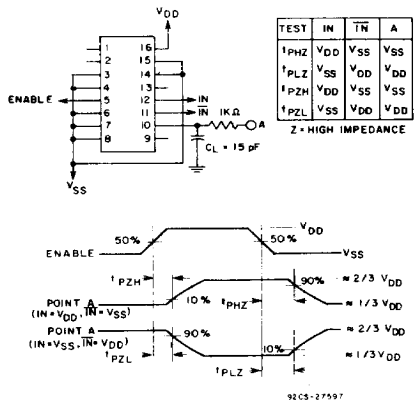


Fig. 12 — ENABLE propagation delay time test circuit and waveforms.

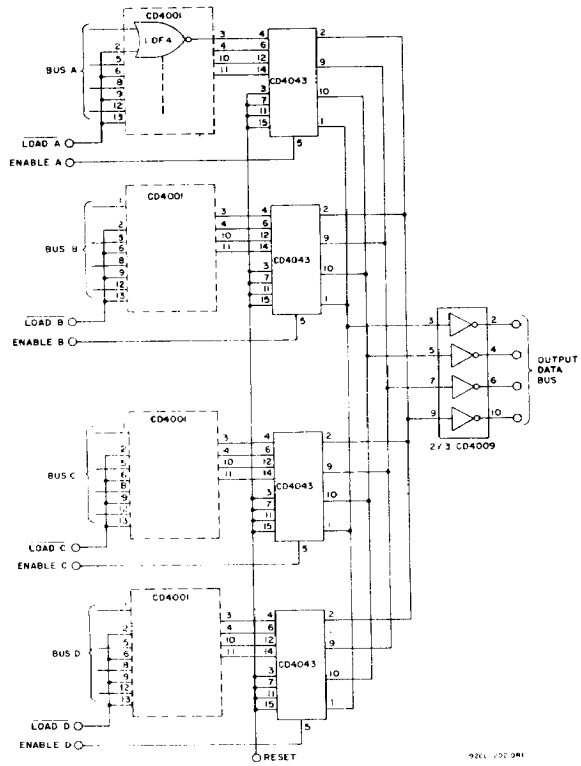


Fig. 14 — Multiple bus storage.

APPLICATIONS

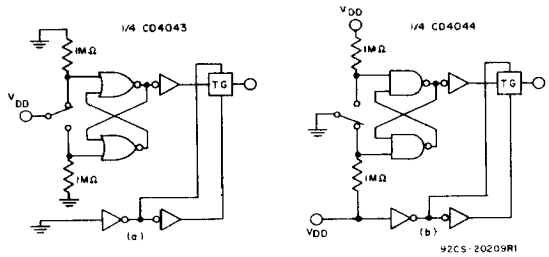


Fig. 13 — Switch bounce eliminator.