

DUAL DECADE COUNTER

- **HIGH SPEED**
 $t_{PD} = 13 \text{ ns (Typ)}$ at $V_{CC} = 5V$
- **LOW POWER DISSIPATION**
 $I_{CC} = 4 \mu A \text{ (MAX.)}$ at $T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 10 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = |I_{OL}| = 4 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- **PIN AND FUNCTION COMPATIBLE**
 WITH 54/74LS390

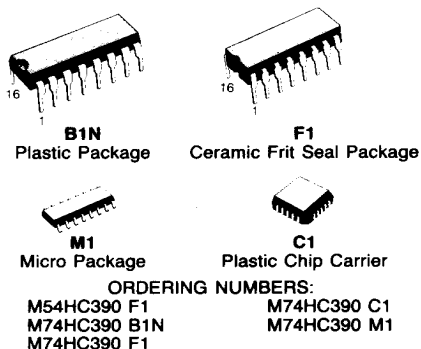
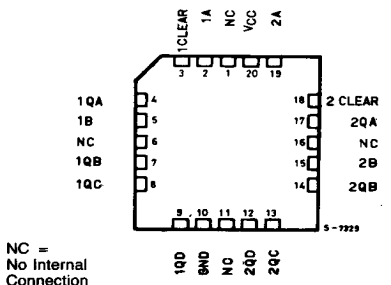
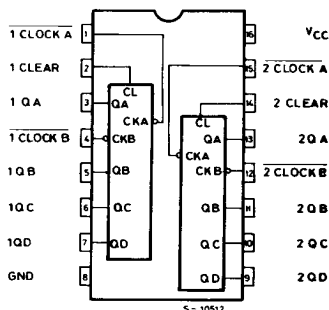
DESCRIPTION

The M54/74HC390 is a high speed CMOS DUAL DECADE COUNTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This dual decade counter contains two independent ripple carry counters. Each counter is composed of a divide-by-two and divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual biquinary, or various combinations up to a single divide-by-100 counter.

Each 4-bit counter is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set low all four bits of each counter are set to low. This enables count truncation and allows the implementation of divide-by-N counter configurations.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

**PIN CONNECTION (top view)**

TRUTH TABLE

COUNT	OUTPUTS							
	BCD COUNT *				BI-QUINARY **			
	QD	QC	QB	QA	QA	QD	QC	QB
0	L	L	L	L	L	L	L	L
1	L	L	L	H	L	L	L	H
2	L	L	H	L	L	L	H	L
3	L	L	H	H	L	L	H	H
4	L	H	L	L	L	H	L	L
5	L	H	L	H	H	L	L	L
6	L	H	H	L	H	L	L	H
7	L	H	H	H	H	L	H	L
8	H	L	L	L	H	L	H	H
9	H	L	L	H	H	H	L	L

INPUTS			OUTPUTS			
CLOCK A	CLOCK B	CLEAR	QA	QB	QC	QD
X	X	H	L	L	L	L
$\overline{\text{L}}$	X	L	BINARY COUNT UP			
X	$\overline{\text{L}}$	L	QUINARY COUNT UP			

Note: * Output QA is connected to input CLOCK B for BCD count.
 ** Output QD is connected to input CLOCK A for bi-quinary count.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	- 65 to 150	°C

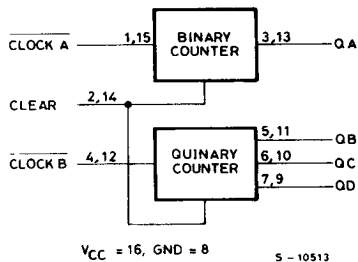
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: $\approx$ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

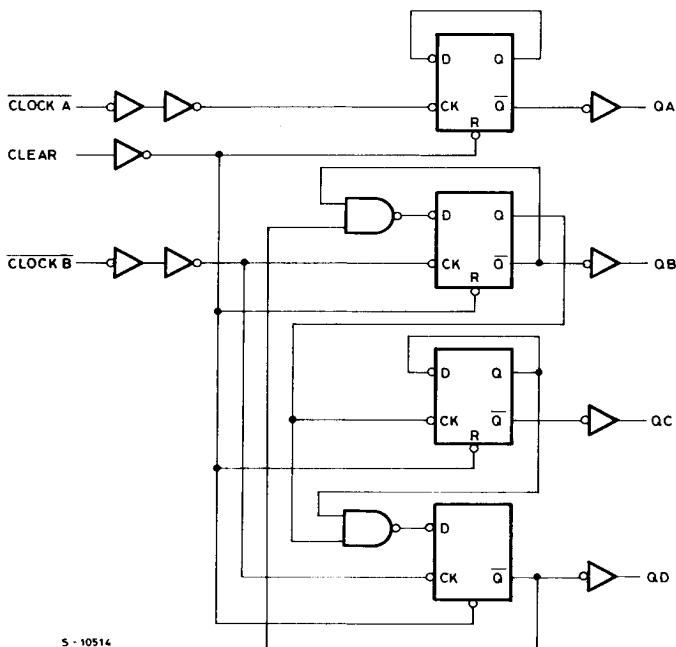
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

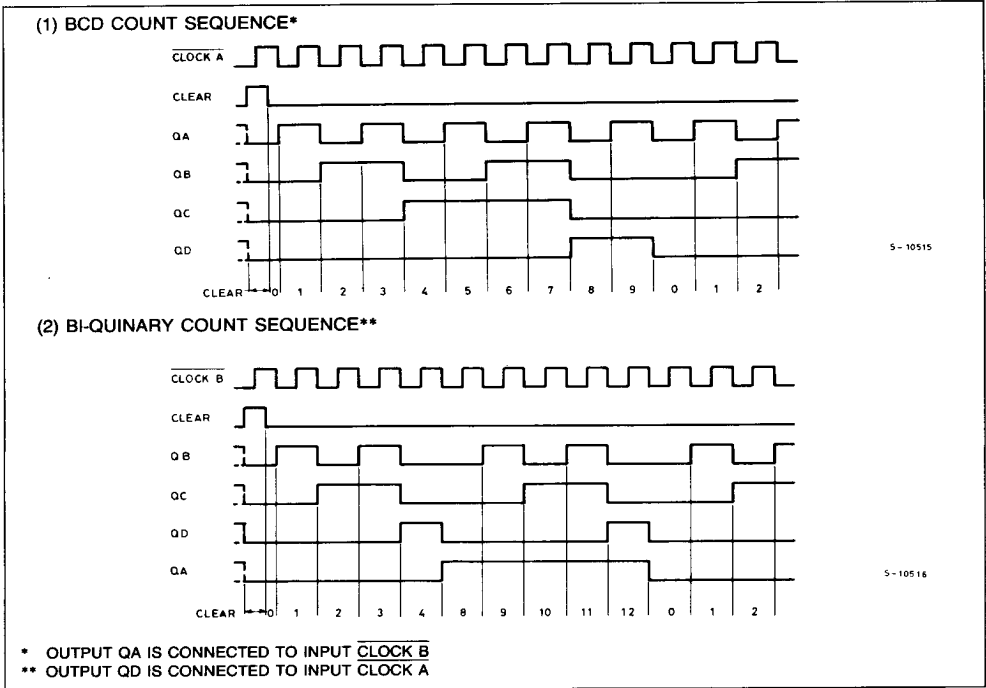
BLOCK DIAGRAM



LOGIC DIAGRAM



TIMING CHART



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC}	Test Condition		T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V _{OH}	High Level Output Voltage	2.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH} or V _{IL}	— 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	— 4.0 mA	4.18	4.31	—	4.13	—	4.10	—	V
		4.5		— 5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
		6.0										
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
V _{OL}	Low Level Output Voltage	4.5	V _{IH} or V _{IL}	4.0 mA	—	0.17	0.26	—	0.33	—	0.40	V
		6.0			—	0.18	0.26	—	0.33	—	0.40	
		6.0			—			—		—		

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND	—	—	±0.1	—	±1.0	—	±1.0	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND	—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t _{TLH} t _{THL}	Output Transition Time	—	4	8	ns
t _{PLH} t _{PHL}	Propagation Delay Time (A - QA)	—	13	21	ns
t _{PLH} t _{PHL}	Propagation Delay Time (B - QB, QD)	—	14	23	ns
t _{PLH} t _{PHL}	Propagation Delay Time (B - QC)	—	21	33	ns
t _{PHL}	Propagation Delay Time (CL - Q)	—	16	26	ns
f _{MAX}	Maximum Clock Frequency (CLOCK A - QA)	35	64	—	MHz
f _{MAX}	Maximum Clock Frequency (CLOCK B - QB)	30	45	—	MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{TLH} t _{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK A - QA)	2.0 4.5 6.0		— — —	64 16 14	130 26 22	— — —	165 33 28		195 39 33	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK B (QB, QN))	2.0 4.5 6.0		— — —	68 17 14	135 27 23	— — —	170 34 29		205 41 35	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK B - QC)	2.0 4.5 6.0		— — —	96 24 20	185 37 31	— — —	230 46 39		280 56 48	ns
t _{PHL}	Propagation Delay Time (CLEAR - Qn)	2.0 4.5 6.0		— — —	76 19 16	150 30 26	— — —	190 38 33		225 45 38	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

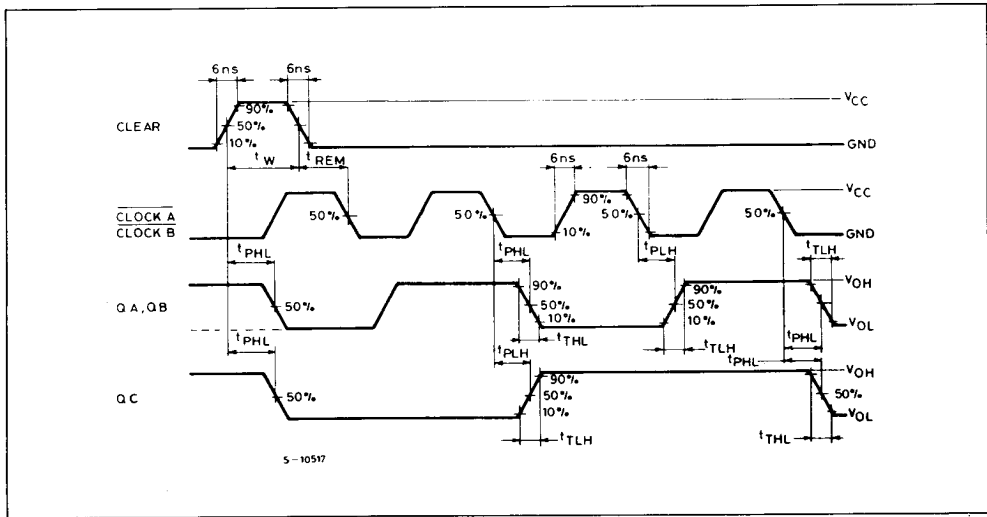
Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}	Maximum Clock Frequency (CLOCK A - QA)	2.0 4.5 6.0		6.4 32 28	15 58 68	—	5.2 26 31	—	4.2 21 25	—	MHz
f _{MAX}	Maximum Clock Frequency (CLOCK B - QB)	2.0 4.5 6.0		5.4 27 32	10 41 48	—	4.4 22 26	—	3.8 19 22	—	MHz
t _{W(H)} t _{W(L)}	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t _{W(L)}	Minimum Pulse Width (CLEAR)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t _{REM}	Minimum Removal Time	2.0 4.5 6.0		— — —	5 0 0	25 5 5	— — —	30 6 6	— — —	40 8 7	ns
C _{IN}	Input Capacitance			—	5	10	—	10		10	pF
C _{PD} (*)	Power Dissipation Capacitance			—	44	—	—	—	—	—	pF

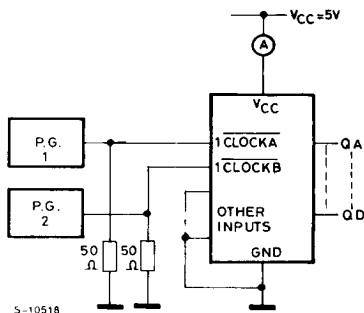
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation:

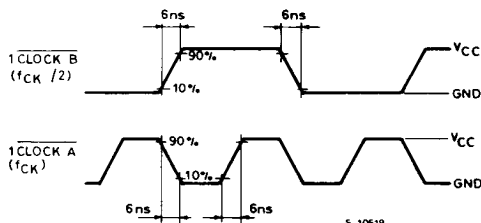
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)

INPUT WAVEFORM



WHEN THE OUTPUTS DRIVE CAPACITIVE LOAD, TOTAL CURRENT CONSUMPTION IS TO BE A SUM OF THE VALUE CALCULATED FROM C_{PD} AND ΔI_{CC} OBTAINED FROM THE FOLLOWING FORMULA.

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \frac{C_a}{2} + \frac{f_{CK}}{2} \cdot V_{CC} \left(\frac{2C_b}{5} + \frac{C_c}{5} + \frac{C_d}{5} \right)$$

$C_a \sim C_d$ ARE THE CAPACITANCE AT QA ~ QD OUTPUT.