AFBR-5972EZ, AFBR-5972BZ

Compact 650nm Transceiver with Compact Versatile Link Connector for Fast Ethernet over POF

Data Sheet

Description

The AFBR-5972xZ transceivers provide system designers with the ability to implement Fast Ethernet (100 Mbps) over standard bandwidth 0.5±0.05 NA POF. The new compact Versatile-Link duplex connector is compatible with existing simplex Versatile-Link connectors and features a very compact design with a form factor similar to the UTP connector. To enable easy visual differentiation the AFBR-5972EZ uses standard black port color while the AFBR-5972BZ has a blue colored port. The AFBR-5972xZ transceivers are lead free and compliant with RoHS.

Transmitter

The transmitter contains a 650nm LED with a driver IC. The LED driver operates at 3.3V. It receives an LVDS electrical input, and converts it into a modulated current driving the LED. IC and LED are packaged in an optical subassembly, part of the transmitter section. The optical subassembly couples the output optical power efficiently into POF fiber.

Receiver

The receiver utilizes an amplifier/quantizer IC with an integrated double photodiode. The IC is packaged in an optical sub-assembly, part of the receiver section. This optical subassembly couples the optical power efficiently from POF fiber to the receiving photodiode. The integrated IC operates at 3.3V and converts the photocurrent into LVDS electrical output.

Package

The transceiver package consists of three basic elements; two opto-electical subassemblies and the housing as illustrated in the block diagrams in figure 1. The package outline drawing and pin-outs are shown in figures 2 and 7.

Features

- Fast Ethernet communications over POF
- Link lengths up to 50m POF (NA0.5) or 70m POF (NA0.3)
- Compact foot print
- 3.3V operation
- Data rates up to 250 MBd
- LVDS Input and Output data connections
- Analog RSSI (receiver signal strength) monitor output
- Temperature range -40°C to 85°C

Applications

- Factory automation at Fast Ethernet speeds
- Fast Ethernet networking over POF

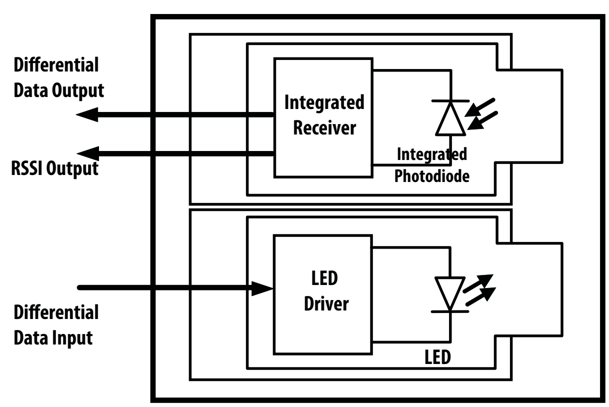


Figure 1. Block diagram

The opto-electrical subassemblies utilize a high volume assembly process together with low cost lens elements which result in a cost effective building block. It consists of the active III-V devices, IC chips and various surface mounted passive components.

There are eight signal pins, four EMI shield solder posts and two mounting posts, which exit the bottom of the housing. The solder posts are isolated from the internal circuit of the transceiver and are to be connected to chassis ground. The mounting posts are to provide mechanical strength to hold the transceiver to the application board.

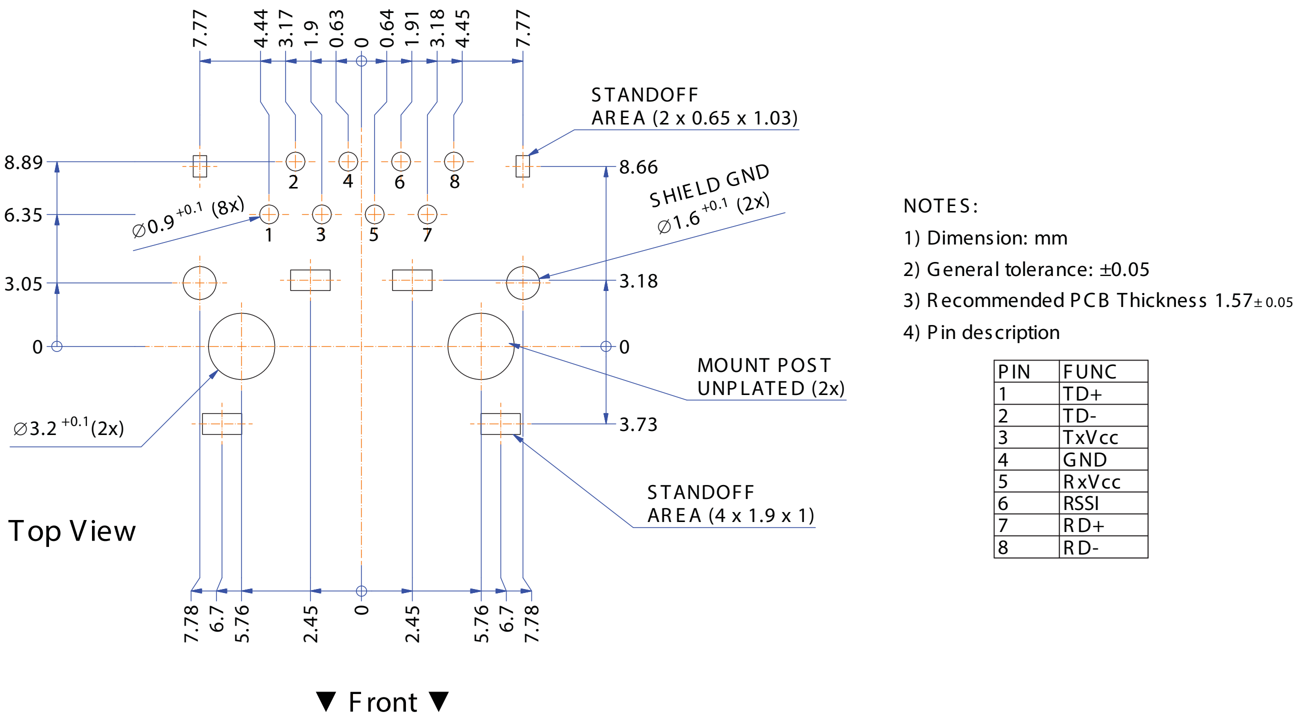


Figure 2. PCB footprint and pinout diagram

Pin Description

Pin 1	TData+:	Transmitter data in positive. This input is an LVDS compatible differential line.
Pin 2	TData-:	Transmitter data in negative. This input is an LVDS compatible differential line.
Pin 3	TxVCC:	Transmitter power supply pin. Provide +3.3 V DC via a transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the TxVcc pin.
Pin 4	GND:	Common ground pin. Directly connect this pin to the signal ground plane of the host board.
Pin 5	RxVCC:	Receiver power supply pin. Provide +3.3 V DC via a receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the RxVcc pin.
Pin 6	RSSI:	Receiver signal strength pin, delivers a DC output current proportional to the average incoming light power.
Pin 7	RData+:	Receiver data out positive. This data line is an LVDS compatible differential output line which should be properly terminated. In absence of an optical input signal, this line is squelched.
Pin 8	RData-:	Receiver data out negative. This data line is an LVDS compatible differential output line which should be properly terminated. In absence of an optical input signal, this line (same as RData+) is squelched.
Shield	Shield	This is to be connected to the equipment chassis ground.

Application Circuit

The recommended application circuitry is shown in figure 3

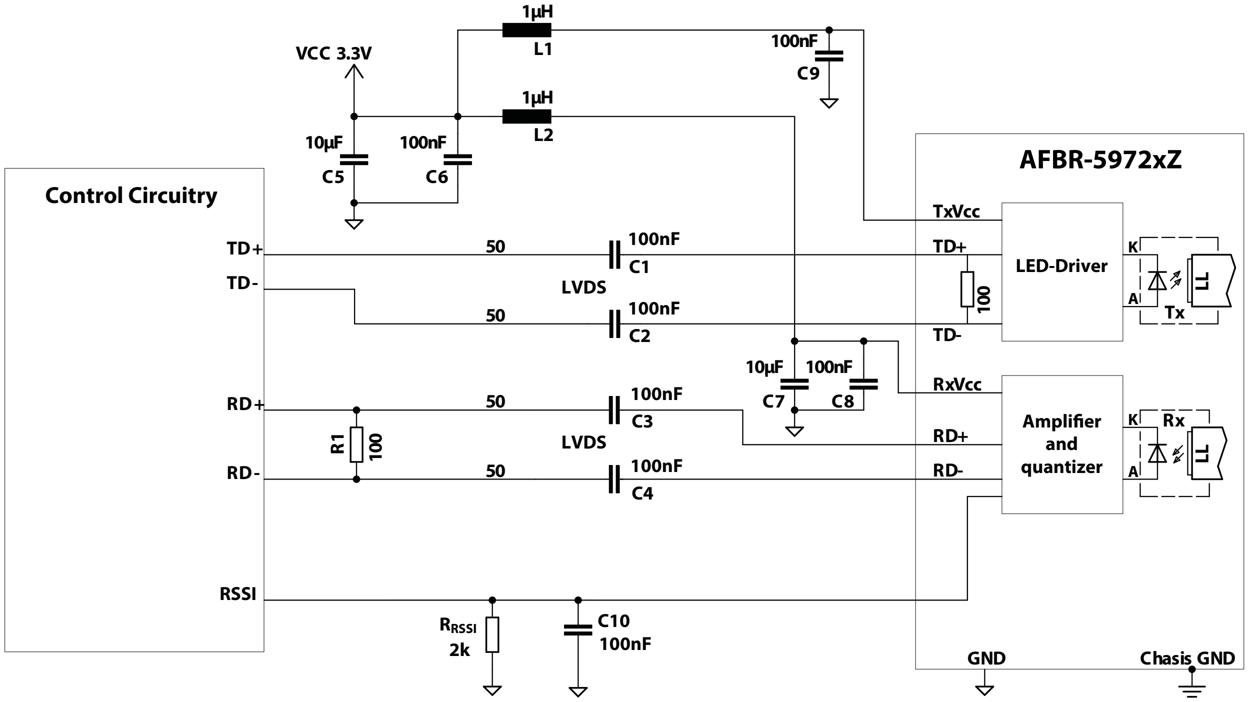


Figure 3. Recommended application circuitry

Board Layout – Decoupling Circuit and Ground Planes

It is important to take care of the layout of the application circuitry to achieve optimum performance of the transceiver. A power supply decoupling circuit is recommended to filter out noise, to assure optimal product performance. It is further recommended that a contiguous signal ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. It is also recommended that the shield posts be connected to the chassis ground to provide optimum EMI, ESD and EMS performance. This recommendation is in keeping with good high frequency board layout practices.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic discharge (ESD) to the electrical Pins	ESD22-A114	Withstands up to 2000V HBM applied between the electrical pins.
Immunity	Variation of IEC 61000-4-3	Typically shows no measurable effect from a 15V/m field swept from 8MHz to 1GHz applied to the transceiver when mounted on a circuit board without chassis enclosure.
Eye Safety	EN 60825-1:52007	Laser class 1 product (LED radiation only). TÜV certificate: R 50217706. CAUTION – Use of controls or adjustments of performance or procedures other than those specified herein may result in hazardous radiation exposure
Component recognition	Underwriter Laboratories	UL File #: E173874

Transceiver diagnostics timing characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Time to initialize	t_init		5	ms	Note 1, figure 4
Assert time	t_ass		100	µs	Notes 2, 4
De-assert time	t_deass		100	µs	Notes 3, 4

Notes:
1. Time from power on to when the modulated optical output rises above 90% of nominal.
2. Time from valid optical signal to assertion.
3. Time from loss of optical signal to de-assertion.
4. There is an internal SD (signal detect) signal which is directly related to assert (PA) and de-assert (PD) levels as specified in table "Receiver Optical Characteristics". There is no direct access to the SD signal, however the Rx data outputs will squelch and the RSSI will switch off, once the optical input power falls below PD. Furthermore, the Rx data and RSSI outputs will be activated, once the optical input power exceeds PA

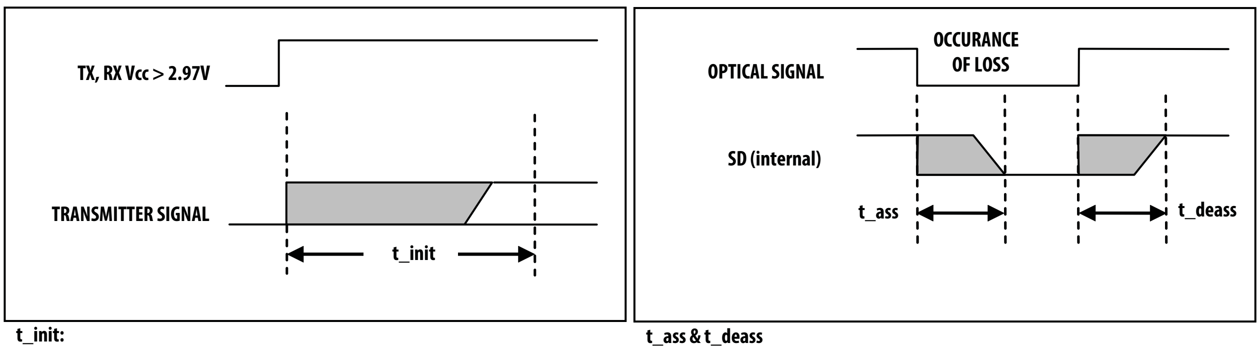


Figure 4. Transceiver timing diagrams

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation. all other parameters having values within the recommended operation conditions. It should not be assumed that limiting values of more than one parameter can be applied to the products at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_S	-40	+100	°C	
Case Operating Temperature	T_C	-40	+85	°C	Note 1, 2
Lead Soldering Temperature	T_{SOLD}		260	°C	Note3
Lead Soldering Time	t_{SOLD}		10	s	Note 3
Supply Voltage	V_{CC}	-0.5	4.0	V	
Data Input Voltage	V_I	-0.5	V_{CC}	V	

Notes:
1. Operating the product outside the maximum rated case operating temperature range will compromise its reliability and may damage the product.
2. The temperature is measured using a thermocouple connected to the hottest position of the housing.
3. The transceiver is Pb-free wave solderable.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Case Operating Temperature	T_C	-40		+85	°C	Note 1, 2
Supply Voltage	V_{CC}	2.97	3.30	3.63	V	
Receiver Output Termination Impedance	R_L		100		Ω	
Signaling Rate (Fast Ethernet)	B_{FE}		125		MBd	4B/5B, note 3
Signaling Rate (general)	B_G	10		250	MBd	Note 4

Notes:
1. The temperature is measured using a thermocouple connected to the housing.
2. Electrical and optical specifications of the product are guaranteed across recommended case operating temperature range only.
3. Ethernet auto-negotiation pulses are not supported.
4. Min. signaling rate for bi-phase coded signal. Max. signaling rate for 8B/10B coded signal (verified by PRBS 27-1 test pattern).

Transceiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Current	I_{CC}		50	65	mA	
Power Dissipation	P_{DISS}		165	240	mW	
Power Supply Noise Immunity	PS_{NI}	50			mV	Peak to peak, Note 1
Tx Differential Input Voltage (pk-pk)	V_{DI}	200		1800	mV	
Tx Input Voltage Range to Circuit Common	V_I	0		2.4	V	

Notes:
1. Frequencies from 0.1MHz to 100MHz, sine wave.

Transmitter Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Average Launched Power (1mm POF, NA=0.5)	$P_{O\text{-}POF}$	-10.0	-6.5	-3.0	dBm	Note 1
Extinction Ratio	EXT	10			dB	Note 1
Central Wavelength	λ_C	635	650	675	nm	Note 1, 2
Spectrum RMS	$\Delta\lambda$			17	nm	Note 2, 3
Optical Rise Time (10%-90%)	t_R		1.7	2	ns	Note 1
Optical Fall Time (90%-10%)	t_F		1.6	2	ns	Note 1
Duty Cycle Distortion Contributed by the Transmitter	DCD			1	ns	Peak to peak, note 1
Data Dependent Jitter	J_{DD}			0.6	ns	Note 1
Random Jitter Contributed by the Transmitter	J_R			0.76	ns	Peak to peak, notes 1, 4
Overshoot	OS		7	25	%	Note 1

Notes:
1. Measured at the end of 1 meter plastic optical fiber with a PRBS 2-7 sequence, running at 250 MBd data rate
2. Central wavelength is defined as:

$$\lambda_c = \frac{\sum_{i=1}^{N} P_i \lambda_i}{\sum_{i=1}^{N} P_i}$$

Ref: EIA/TIA standard FOTP-127/6.1, 1991

3. Spectrum RMS is defined as:

$$\Delta\lambda = \left[\left(\frac{\sum_{i=1}^{N} P_i \lambda_i^2}{\sum_{i=1}^{N} P_i}\right) - \lambda_c^2\right]^{\frac{1}{2}}$$

Ref: EIA/TIA standard FOTP-127/6.3, 1991

4. Based on BER=2.5×10^{-10}

Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Output Voltage (pk-pk)	V_{DO}	500		900	mV	Note 1
Output Common Mode Voltage	V_{OCM}		1.2		V	Note 1
Data Output Rise Time (10%-90%)	t_R		0.8	1.5	ns	Note 1
Data Output Fall Time (90%-10%)	t_F		0.8	1.5	ns	Note 1
Duty Cycle Distortion	DCD			1.0	ns	Notes 1, 2
Data Dependent Jitter	J_{DD}			1.2	ns	Notes1, 2
Random Jitter	J_R			2.14	ns	Peak to peak, notes 1, 2, 3
RSSI Output Responsivity	I_{RSSI}/P_{IN}		0.45		A/W	Fig. 5, 6
Voltage at RSSI Output	V_{RSSI}	0		V_{CC}-1.5	V	

Notes:
1. Characterized with LVDS termination (100 Ω)
2. Contributed by Rx only.
3. Based on BER=2.5×10^{-10}

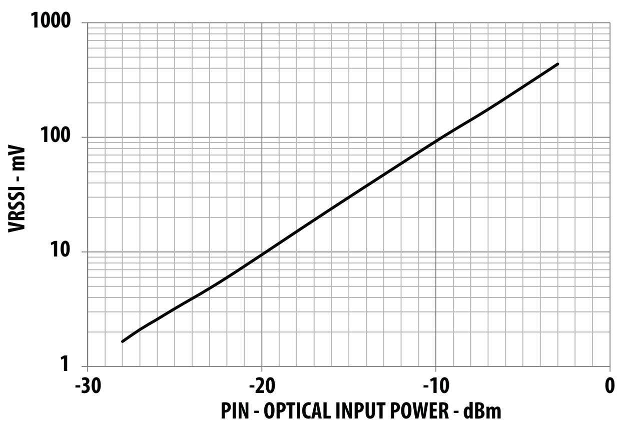


Figure 5. Typical RSSI output voltage across R_{RSSI} = 2 kΩ

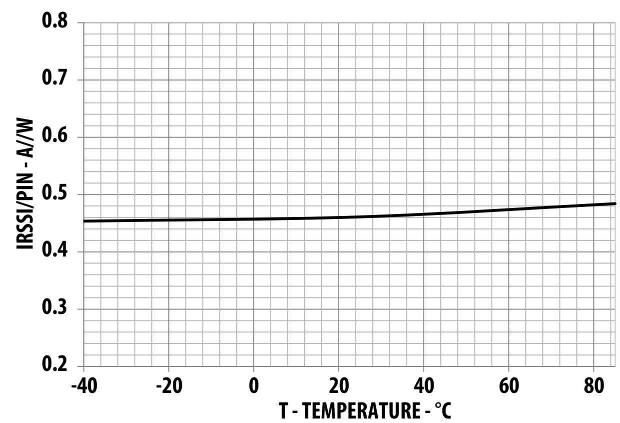


Figure 6. Typical responsivity vs. temperature

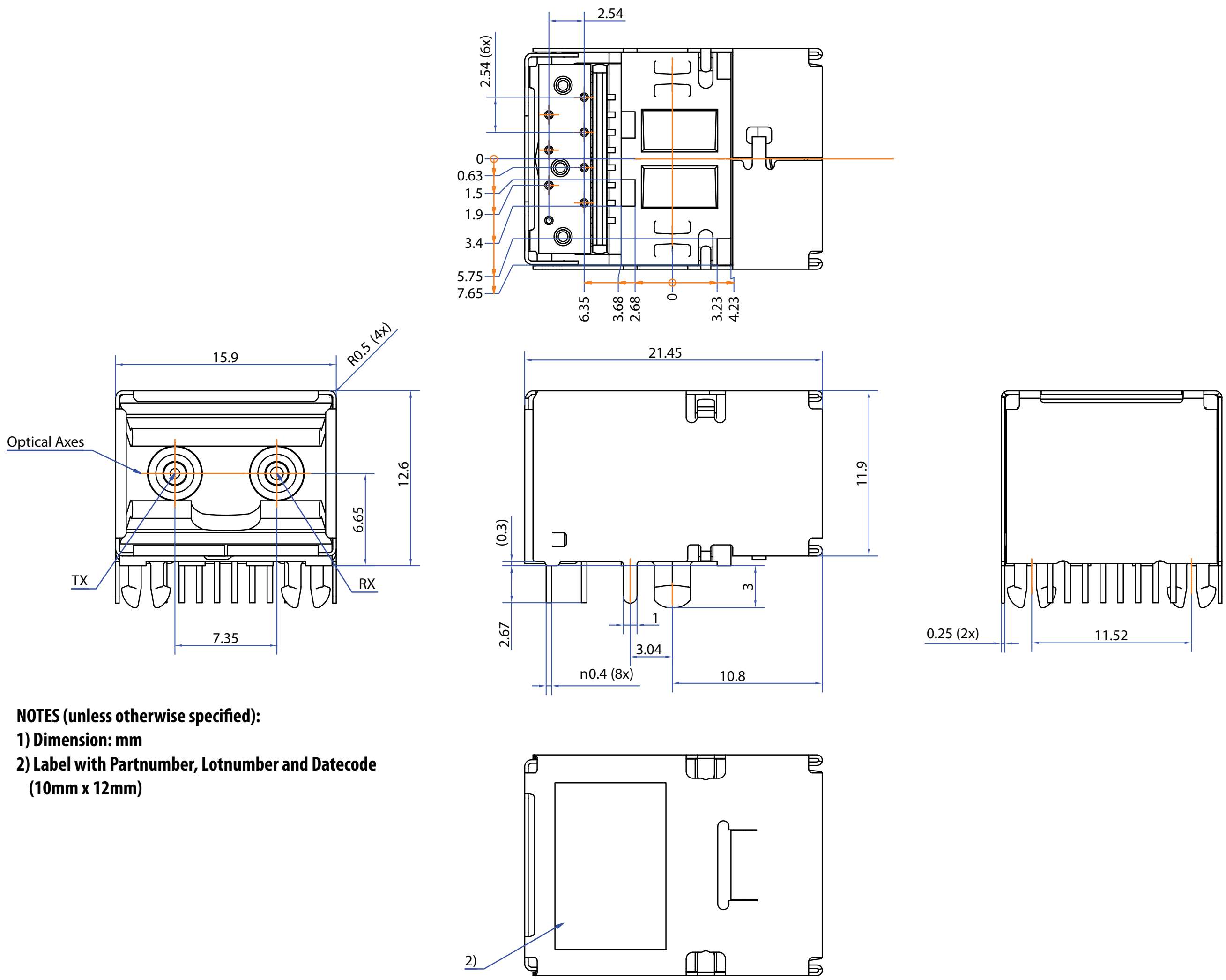
Notes:
RSSI is actually a current output, providing an output current proportional to the coupled optical power. To provide a suitable monitoring voltage, choose the value of R_{RSSI} according to the particular optical power situation. For the characterization of the RSSI output responsivity, as shown in figure 5, a 2 kΩ resistor was used. The lower the power, the higher the resistor value should be. However, do not override the max. limit of V_{RSSI}.

Receiver Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unstressed receiver sensitivity, (POF) for Fast Ethernet data rate (125 MBd)	$CSEN_{125}$	-26			dBm	Note 1
Unstressed receiver sensitivity, (POF) for data rate 250 Mbd	$CSEN_{250}$	-22			dBm	Note 2
Input Optical Power Maximum, (POF)	P_{IN-MAX}			-3.0	dBm	Notes 1, 3
Operating Wavelength	λ_C	635	650	675	nm	
Assert input power level	PA		-29.5		dBm	Notes 4, 5
De-assert input power level	PD		-31		dBm	Notes 4, 5
Hysteresis between assert and de-assert	PA-PD		1.0		dBm	Note 5

Notes:
1. Measured with PRBS 2^7-1 sequence at 125 MBd, BER < 2.5×10^{-10}
2. Measured with PRBS 2^7-1 sequence at 250 MBd, BER < 2.5×10^{-10}
3. Input Optical Power Maximum is defined as the maximum optical modulation amplitude where the receiver duty cycle distortion reaches ±1 ns.
4. Asserted and De-asserted levels are indicated as dB below unstressed receiver sensitivity level for POF.
5. There is an internal SD (signal detect) signal which is directly related to assert (PA) de-assert (PD) levels. There is no direct access to the SD signal, however the Rx data outputs will squelch and the RSSI will switch off, once the optical input power falls below PD. Furthermore, the Rx data and RSSI outputs will be activated, once the optical input power exceeds PA

Package Outline Drawing



NOTES (unless otherwise specified):
1) Dimension: mm
2) Label with Partnumber, Lotnumber and Datecode (10mm x 12mm)

Figure 7. Package Outline Drawing

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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