

1M-BIT CMOS STATIC RAM  
128K-WORD BY 8-BIT  
EXTENDED TEMPERATURE OPERATION

## Description

The  $\mu$ PD441000L-X is a high speed, low power, 1,048,576 bits (131,072 words by 8 bits) CMOS static RAM.

The  $\mu$ PD441000L-X has two chip enable pins (/CE1, CE2) to extend the capacity.

- ★ The  $\mu$ PD441000L-X is packed in 32-pin plastic SOP and 32-pin plastic TSOP (I) (8×13.4 mm) and (8×20 mm).

## Features

- 131,072 words by 8 bits organization
- Fast access time : 70, 85, 100, 120, 150 ns (MAX.)
- Low voltage operation  
(B version :  $V_{CC} = 2.7$  to  $3.6$  V, C version :  $V_{CC} = 2.2$  to  $3.6$  V, D version :  $V_{CC} = 1.8$  to  $3.6$  V)
- Low  $V_{CC}$  data retention  
(B version :  $2.0$  V (MIN.), C version, D version :  $1.5$  V (MIN.))
- Operating ambient temperature :  $T_A = -25$  to  $+85$  °C
- Output Enable input for easy application
- Two Chip Enable inputs : /CE1, CE2

| Part number          | Access time<br>ns (MAX.) | Operating supply<br>voltage<br>V | Operating ambient<br>temperature<br>°C | Supply current            |                              |                                     |
|----------------------|--------------------------|----------------------------------|----------------------------------------|---------------------------|------------------------------|-------------------------------------|
|                      |                          |                                  |                                        | At operating<br>mA (MAX.) | At standby<br>$\mu$ A (MAX.) | At data retention<br>$\mu$ A (MAX.) |
| $\mu$ PD441000L-BxxX | 70, 85, 100              | 2.7 to 3.6                       | -25 to +85                             | 25                        | 2                            | 2 <sup>Note</sup>                   |
| $\mu$ PD441000L-CxxX | 100, 120                 | 2.2 to 3.6                       |                                        |                           |                              |                                     |
| $\mu$ PD441000L-DxxX | 120, 150                 | 1.8 to 3.6                       |                                        |                           |                              |                                     |

**Note**  $0.5 \mu\text{A}$  ( $T_A \leq 40$  °C)

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

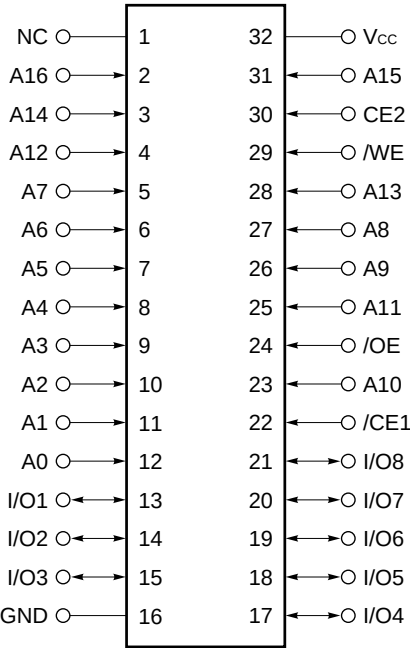
★ Ordering Information

| Part number           | Package                                            | Access time<br>ns (MAX.) | Operating<br>supply voltage<br>V | Operating<br>temperature<br>°C | Remark    |
|-----------------------|----------------------------------------------------|--------------------------|----------------------------------|--------------------------------|-----------|
| μPD441000LGW-B70X     | 32-pin Plastic SOP<br>(13.34 mm (525))             | 70                       | 2.7 to 3.6                       | −25 to +85                     | B version |
| μPD441000LGW-B85X     |                                                    | 85                       |                                  |                                |           |
| μPD441000LGW-B10X     |                                                    | 100                      |                                  |                                |           |
| μPD441000LGU-B70X-9JH | 32-pin Plastic TSOP (I)<br>(8×13.4) (Normal bent)  | 70                       |                                  |                                |           |
| μPD441000LGU-B85X-9JH |                                                    | 85                       |                                  |                                |           |
| μPD441000LGU-B10X-9JH |                                                    | 100                      |                                  |                                |           |
| μPD441000LGU-B70X-9KH | 32-pin Plastic TSOP (I)<br>(8×13.4) (Reverse bent) | 70                       |                                  |                                |           |
| μPD441000LGU-B85X-9KH |                                                    | 85                       |                                  |                                |           |
| μPD441000LGU-B10X-9KH |                                                    | 100                      |                                  |                                |           |
| μPD441000LGZ-B70X-KJH | 32-pin Plastic TSOP (I)<br>(8×20) (Normal bent)    | 70                       |                                  |                                |           |
| μPD441000LGZ-B85X-KJH |                                                    | 85                       |                                  |                                |           |
| μPD441000LGZ-B10X-KJH |                                                    | 100                      |                                  |                                |           |
| μPD441000LGZ-B70X-KKH | 32-pin Plastic TSOP (I)<br>(8×20) (Reverse bent)   | 70                       |                                  |                                |           |
| μPD441000LGZ-B85X-KKH |                                                    | 85                       |                                  |                                |           |
| μPD441000LGZ-B10X-KKH |                                                    | 100                      |                                  |                                |           |
| μPD441000LGW-C10X     | 32-pin Plastic SOP<br>(13.34 mm (525))             | 100                      | 2.2 to 3.6                       |                                | C version |
| μPD441000LGW-C12X     |                                                    | 120                      |                                  |                                |           |
| μPD441000LGU-C10X-9JH | 32-pin Plastic TSOP (I)<br>(8×13.4) (Normal bent)  | 100                      |                                  |                                |           |
| μPD441000LGU-C12X-9JH |                                                    | 120                      |                                  |                                |           |
| μPD441000LGU-C10X-9KH | 32-pin Plastic TSOP (I)<br>(8×13.4) (Reverse bent) | 100                      |                                  |                                |           |
| μPD441000LGU-C12X-9KH |                                                    | 120                      |                                  |                                |           |
| μPD441000LGZ-C10X-KJH | 32-pin Plastic TSOP (I)<br>(8×20) (Normal bent)    | 100                      |                                  |                                |           |
| μPD441000LGZ-C12X-KJH |                                                    | 120                      |                                  |                                |           |
| μPD441000LGZ-C10X-KKH | 32-pin Plastic TSOP (I)<br>(8×20) (Reverse bent)   | 100                      |                                  |                                |           |
| μPD441000LGZ-C12X-KKH |                                                    | 120                      |                                  |                                |           |
| μPD441000LGW-D12X     | 32-pin Plastic SOP<br>(13.34 mm (525))             | 120                      | 1.8 to 3.6                       |                                | D version |
| μPD441000LGW-D15X     |                                                    | 150                      |                                  |                                |           |
| μPD441000LGU-D12X-9JH | 32-pin Plastic TSOP (I)<br>(8×13.4) (Normal bent)  | 120                      |                                  |                                |           |
| μPD441000LGU-D15X-9JH |                                                    | 150                      |                                  |                                |           |
| μPD441000LGU-D12X-9KH | 32-pin Plastic TSOP (I)<br>(8×13.4) (Reverse bent) | 120                      |                                  |                                |           |
| μPD441000LGU-D15X-9KH |                                                    | 150                      |                                  |                                |           |
| μPD441000LGZ-D12X-KJH | 32-pin Plastic TSOP (I)<br>(8×20) (Normal bent)    | 120                      |                                  |                                |           |
| μPD441000LGZ-D15X-KJH |                                                    | 150                      |                                  |                                |           |
| μPD441000LGZ-D12X-KKH | 32-pin Plastic TSOP (I)<br>(8×20) (Reverse bent)   | 120                      |                                  |                                |           |
| μPD441000LGZ-D15X-KKH |                                                    | 150                      |                                  |                                |           |

Pin Configurations (Marking Side)

/xxx indicates active low signal.

32-pin Plastic SOP (13.34 mm (525))  
[ μPD441000LGW-BxxX ]  
[ μPD441000LGW-CxxX ]  
[ μPD441000LGW-DxxX ]



- A0 - A16 : Address inputs
- I/O1 - I/O8 : Data inputs / outputs
- /CE1, CE2 : Chip Enable 1, 2
- /WE : Write Enable
- /OE : Output Enable
- Vcc : Power supply
- GND : Ground
- NC : No connection

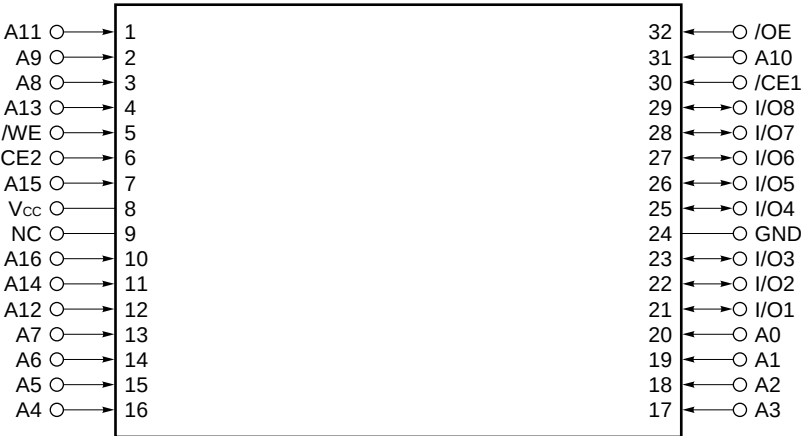
**Remark** Refer to **Package Drawings** for the 1-pin index mark.

32-pin Plastic TSOP (I) (8x13.4) (Normal bent)

- [ μPD441000LGU-BxxX-9JH ]
- [ μPD441000LGU-CxxX-9JH ]
- [ μPD441000LGU-DxxX-9JH ]

32-pin Plastic TSOP (I) (8x20) (Normal bent)

- [ μPD441000LGZ-BxxX-KJH ]
- [ μPD441000LGZ-CxxX-KJH ]
- [ μPD441000LGZ-DxxX-KJH ]



- A0 - A16 : Address inputs
- /O1 - /O8 : Data inputs / outputs
- /CE1, CE2 : Chip Enable 1, 2
- /WE : Write Enable
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- Vcc : Power supply
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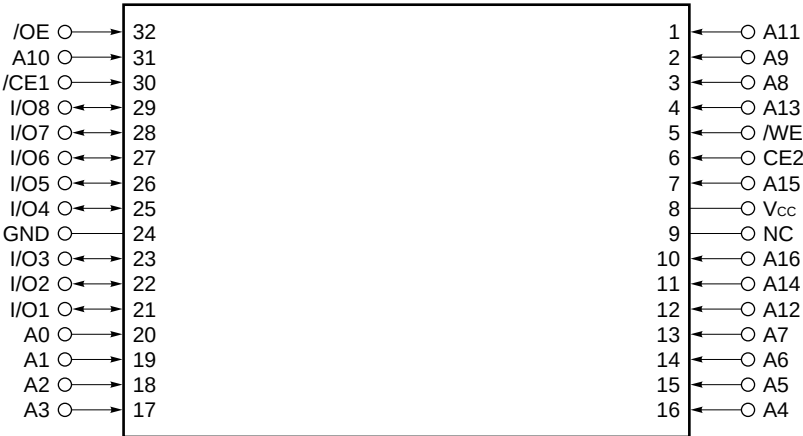
**Remark** Refer to **Package Drawings** for the 1-pin index mark.

32-pin Plastic TSOP (I) (8x13.4) (Reverse bent)

- [ μPD441000LGU-BxxX-9KH ]
- [ μPD441000LGU-CxxX-9KH ]
- [ μPD441000LGU-DxxX-9KH ]

32-pin Plastic TSOP (I) (8x20) (Reverse bent)

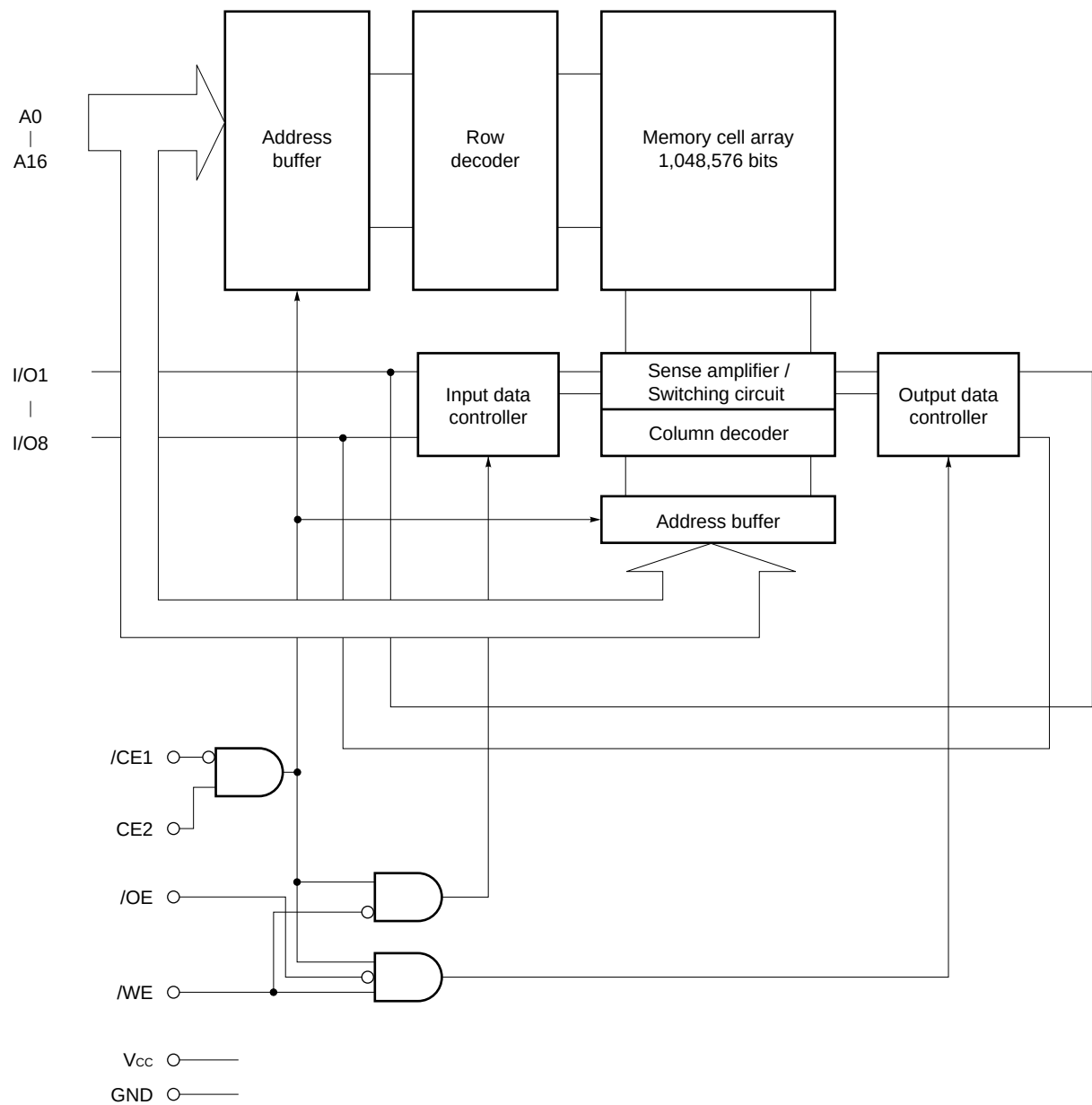
- [ μPD441000LGZ-BxxX-KKH ]
- [ μPD441000LGZ-CxxX-KKH ]
- [ μPD441000LGZ-DxxX-KKH ]



- A0 - A16 : Address inputs
- I/O1 - I/O8 : Data inputs / outputs
- /CE1, CE2 : Chip Enable 1, 2
- /WE : Write Enable
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- Vcc : Power supply
- GND : Ground
- NC : No connection

**Remark** Refer to **Package Drawings** for the 1-pin index mark.

Block Diagram



Truth Table

| /CE1 | CE2 | /OE | /WE | Mode           | I/O              | Supply current   |
|------|-----|-----|-----|----------------|------------------|------------------|
| H    | ×   | ×   | ×   | Not selected   | High impedance   | I <sub>SB</sub>  |
| ×    | L   | ×   | ×   | Not selected   | High impedance   |                  |
| L    | H   | H   | H   | Output disable | High impedance   | I <sub>CCA</sub> |
| L    | H   | L   | H   | Read           | D <sub>OUT</sub> |                  |
| L    | H   | ×   | L   | Write          | D <sub>IN</sub>  |                  |

Remark × : V<sub>IH</sub> or V<sub>IL</sub>

## Electrical Specifications

### Absolute Maximum Ratings

| Parameter                     | Symbol    | Condition | Rating                               | Unit |
|-------------------------------|-----------|-----------|--------------------------------------|------|
| Supply voltage                | $V_{CC}$  |           | $-0.5^{\text{Note}}$ to +4.6         | V    |
| Input / Output voltage        | $V_T$     |           | $-0.5^{\text{Note}}$ to $V_{CC}+0.5$ | V    |
| Operating ambient temperature | $T_A$     |           | -25 to +85                           | °C   |
| Storage temperature           | $T_{stg}$ |           | -55 to +125                          | °C   |

**Note** -3.0 V (MIN.) (Pulse width : 30 ns)

**Caution** Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### Recommended Operating Conditions

| Parameter                     | Symbol   | Condition                                      | μPD441000L-BxxX      |              | μPD441000L-CxxX      |              | μPD441000L-DxxX      |              | Unit |
|-------------------------------|----------|------------------------------------------------|----------------------|--------------|----------------------|--------------|----------------------|--------------|------|
|                               |          |                                                | MIN.                 | MAX.         | MIN.                 | MAX.         | MIN.                 | MAX.         |      |
| Supply voltage                | $V_{CC}$ |                                                | 2.7                  | 3.6          | 2.2                  | 3.6          | 1.8                  | 3.6          | V    |
| High level input voltage      | $V_{IH}$ | $2.7 \text{ V} \leq V_{CC} \leq 3.6 \text{ V}$ | 2.4                  | $V_{CC}+0.5$ | 2.4                  | $V_{CC}+0.5$ | 2.4                  | $V_{CC}+0.5$ | V    |
|                               |          | $2.2 \text{ V} \leq V_{CC} < 2.7 \text{ V}$    | —                    | —            | 2.0                  | $V_{CC}+0.5$ | 2.0                  | $V_{CC}+0.5$ |      |
|                               |          | $1.8 \text{ V} \leq V_{CC} < 2.2 \text{ V}$    | —                    | —            | —                    | —            | 1.6                  | $V_{CC}+0.5$ |      |
| Low level input voltage       | $V_{IL}$ |                                                | $-0.3^{\text{Note}}$ | +0.5         | $-0.3^{\text{Note}}$ | +0.3         | $-0.3^{\text{Note}}$ | +0.2         | V    |
| Operating ambient temperature | $T_A$    |                                                | -25                  | +85          | -25                  | +85          | -25                  | +85          | °C   |

**Note** -3.0 V (MIN.) (Pulse width : 30 ns)

### Capacitance ( $T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ )

| Parameter                  | Symbol    | Test condition          | MIN. | TYP. | MAX. | Unit |
|----------------------------|-----------|-------------------------|------|------|------|------|
| Input capacitance          | $C_{IN}$  | $V_{IN} = 0 \text{ V}$  |      |      | 6    | pF   |
| Input / Output capacitance | $C_{I/O}$ | $V_{I/O} = 0 \text{ V}$ |      |      | 10   | pF   |

**Remarks 1.**  $V_{IN}$  : Input voltage

$V_{I/O}$  : Input / Output voltage

**2.** These parameters are periodically sampled and not 100% tested.

**DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

| Parameter                 | Symbol            | Test condition                                                                                                                                | μPD441000L-BxxX |      |      | μPD441000L-CxxX |      |      | μPD441000L-DxxX |      |      | Unit |
|---------------------------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------------|------|------|-----------------|------|------|-----------------|------|------|------|
|                           |                   |                                                                                                                                               | MIN.            | TYP. | MAX. | MIN.            | TYP. | MAX. | MIN.            | TYP. | MAX. |      |
| Input leakage current     | I <sub>LI</sub>   | V <sub>IN</sub> = 0 V to V <sub>CC</sub>                                                                                                      | -1.0            |      | +1.0 | -1.0            |      | +1.0 | -1.0            |      | +1.0 | μA   |
| I/O leakage current       | I <sub>LO</sub>   | V <sub>I/O</sub> = 0 V to V <sub>CC</sub> , /CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or /WE = V <sub>IL</sub> or /OE = V <sub>IH</sub> | -1.0            |      | +1.0 | -1.0            |      | +1.0 | -1.0            |      | +1.0 | μA   |
| Operating supply current  | I <sub>CCA1</sub> | /CE1 = V <sub>IL</sub> , CE2 = V <sub>IH</sub> ,                                                                                              |                 | 23   | 25   |                 | 23   | 25   |                 | 23   | 25   | mA   |
|                           |                   | Minimum cycle time, V <sub>CC</sub> ≤ 2.7 V                                                                                                   |                 | —    | —    |                 | 20   | 23   |                 | 20   | 23   |      |
|                           |                   | I <sub>I/O</sub> = 0 mA, V <sub>CC</sub> ≤ 2.2 V                                                                                              |                 | —    | —    |                 | —    | —    |                 | 17   | 20   |      |
|                           | I <sub>CCA2</sub> | /CE1 = V <sub>IL</sub> , CE2 = V <sub>IH</sub> ,                                                                                              |                 |      | 5    |                 |      | 5    |                 |      | 5    |      |
|                           |                   | I <sub>I/O</sub> = 0 mA, V <sub>CC</sub> ≤ 2.7 V                                                                                              |                 |      | —    |                 |      | 4    |                 |      | 4    |      |
|                           |                   | V <sub>CC</sub> ≤ 2.2 V                                                                                                                       |                 |      | —    |                 |      | —    |                 |      | 3    |      |
|                           | I <sub>CCA3</sub> | /CE1 ≤ 0.2 V, CE2 ≥ V <sub>CC</sub> - 0.2 V,                                                                                                  |                 |      | 4    |                 |      | 4    |                 |      | 4    |      |
|                           |                   | Cycle = 1 MHz, I <sub>I/O</sub> = 0 mA,                                                                                                       |                 |      |      |                 |      |      |                 |      |      |      |
|                           |                   | V <sub>IL</sub> ≤ 0.2 V, V <sub>CC</sub> ≤ 2.7 V                                                                                              |                 |      | —    |                 |      | 3    |                 |      | 3    |      |
|                           |                   | V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>CC</sub> ≤ 2.2 V                                                                            |                 |      | —    |                 |      | —    |                 |      | 3    |      |
|                           |                   |                                                                                                                                               |                 |      |      |                 |      |      |                 |      |      |      |
|                           |                   |                                                                                                                                               |                 |      |      |                 |      |      |                 |      |      |      |
| Standby supply current    | I <sub>SB</sub>   | /CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub>                                                                                               |                 |      | 0.3  |                 |      | 0.3  |                 |      | 0.3  | mA   |
|                           | I <sub>SB1</sub>  | /CE1 ≥ V <sub>CC</sub> - 0.2 V,                                                                                                               |                 | 0.05 | 2    |                 | 0.05 | 2    |                 | 0.05 | 2    |      |
|                           |                   | CE2 ≥ V <sub>CC</sub> - 0.2 V, V <sub>CC</sub> ≤ 2.7 V                                                                                        |                 | —    | —    |                 | 0.04 | 2    |                 | 0.04 | 2    |      |
|                           |                   | V <sub>CC</sub> ≤ 2.2 V                                                                                                                       |                 | —    | —    |                 | —    | —    |                 | 0.03 | 1.5  |      |
|                           | I <sub>SB2</sub>  | CE2 ≤ 0.2 V                                                                                                                                   |                 | 0.05 | 2    |                 | 0.05 | 2    |                 | 0.05 | 2    |      |
|                           |                   | V <sub>CC</sub> ≤ 2.7 V                                                                                                                       |                 | —    | —    |                 | 0.04 | 2    |                 | 0.04 | 2    |      |
|                           |                   | V <sub>CC</sub> ≤ 2.2 V                                                                                                                       |                 | —    | —    |                 | —    | —    |                 | 0.03 | 1.5  |      |
| High level output voltage | V <sub>OH</sub>   | I <sub>OH</sub> = -0.5 mA                                                                                                                     | 2.4             |      |      | 2.4             |      |      | 2.4             |      |      | V    |
|                           |                   | V <sub>CC</sub> ≤ 2.7 V                                                                                                                       | —               |      |      | 1.8             |      |      | 1.8             |      |      |      |
|                           |                   | V <sub>CC</sub> ≤ 2.2 V                                                                                                                       | —               |      |      | —               |      |      | 1.5             |      |      |      |
| Low level output voltage  | V <sub>OL</sub>   | I <sub>OL</sub> = 1.0 mA                                                                                                                      |                 |      | 0.4  |                 |      | 0.4  |                 |      | 0.4  | V    |

**Remarks 1.** V<sub>IN</sub> : Input voltage

V<sub>I/O</sub> : Input / Output voltage

**2.** These DC characteristics are in common regardless of package types and access time.

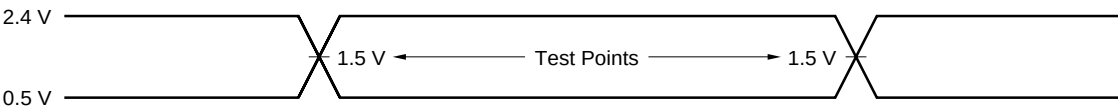


AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

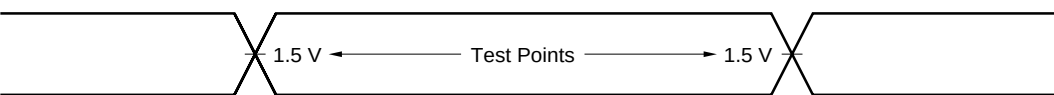
AC Test Conditions

[ μPD441000L-B70X, μPD441000L-B85X, μPD441000L-B10X ]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

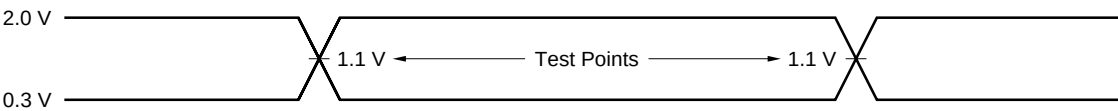


Output Load

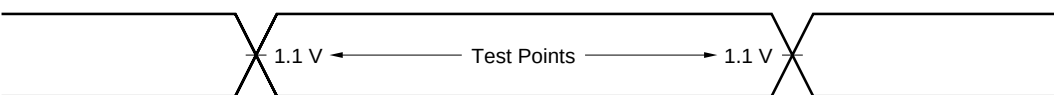
1TTL + 50 pF

[ μPD441000L-C10X, μPD441000L-C12X ]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

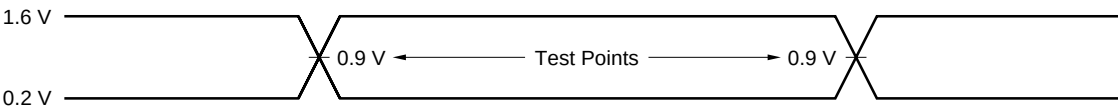


Output Load

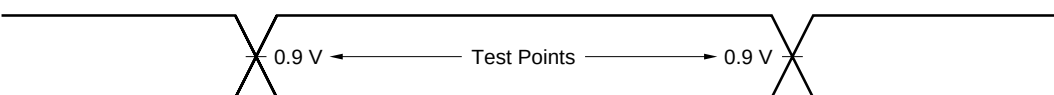
1TTL + 30 pF

[ μPD441000L-D12X, μPD441000L-D15X ]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1TTL + 30 pF

Read Cycle (1/3) (B version)

| Parameter                        | Symbol           | μPD441000L-B70X |      | μPD441000L-B85X |      | μPD441000L-B10X |      | Unit | Condition |
|----------------------------------|------------------|-----------------|------|-----------------|------|-----------------|------|------|-----------|
|                                  |                  | MIN.            | MAX. | MIN.            | MAX. | MIN.            | MAX. |      |           |
| Read cycle time                  | t <sub>RC</sub>  | 70              |      | 85              |      | 100             |      | ns   |           |
| Address access time              | t <sub>AA</sub>  |                 | 70   |                 | 85   |                 | 100  | ns   | Note 1    |
| /CE1 access time                 | t <sub>CO1</sub> |                 | 70   |                 | 85   |                 | 100  | ns   |           |
| CE2 access time                  | t <sub>CO2</sub> |                 | 70   |                 | 85   |                 | 100  | ns   |           |
| /OE to output valid              | t <sub>OE</sub>  |                 | 35   |                 | 45   |                 | 50   | ns   |           |
| Output hold from address change  | t <sub>OH</sub>  | 10              |      | 10              |      | 10              |      | ns   |           |
| /CE1 to output in low impedance  | t <sub>LZ1</sub> | 10              |      | 10              |      | 10              |      | ns   | Note 2    |
| CE2 to output in low impedance   | t <sub>LZ2</sub> | 10              |      | 10              |      | 10              |      | ns   |           |
| /OE to output in low impedance   | t <sub>OLZ</sub> | 5               |      | 5               |      | 5               |      | ns   |           |
| /CE1 to output in high impedance | t <sub>HZ1</sub> |                 | 25   |                 | 30   |                 | 35   | ns   |           |
| CE2 to output in high impedance  | t <sub>HZ2</sub> |                 | 25   |                 | 30   |                 | 35   | ns   |           |
| /OE to output in high impedance  | t <sub>OHZ</sub> |                 | 25   |                 | 30   |                 | 35   | ns   |           |

**Notes** 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

**Remark** These AC characteristics are in common regardless of package types.

Read Cycle (2/3) (C version)

| Parameter                        | Symbol           | μPD441000L-C10X |      | μPD441000L-C12X |      | Unit | Condition |
|----------------------------------|------------------|-----------------|------|-----------------|------|------|-----------|
|                                  |                  | MIN.            | MAX. | MIN.            | MAX. |      |           |
| Read cycle time                  | t <sub>RC</sub>  | 100             |      | 120             |      | ns   |           |
| Address access time              | t <sub>AA</sub>  |                 | 100  |                 | 120  | ns   | Note 1    |
| /CE1 access time                 | t <sub>CO1</sub> |                 | 100  |                 | 120  | ns   |           |
| CE2 access time                  | t <sub>CO2</sub> |                 | 100  |                 | 120  | ns   |           |
| /OE to output valid              | t <sub>OE</sub>  |                 | 50   |                 | 60   | ns   |           |
| Output hold from address change  | t <sub>OH</sub>  | 10              |      | 10              |      | ns   |           |
| /CE1 to output in low impedance  | t <sub>LZ1</sub> | 10              |      | 10              |      | ns   | Note 2    |
| CE2 to output in low impedance   | t <sub>LZ2</sub> | 10              |      | 10              |      | ns   |           |
| /OE to output in low impedance   | t <sub>OLZ</sub> | 5               |      | 5               |      | ns   |           |
| /CE1 to output in high impedance | t <sub>HZ1</sub> |                 | 35   |                 | 40   | ns   |           |
| CE2 to output in high impedance  | t <sub>HZ2</sub> |                 | 35   |                 | 40   | ns   |           |
| /OE to output in high impedance  | t <sub>OHZ</sub> |                 | 35   |                 | 40   | ns   |           |

**Notes** 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

**Remark** These AC characteristics are in common regardless of package types.

Read Cycle (3/3) (D version)

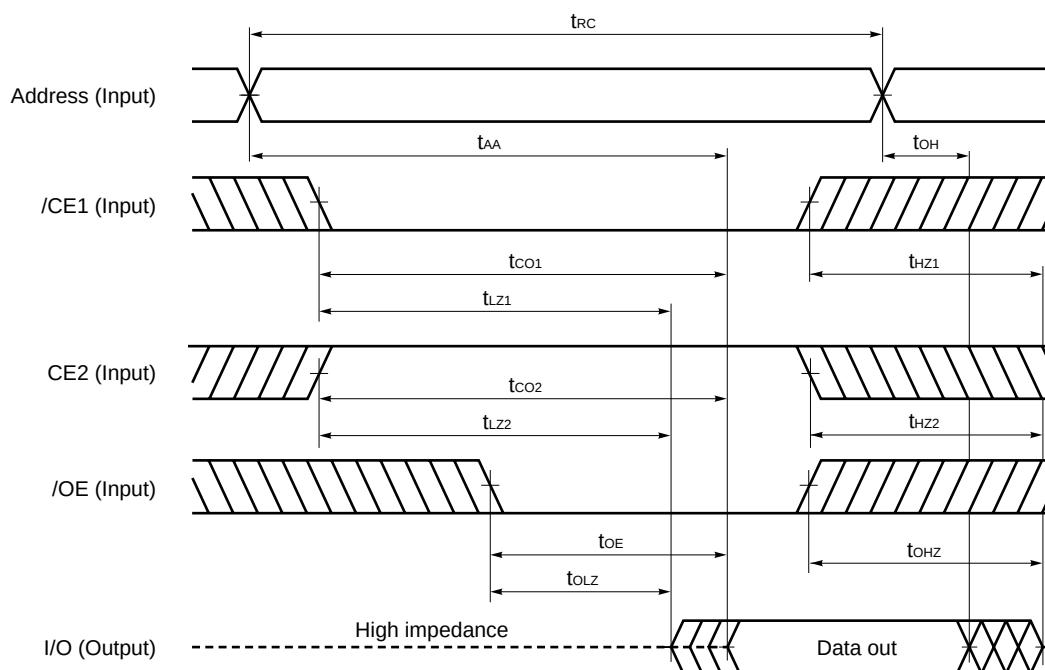
| Parameter                        | Symbol    | μPD441000L-D12X |      | μPD441000L-D15X |      | Unit | Condition |
|----------------------------------|-----------|-----------------|------|-----------------|------|------|-----------|
|                                  |           | MIN.            | MAX. | MIN.            | MAX. |      |           |
| Read cycle time                  | $t_{RC}$  | 120             |      | 150             |      | ns   |           |
| Address access time              | $t_{AA}$  |                 | 120  |                 | 150  | ns   | Note 1    |
| /CE1 access time                 | $t_{CO1}$ |                 | 120  |                 | 150  | ns   |           |
| CE2 access time                  | $t_{CO2}$ |                 | 120  |                 | 150  | ns   |           |
| /OE to output valid              | $t_{OE}$  |                 | 60   |                 | 70   | ns   |           |
| Output hold from address change  | $t_{OH}$  | 10              |      | 10              |      | ns   |           |
| /CE1 to output in low impedance  | $t_{LZ1}$ | 10              |      | 10              |      | ns   | Note 2    |
| CE2 to output in low impedance   | $t_{LZ2}$ | 10              |      | 10              |      | ns   |           |
| /OE to output in low impedance   | $t_{OLZ}$ | 5               |      | 5               |      | ns   |           |
| /CE1 to output in high impedance | $t_{HZ1}$ |                 | 40   |                 | 50   | ns   |           |
| CE2 to output in high impedance  | $t_{HZ2}$ |                 | 40   |                 | 50   | ns   |           |
| /OE to output in high impedance  | $t_{OHZ}$ |                 | 40   |                 | 50   | ns   |           |

**Notes** 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

**Remark** These AC characteristics are in common regardless of package types.

Read Cycle Timing Chart



**Remark** In read cycle, /WE should be fixed to high level.

**Write Cycle (1/3) (B version)**

| Parameter                       | Symbol           | μPD441000L-B70X |      | μPD441000L-B85X |      | μPD441000L-B10X |      | Unit | Condition   |
|---------------------------------|------------------|-----------------|------|-----------------|------|-----------------|------|------|-------------|
|                                 |                  | MIN.            | MAX. | MIN.            | MAX. | MIN.            | MAX. |      |             |
| Write cycle time                | t <sub>WC</sub>  | 70              |      | 85              |      | 100             |      | ns   |             |
| /CE1 to end of write            | t <sub>CW1</sub> | 55              |      | 70              |      | 80              |      | ns   |             |
| CE2 to end of write             | t <sub>CW2</sub> | 55              |      | 70              |      | 80              |      | ns   |             |
| Address valid to end of write   | t <sub>AW</sub>  | 55              |      | 70              |      | 80              |      | ns   |             |
| Address setup time              | t <sub>AS</sub>  | 0               |      | 0               |      | 0               |      | ns   |             |
| Write pulse width               | t <sub>WP</sub>  | 50              |      | 60              |      | 60              |      | ns   |             |
| Write recovery time             | t <sub>WR</sub>  | 0               |      | 0               |      | 0               |      | ns   |             |
| Data valid to end of write      | t <sub>DW</sub>  | 35              |      | 35              |      | 40              |      | ns   |             |
| Data hold time                  | t <sub>DH</sub>  | 0               |      | 0               |      | 0               |      | ns   |             |
| /WE to output in high impedance | t <sub>WHZ</sub> |                 | 25   |                 | 30   |                 | 35   | ns   | <b>Note</b> |
| Output active from end of write | t <sub>OW</sub>  | 5               |      | 5               |      | 5               |      | ns   |             |

**Note** The output load is 1TTL + 5 pF.

**Remark** These AC characteristics are in common regardless of package types.

**Write Cycle (2/3) (C version)**

| Parameter                       | Symbol           | μPD441000L-C10X |      | μPD441000L-C12X |      | Unit | Condition   |
|---------------------------------|------------------|-----------------|------|-----------------|------|------|-------------|
|                                 |                  | MIN.            | MAX. | MIN.            | MAX. |      |             |
| Write cycle time                | t <sub>WC</sub>  | 100             |      | 120             |      | ns   |             |
| /CE1 to end of write            | t <sub>CW1</sub> | 80              |      | 100             |      | ns   |             |
| CE2 to end of write             | t <sub>CW2</sub> | 80              |      | 100             |      | ns   |             |
| Address valid to end of write   | t <sub>AW</sub>  | 80              |      | 100             |      | ns   |             |
| Address setup time              | t <sub>AS</sub>  | 0               |      | 0               |      | ns   |             |
| Write pulse width               | t <sub>WP</sub>  | 60              |      | 85              |      | ns   |             |
| Write recovery time             | t <sub>WR</sub>  | 0               |      | 0               |      | ns   |             |
| Data valid to end of write      | t <sub>DW</sub>  | 45              |      | 60              |      | ns   |             |
| Data hold time                  | t <sub>DH</sub>  | 0               |      | 0               |      | ns   |             |
| /WE to output in high impedance | t <sub>WHZ</sub> |                 | 35   |                 | 40   | ns   | <b>Note</b> |
| Output active from end of write | t <sub>OW</sub>  | 5               |      | 5               |      | ns   |             |

**Note** The output load is 1TTL + 5 pF.

**Remark** These AC characteristics are in common regardless of package types.

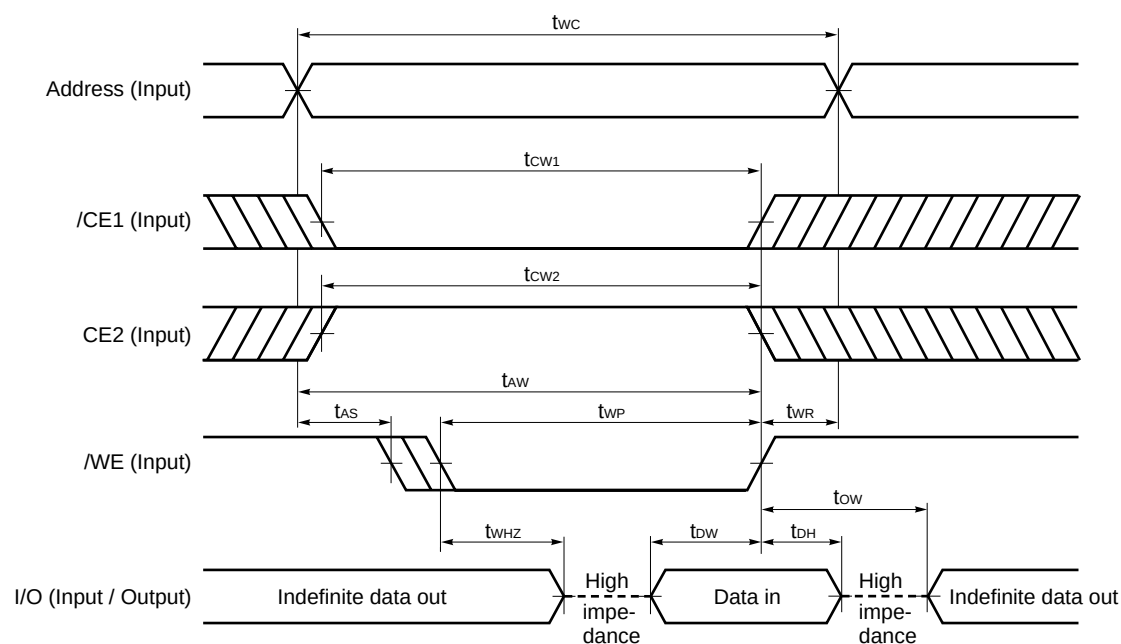
Write Cycle (3/3) (D version)

| Parameter                       | Symbol           | μPD441000L-D12X |      | μPD441000L-D15X |      | Unit | Condition |
|---------------------------------|------------------|-----------------|------|-----------------|------|------|-----------|
|                                 |                  | MIN.            | MAX. | MIN.            | MAX. |      |           |
| Write cycle time                | t <sub>WC</sub>  | 120             |      | 150             |      | ns   |           |
| /CE1 to end of write            | t <sub>CW1</sub> | 100             |      | 120             |      | ns   |           |
| CE2 to end of write             | t <sub>CW2</sub> | 100             |      | 120             |      | ns   |           |
| Address valid to end of write   | t <sub>AW</sub>  | 100             |      | 120             |      | ns   |           |
| Address setup time              | t <sub>AS</sub>  | 0               |      | 0               |      | ns   |           |
| Write pulse width               | t <sub>WP</sub>  | 85              |      | 100             |      | ns   |           |
| Write recovery time             | t <sub>WR</sub>  | 0               |      | 0               |      | ns   |           |
| Data valid to end of write      | t <sub>DW</sub>  | 60              |      | 80              |      | ns   |           |
| Data hold time                  | t <sub>DH</sub>  | 0               |      | 0               |      | ns   |           |
| /WE to output in high impedance | t <sub>WHZ</sub> |                 | 40   |                 | 50   | ns   | Note      |
| Output active from end of write | t <sub>OW</sub>  | 5               |      | 5               |      | ns   |           |

**Note** The output load is 1TTL + 5 pF.

**Remark** These AC characteristics are in common regardless of package types.

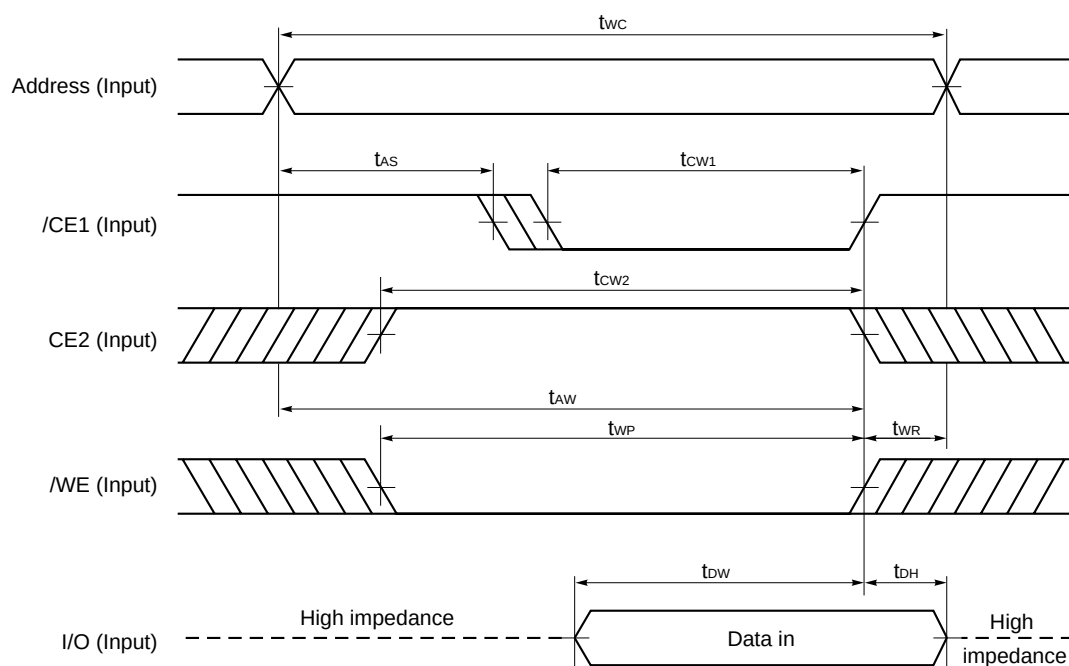
Write Cycle Timing Chart 1 (/WE Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
  2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

- Remarks**
1. Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.
  2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.
  3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

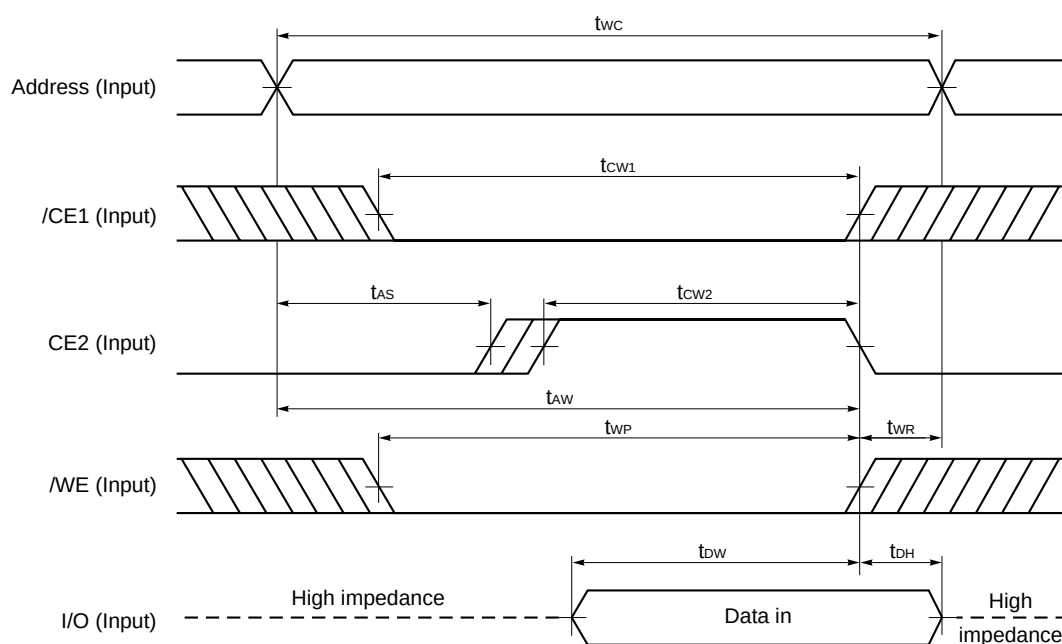
Write Cycle Timing Chart 2 (/CE1 Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
  2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

**Remark** Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
  2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

**Remark** Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.



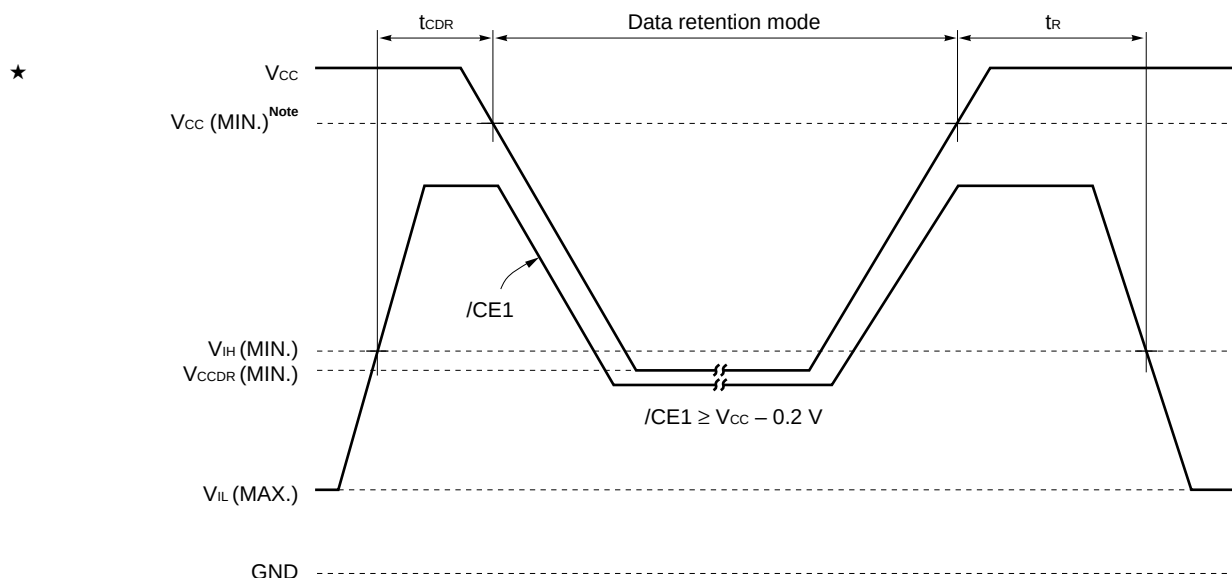
Low V<sub>CC</sub> Data Retention Characteristics (T<sub>A</sub> = -25 to +85 °C)

| Parameter                                  | Symbol             | Test Condition                                                                                           | μPD441000L<br>-BxxX |      |                   | μPD441000L<br>-CxxX |      |                   | μPD441000L<br>-DxxX |      |                   | Unit |
|--------------------------------------------|--------------------|----------------------------------------------------------------------------------------------------------|---------------------|------|-------------------|---------------------|------|-------------------|---------------------|------|-------------------|------|
|                                            |                    |                                                                                                          | MIN.                | TYP. | MAX.              | MIN.                | TYP. | MAX.              | MIN.                | TYP. | MAX.              |      |
| Data retention<br>supply voltage           | V <sub>CCDR1</sub> | /CE1 ≥ V <sub>CC</sub> - 0.2 V,<br>CE2 ≥ V <sub>CC</sub> - 0.2 V                                         | 2                   |      | 3.6               | 1.5                 |      | 3.6               | 1.5                 |      | 3.6               | V    |
|                                            | V <sub>CCDR2</sub> | CE2 ≤ 0.2 V                                                                                              | 2                   |      | 3.6               | 1.5                 |      | 3.6               | 1.5                 |      | 3.6               |      |
| Data retention<br>supply current           | I <sub>CCDR1</sub> | V <sub>CC</sub> = 3.0 V, /CE1 ≥ V <sub>CC</sub> - 0.2 V,<br>CE2 ≥ V <sub>CC</sub> - 0.2 V or CE2 ≤ 0.2 V |                     | 0.05 | 2 <sup>Note</sup> |                     | 0.05 | 2 <sup>Note</sup> |                     | 0.05 | 2 <sup>Note</sup> | μA   |
|                                            | I <sub>CCDR2</sub> | V <sub>CC</sub> = 3.0 V, CE2 ≤ 0.2 V                                                                     |                     | 0.05 | 2 <sup>Note</sup> |                     | 0.05 | 2 <sup>Note</sup> |                     | 0.05 | 2 <sup>Note</sup> |      |
| Chip deselection to<br>data retention mode | t <sub>CDR</sub>   |                                                                                                          | 0                   |      |                   | 0                   |      |                   | 0                   |      |                   | ns   |
| Operation recovery<br>time                 | t <sub>R</sub>     |                                                                                                          | 5                   |      |                   | 5                   |      |                   | 5                   |      |                   | ms   |

**Note** 0.5 μA (T<sub>A</sub> ≤ 40 °C)

# Data Retention Timing Chart

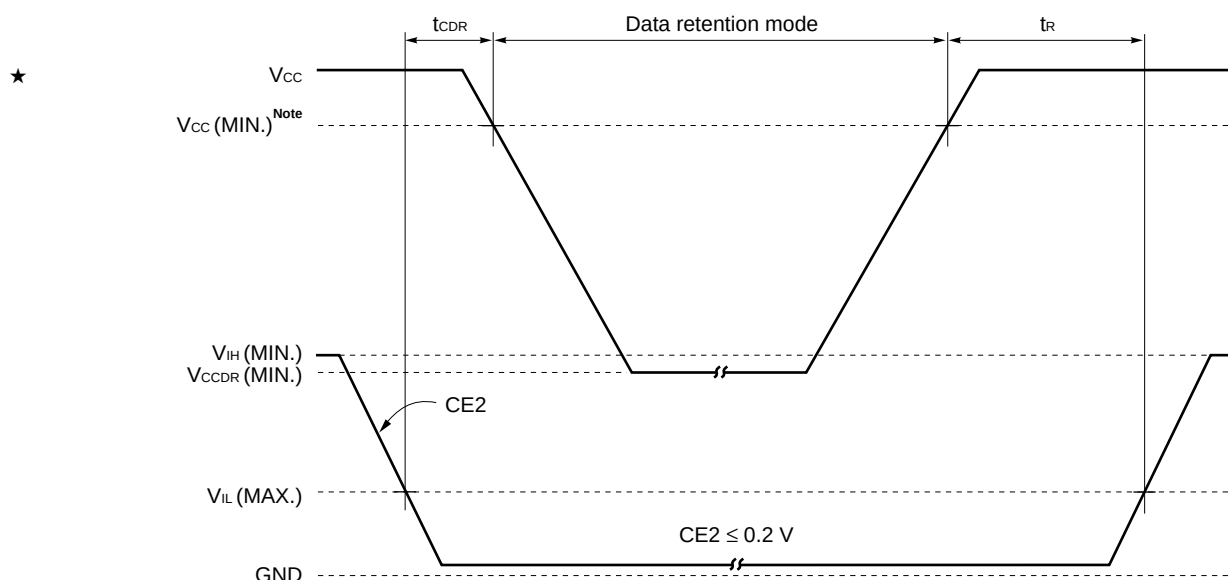
## (1) /CE1 Controlled



**Note** B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

**Remark** On the data retention mode by controlling  $\overline{\text{CE1}}$ , the input level of CE2 must be  $\geq V_{\text{CC}} - 0.2 \text{ V}$  or  $\leq 0.2 \text{ V}$ . The other pins (Address, I/O,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ) can be in high impedance state.

## (2) CE2 Controlled

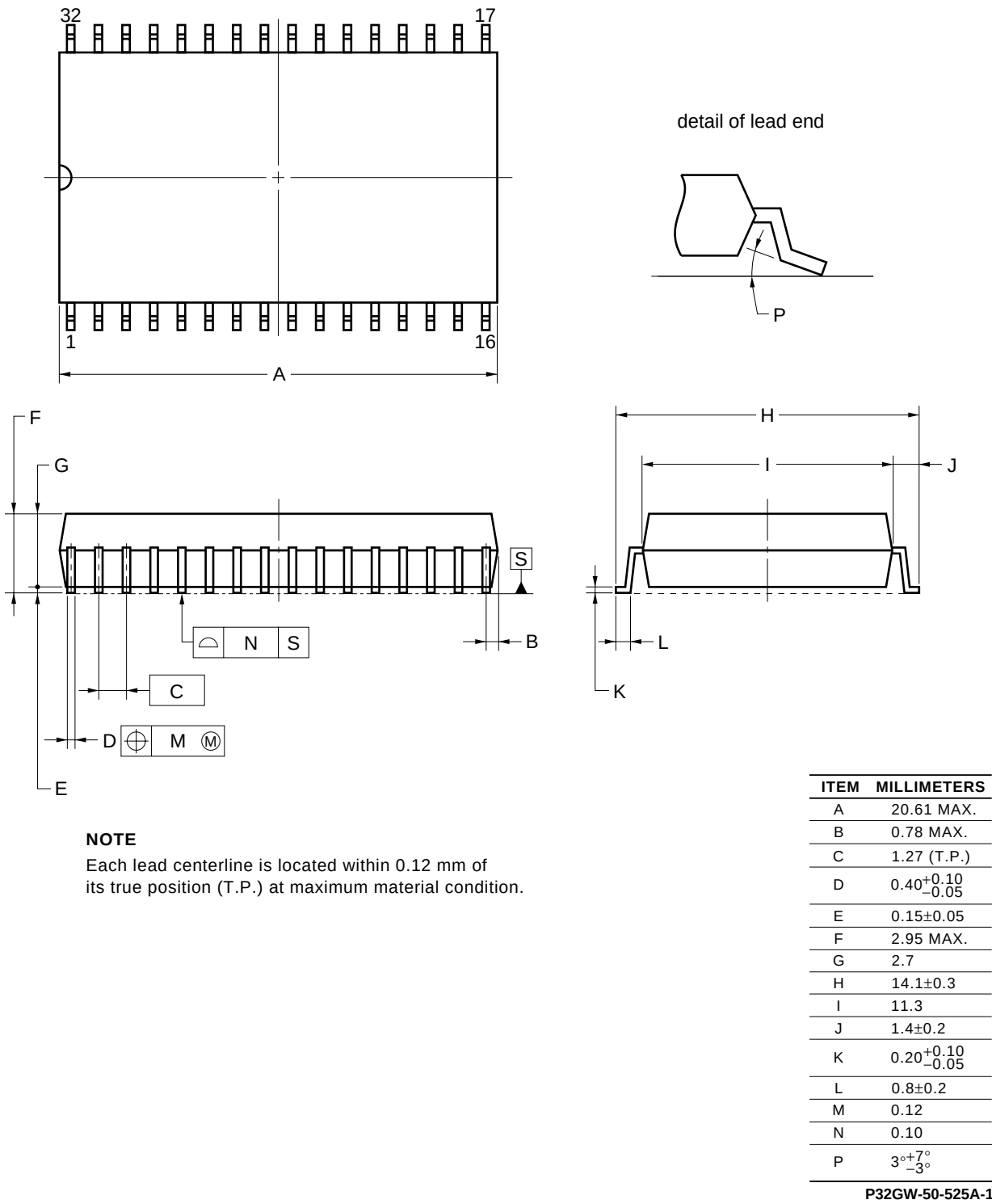


**Note** B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

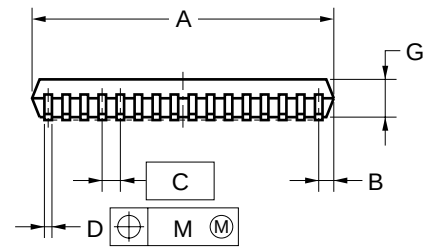
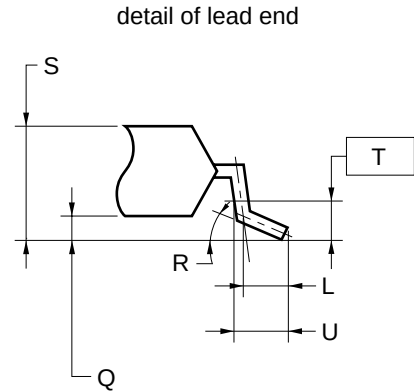
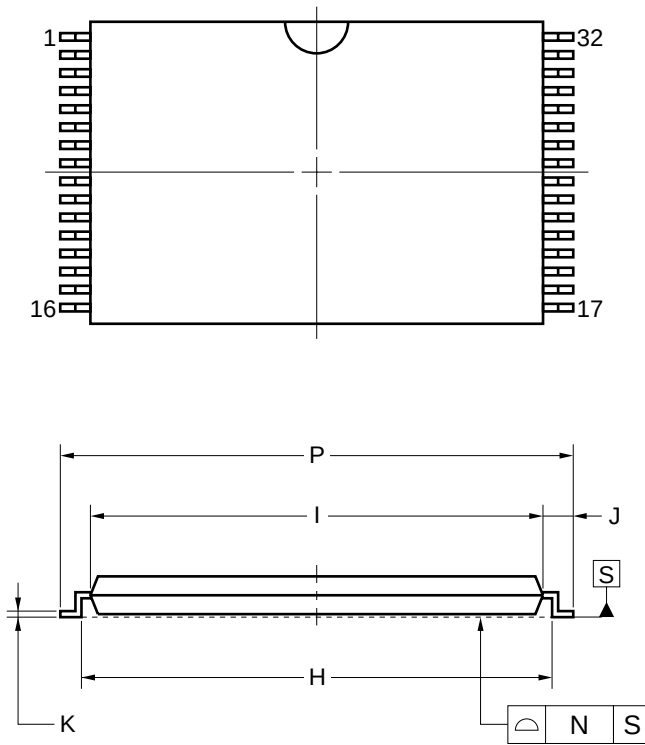
**Remark** On the data retention mode by controlling CE2, the other pins ( $\overline{\text{CE1}}$ , Address, I/O,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ) can be in high impedance state.

Package Drawings

★ 32-PIN PLASTIC SOP (13.34 mm (525))



★ 32-PIN PLASTIC TSOP(I) (8x13.4)



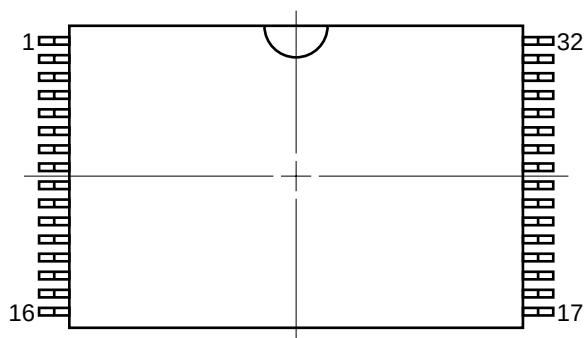
NOTES

- Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
- "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

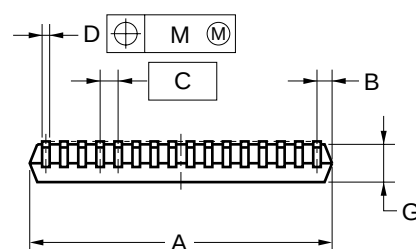
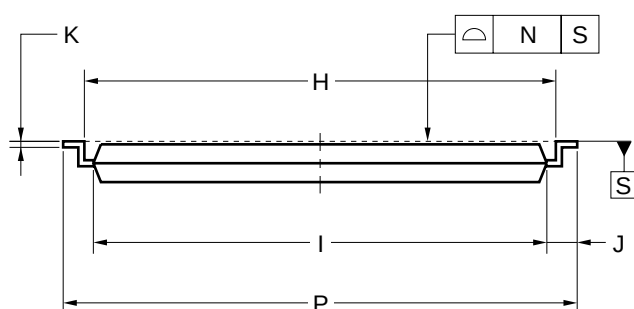
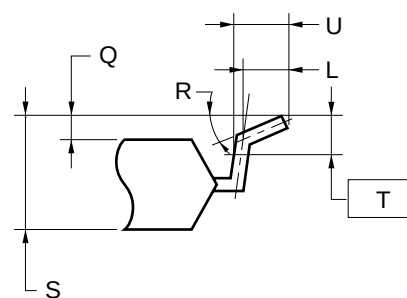
| ITEM | MILLIMETERS                               |
|------|-------------------------------------------|
| A    | 8.0±0.1                                   |
| B    | 0.45 MAX.                                 |
| C    | 0.5 (T.P.)                                |
| D    | 0.22±0.05                                 |
| G    | 1.0±0.05                                  |
| H    | 12.4±0.2                                  |
| I    | 11.8±0.1                                  |
| J    | 0.8±0.2                                   |
| K    | 0.145 <sup>+0.025</sup> <sub>-0.015</sub> |
| L    | 0.5                                       |
| M    | 0.08                                      |
| N    | 0.08                                      |
| P    | 13.4±0.2                                  |
| Q    | 0.1±0.05                                  |
| R    | 3° <sup>+5°</sup> <sub>-3°</sub>          |
| S    | 1.2 MAX.                                  |
| T    | 0.25                                      |
| U    | 0.6±0.15                                  |

P32GU-50-9JH-2

★ 32-PIN PLASTIC TSOP(I) (8x13.4)



detail of lead end



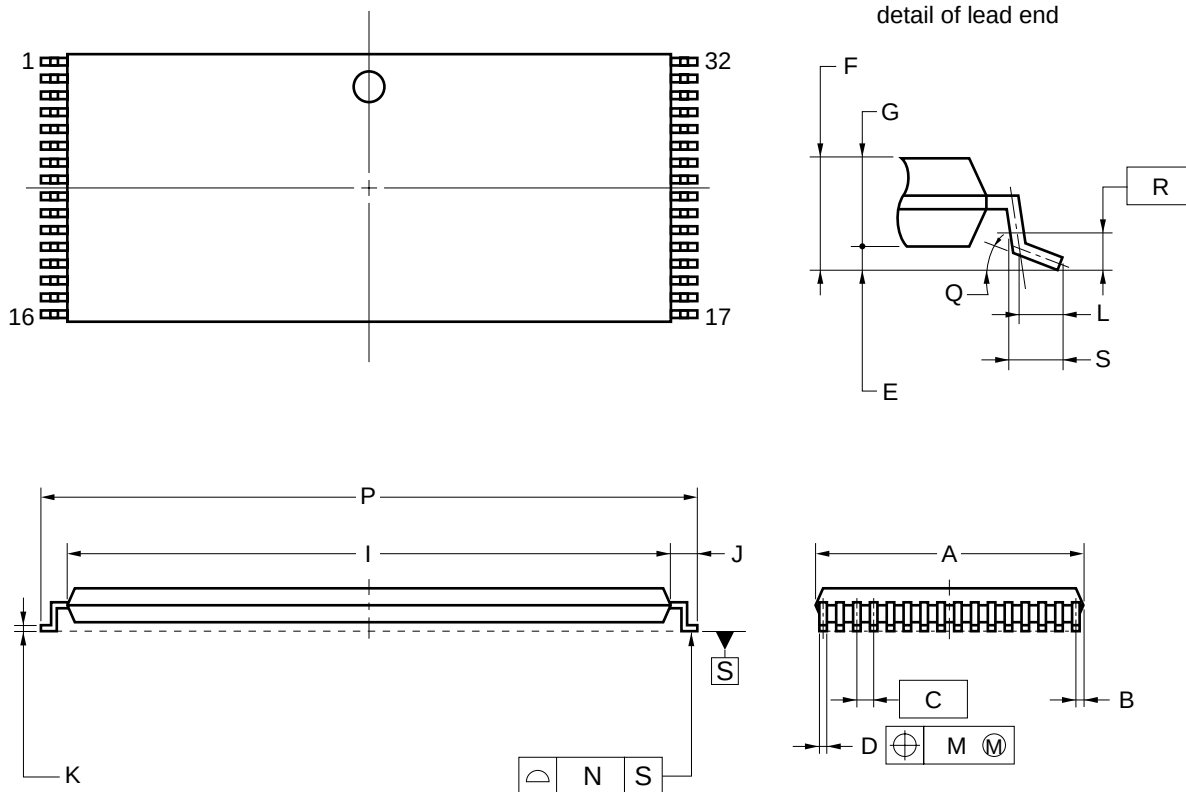
NOTES

1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

| ITEM | MILLIMETERS                               |
|------|-------------------------------------------|
| A    | 8.0±0.1                                   |
| B    | 0.45 MAX.                                 |
| C    | 0.5 (T.P.)                                |
| D    | 0.22±0.05                                 |
| G    | 1.0±0.05                                  |
| H    | 12.4±0.2                                  |
| I    | 11.8±0.1                                  |
| J    | 0.8±0.2                                   |
| K    | 0.145 <sup>+0.025</sup> <sub>-0.015</sub> |
| L    | 0.5                                       |
| M    | 0.08                                      |
| N    | 0.08                                      |
| P    | 13.4±0.2                                  |
| Q    | 0.1±0.05                                  |
| R    | 3° <sup>+5°</sup> <sub>-3°</sub>          |
| S    | 1.2 MAX.                                  |
| T    | 0.25                                      |
| U    | 0.6±0.15                                  |

P32GU-50-9KH-2

★ 32-PIN PLASTIC TSOP(I) (8x20)



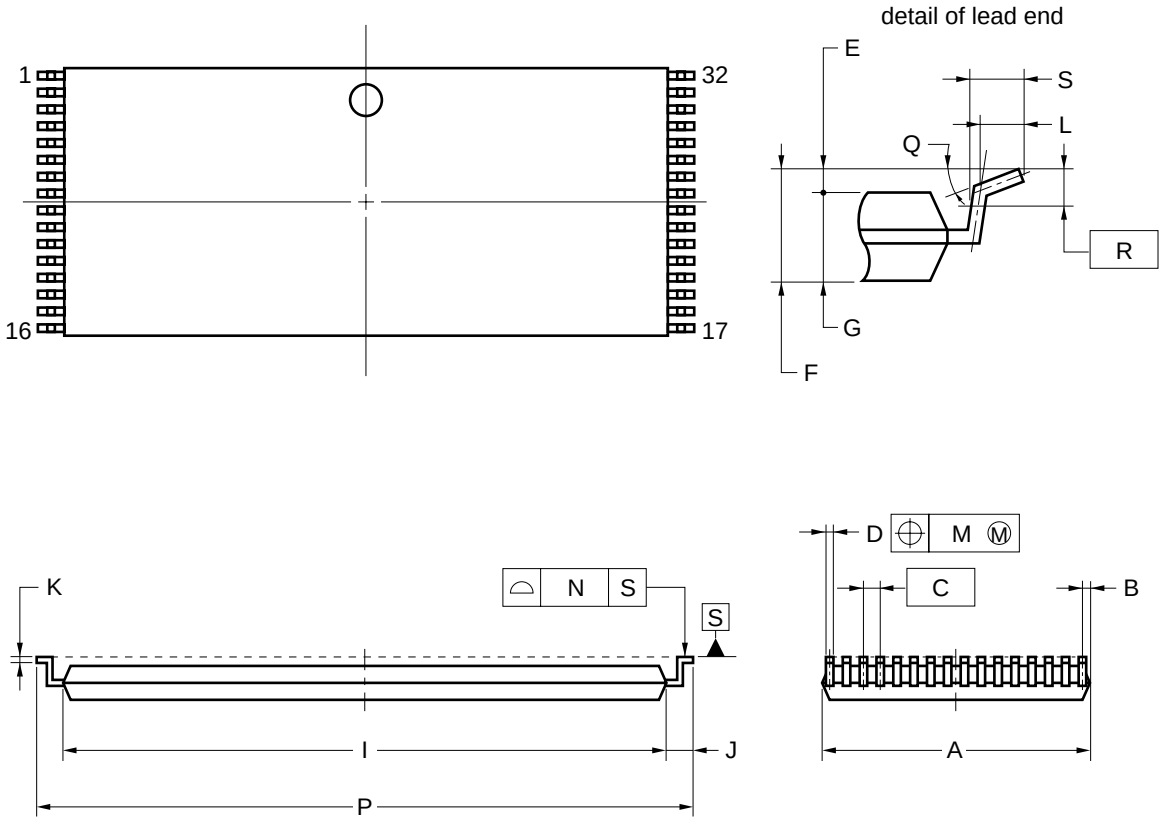
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

| ITEM | MILLIMETERS                      |
|------|----------------------------------|
| A    | 8.0±0.1                          |
| B    | 0.45 MAX.                        |
| C    | 0.5 (T.P.)                       |
| D    | 0.22±0.05                        |
| E    | 0.1±0.05                         |
| F    | 1.2 MAX.                         |
| G    | 0.97±0.08                        |
| I    | 18.4±0.1                         |
| J    | 0.8±0.2                          |
| K    | 0.145±0.05                       |
| L    | 0.5                              |
| M    | 0.10                             |
| N    | 0.10                             |
| P    | 20.0±0.2                         |
| Q    | 3° <sup>+5°</sup> <sub>-3°</sub> |
| R    | 0.25                             |
| S    | 0.60±0.15                        |

S32GZ-50-KJH1-2

★ 32-PIN PLASTIC TSOP(I) (8x20)



NOTES

- 1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
- 2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

| ITEM | MILLIMETERS                      |
|------|----------------------------------|
| A    | 8.0±0.1                          |
| B    | 0.45 MAX.                        |
| C    | 0.5 (T.P.)                       |
| D    | 0.22±0.05                        |
| E    | 0.1±0.05                         |
| F    | 1.2 MAX.                         |
| G    | 0.97±0.08                        |
| I    | 18.4±0.1                         |
| J    | 0.8±0.2                          |
| K    | 0.145±0.05                       |
| L    | 0.5                              |
| M    | 0.10                             |
| N    | 0.10                             |
| P    | 20.0±0.2                         |
| Q    | 3° <sup>+5°</sup> <sub>-3°</sub> |
| R    | 0.25                             |
| S    | 0.60±0.15                        |

S32GZ-50-KKH1-2

**Recommended Soldering Conditions**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD441000L-X.

★ **Types of Surface Mount Device**

|                            |                                                   |
|----------------------------|---------------------------------------------------|
| $\mu$ PD441000LGW-BxxX     | : 32-pin Plastic SOP (13.34 mm (525))             |
| $\mu$ PD441000LGW-CxxX     | : 32-pin Plastic SOP (13.34 mm (525))             |
| $\mu$ PD441000LGW-DxxX     | : 32-pin Plastic SOP (13.34 mm (525))             |
| $\mu$ PD441000LGU-BxxX-9JH | : 32-pin Plastic TSOP (I) (8×13.4) (Normal bent)  |
| $\mu$ PD441000LGU-CxxX-9JH | : 32-pin Plastic TSOP (I) (8×13.4) (Normal bent)  |
| $\mu$ PD441000LGU-DxxX-9JH | : 32-pin Plastic TSOP (I) (8×13.4) (Normal bent)  |
| $\mu$ PD441000LGU-BxxX-9KH | : 32-pin Plastic TSOP (I) (8×13.4) (Reverse bent) |
| $\mu$ PD441000LGU-CxxX-9KH | : 32-pin Plastic TSOP (I) (8×13.4) (Reverse bent) |
| $\mu$ PD441000LGU-DxxX-9KH | : 32-pin Plastic TSOP (I) (8×13.4) (Reverse bent) |
| $\mu$ PD441000LGZ-BxxX-KJH | : 32-pin Plastic TSOP (I) (8×20) (Normal bent)    |
| $\mu$ PD441000LGZ-CxxX-KJH | : 32-pin Plastic TSOP (I) (8×20) (Normal bent)    |
| $\mu$ PD441000LGZ-DxxX-KJH | : 32-pin Plastic TSOP (I) (8×20) (Normal bent)    |
| $\mu$ PD441000LGZ-BxxX-KKH | : 32-pin Plastic TSOP (I) (8×20) (Reverse bent)   |
| $\mu$ PD441000LGZ-CxxX-KKH | : 32-pin Plastic TSOP (I) (8×20) (Reverse bent)   |
| $\mu$ PD441000LGZ-DxxX-KKH | : 32-pin Plastic TSOP (I) (8×20) (Reverse bent)   |



[ MEMO ]

[ MEMO ]

## NOTES FOR CMOS DEVICES

**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:  
 "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.  
 "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots  
 "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)  
 "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.  
 The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.  
 (Note)  
 (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.  
 (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).