3-Channel LED Array Driver IC

Features

- Integrated 200V, 25Ω (typ.) MOSFETs
- Programmable output current to 80mA per channel
- TTL compatible PWM dimming inputs
- 3-Phase synchronous operation
- Leading edge blanking
- Short circuit protection with skip mode
- Over-temperature protection

Applications

- LCD panel backlighting
- DLP RPTV or projector LED engine driver
- RGB decorative lighting
- General LED lighting

General Description

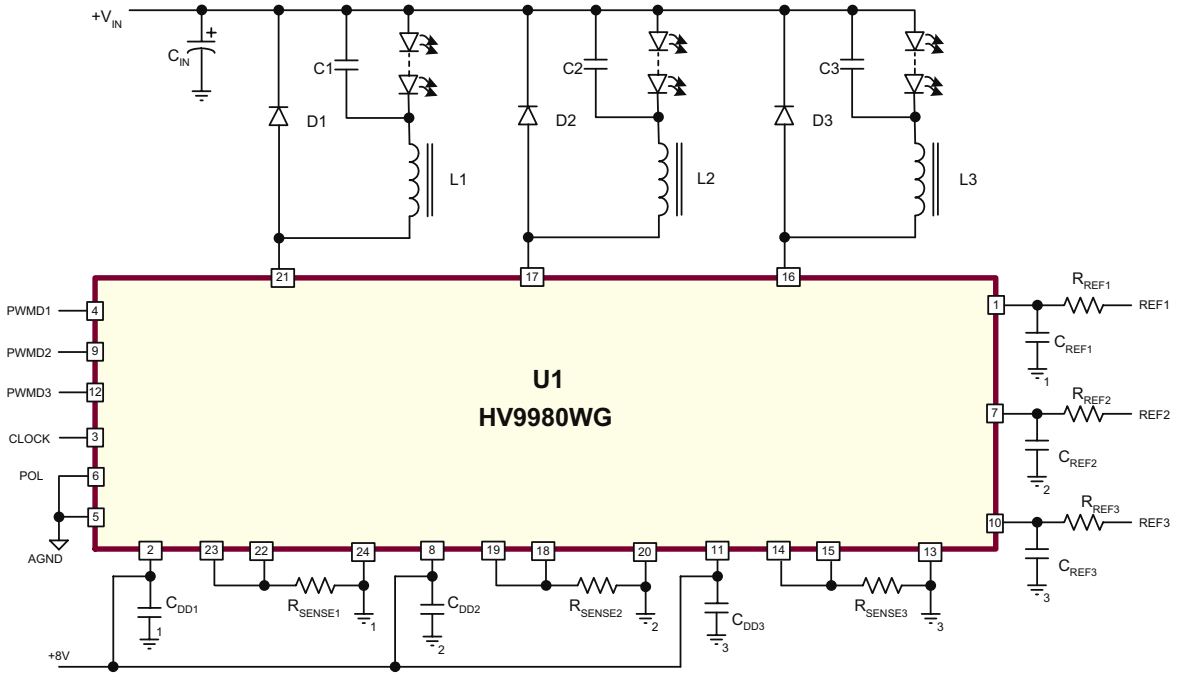
The HV9980 is a fully integrated 3-channel peak-current PWM controller for driving buck converters in constant output current mode. It is optimized for use with a large array of 20~80mA LED strings, where multiple HV9980 ICs are used sharing a common clock and a common reference voltage.

Both the clock and the voltage reference are external to the HV9980 for improved output current accuracy and uniform illumination. The output currents are programmed by controlling peak source current in each of the three internal 200V, 25Ω switching MOSFETs.

The peak current is detected by monitoring voltage at external sense resistors connected to RSENSE1-3. The switching MOSFET is turned off when the corresponding current sense signal exceeds the reference voltage applied at REF1-3 (in the case of normal output signal polarity). Beginning of the next switching cycle is determined by the external clock signal received at the CLK input. All three channels operate at a switching frequency of 1/6 of the external clock frequency and positioned 120º out-of-phase for the purpose of input and output ripple current reduction. Each channel is protected from an output short circuit condition. When an over-current condition is detected in the output switch (RSENSE1-3), the corresponding channel shuts down for 200us. HV9980 recovers automatically, when the short circuit condition is removed. Each current sense input (CS1-CS3) is equipped with a leading edge blanking delay to prevent false triggering of the current sense comparators due to circuit parasitics.

Over-temperature protection is included to prevent destructive failures due to over-heating. Programmable slope compensation is available at each CS input. AGND and PGND1-3 must be tied together on the printed circuit board. VDD1-3 must be also connected together on the PCB.

Typical Application Circuit

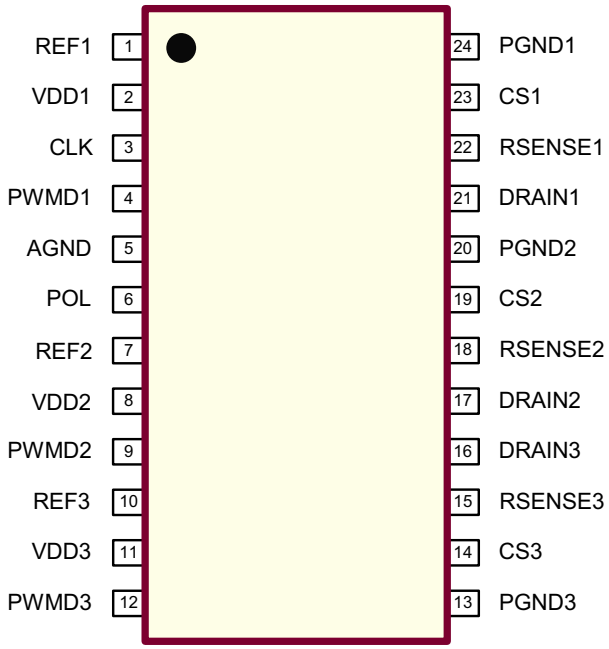


Ordering Information

Device	Package Option
	24-Lead SOW ***15.40x7.50 body*** ***2.65mm height (max)*** ***1.27mm pitch***
HV9980	HV9980WG-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



24-Lead SOW
(top view)

Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{DD}	-0.3V to +10V
Drain1-3 outputs	-0.3V to +200V
CS1-3 inputs	-0.3V to +5.0V
Other inputs and outputs	-0.3V to V_{DD}
Supply current, I_{DD}	+10mA
Power dissipation (T_A = +25°C)	1300mW
Thermal impedance (θ_{JA})	60°C/W
Operating ambient temperature range	-40°C to +85°C
Operating junction temperature range	-40°C to +125°C[1]
	-40°C to +150°C[2]
Storage temperature range	-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. All voltages referenced to ground.

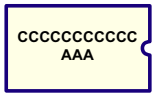
Notes:

1. *Operation out of this range will not guarantee electrical characteristics described in this datasheet.*
2. *Operation out of this range will be destructive to the IC.*

Product Marking

Top Marking

Bottom Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin
A = Assembler ID*
——— = "Green" Packaging

**May be part of top marking*

24-Lead SOW (WG)

Electrical Characteristics *(The specifications are at T_A = 25°C and V_{DD} = 8.0V, unless otherwise noted.)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
Supply Input (VDD1 - VDD3)							
$V_{DD(UVLO)}$	V_{DD} undervoltage threshold	*	-	-	5.3	V	VDD falling
$\Delta V_{DD(UVLO)}$	V_{DD} undervoltage hysteresis	-	-	500	-	mV	---
I_{DD}	Operating supply current	*	-	-	3.0	mA	Total of VDD1 - VDD3
High Voltage Switches (DRAIN1 - RSENSE1, DRAIN2 - RSENSE2, DRAIN3 - RSENSE3)							
V_{BR}	Breakdown voltage	*	210	-	-	V	---
R_{ON}	On-resistance	-	-	25	45	Ω	I_{DRAIN} = 50mA, V_{RSENSE} = 0V
I_{SAT}	DRAIN saturation current	*	200	-	-	mA	V_{DRAIN} = 120V, V_{RSENSE} = 1.3V

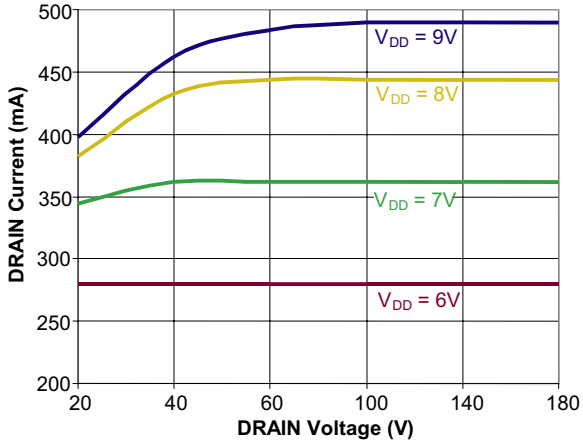
* *Denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +85°C.*

Electrical Characteristics *(cont.) (The specifications are at T_A = 25°C and V_{DD} = 8.0V, unless otherwise noted.)*

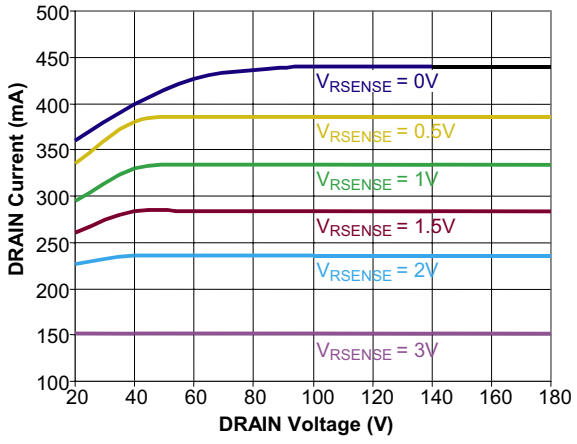
Sym	Parameter		Min	Typ	Max	Units	Conditions
Current Sense Comparators (CS1 - REF1, CS2 - REF2, CS3 - REF3)							
$V_{CS(LIM)}$	Short circuit protection threshold	*	1.0	-	1.3	V	---
T_{SKIP}	Short circuit recovery delay	-	-	200	-	µs	---
T_{BLANK}	Leading edge blanking delay	-	120	-	220	ns	---
V_{OS}	Input offset voltage	*	-7.0	-	7.0	mV	---
T_{DELAY}	Propagation delay CS-to-DRAIN	*	-	-	150	ns	V_{CS} - V_{REF} = 50mV
$T_{DELAY(LIM)}$	Shutdown delay CS-to-DRAIN	*	-	-	0.5	µs	V_{CS} = $V_{CS(LIM)}$ + 100mV, V_{REF} > $V_{CS(LIM)}$
Oscillator Input and Frequency Divider (CLK)							
$F_{SW(max)}$	Maximum switching frequency	*	500	-	-	kHz	f_{CLK} = 3.0MHz
K_{SW}	Frequency divider ratio	-	-	6	-	-	Guaranteed by design
φ_2	DRAIN1-DRAIN2 phase delay	-	-	120	-	deg	Guaranteed by design
φ_3	DRAIN1-DRAIN3 phase delay	-	-	240	-	deg	Guaranteed by design
T_{OFF}	CLK high time	-	50	-	-	ns	---
T_{ON}	CLK low time	-	50	-	-	ns	---
$V_{CLK,HI}$	CLK Input high	*	2.0	-	-	V	---
$V_{CLK,LO}$	CLK Input low	*	-	-	0.8	V	---
PWM Dimming (PWMD1, PWMD2, PWMD3)							
$V_{PWMD,HI}$	PWMD Input high	*	2.0	-	-	V	---
$V_{PWMD,LO}$	PWMD Input low	*	-	-	0.8	V	---
R_{PWMD}	PWMD Pull down resistance	-	100	200	300	kΩ	PWMD = 5.0V
Over Temperature Protection							
T_{OT}	Over temperature trip limit	-	125	140	-	°C	Guaranteed by design
T_{HYST}	Temperature hysteresis	-	-	60	-	°C	Guaranteed by design

* *Denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +85°C.*

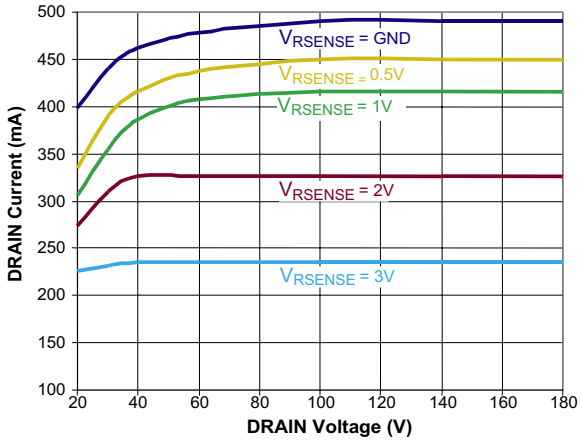
Typical Performance Characteristics *(T_J = 25°C unless otherwise noted)*



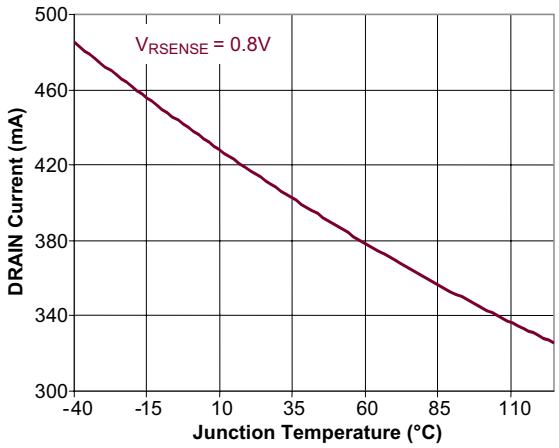
Output Saturation Current
(I_{DRAIN} vs. V_{DRAIN} at V_{RSENSE} = 0V)



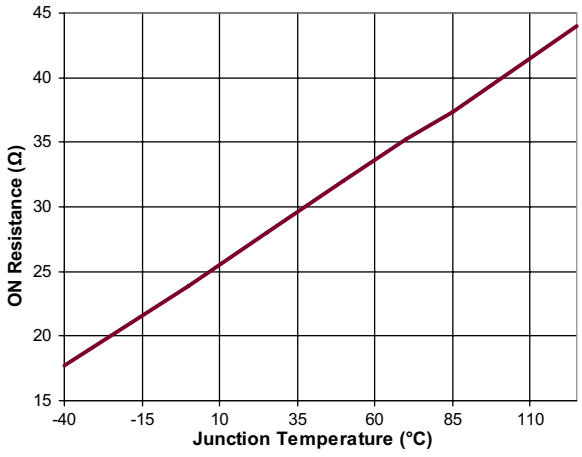
Output Saturation Current
(I_{DRAIN} vs. V_{DRAIN} at V_{DD} = 8.0V)



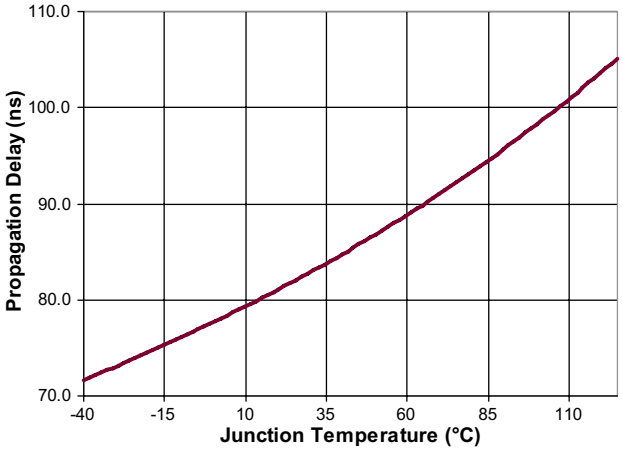
Output Saturation Current
(I_{DRAIN} vs. V_{DRAIN} at V_{DD} = 9.0V)



Output Saturation Current
(I_{DRAIN} vs. T_J at V_{DD} = 9.0V)

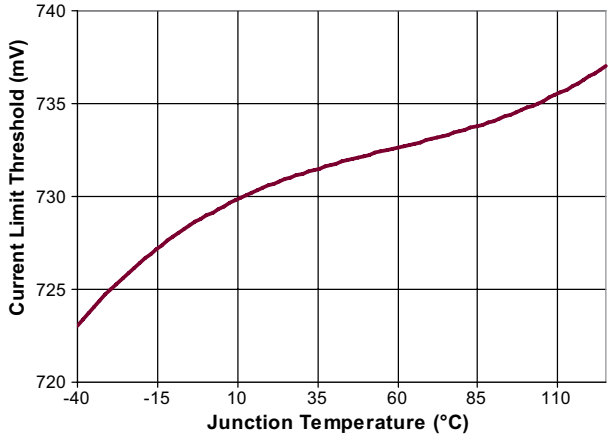


ON Resistance
(R_{ON} vs. T_J at V_{DD} = 8.0 or 9.0V)

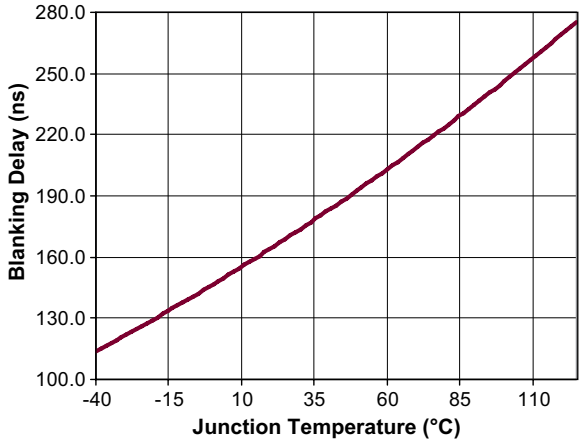


CS-to-DRAIN Propagation Delay
(T_{DELAY} vs. T_J at V_{DD} = 8.0 or 9.0V)

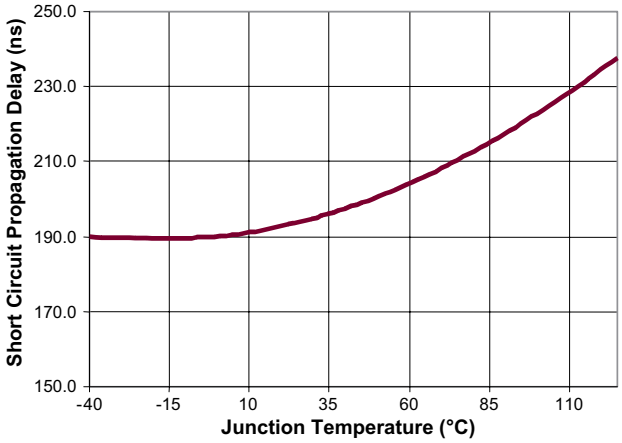
Typical Performance Characteristics *(cont.)* (T_J = 25°C unless otherwise noted)



Short Circuit Threshold Voltage
($V_{CS(LIM)}$ vs. T_J at V_{DD} = 8.0 or 9.0V)



Leading Edge Blanking Delay
(T_{BLANK} vs. T_J at V_{DD} = 8.0 or 9.0V)



Short Circuit Protection Delay
($T_{DELAY(LIM)}$ vs. T_J at V_{DD} = 8.0 or 9.0V)

Figure 1: 110-190VDC 3-channel 50V 70mA LED Driver Schematic

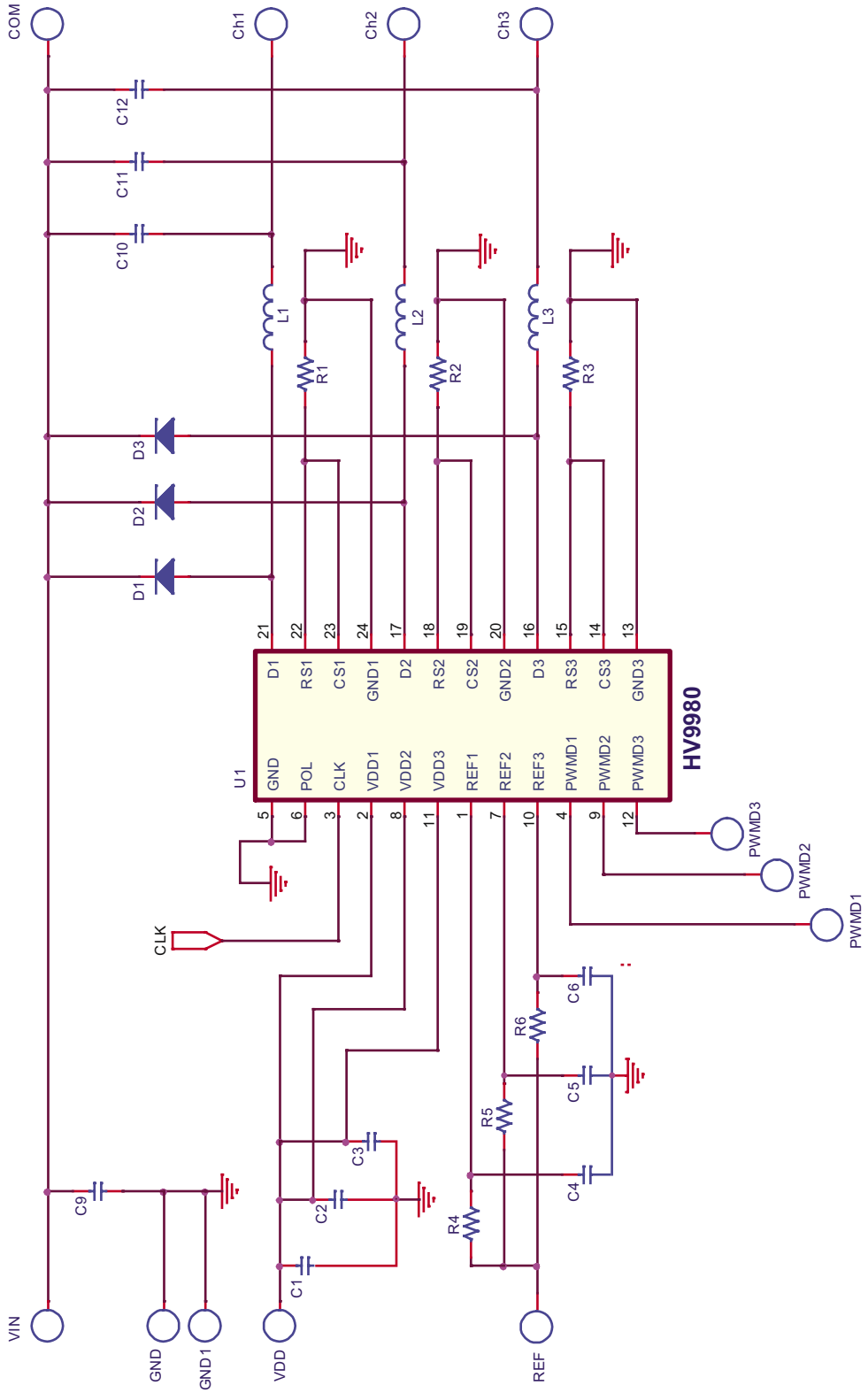
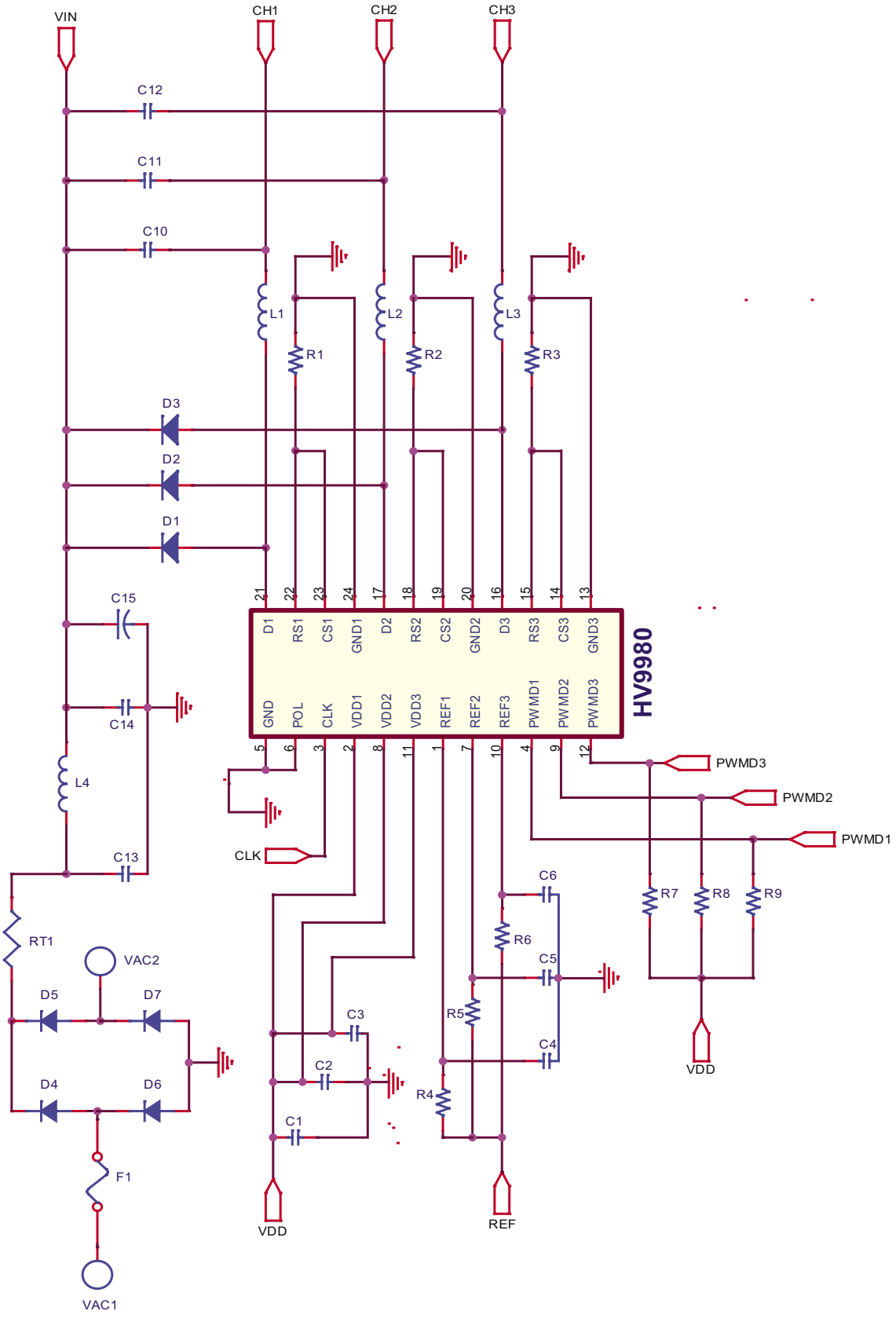


Figure 2: 90-135VAC 3-channel 50V 70mA LED Driver Schematic



Application Information

Programming LED current and selecting L and D

The required value of the output inductor L is inversely proportional to the ripple current ΔI_O in it. Setting the relative peak-to-peak ripple to 20~30% is a good practice to ensure noise immunity of the current sense comparator.

$$L = (V_O \bullet T_{OFF}) / \Delta I_O = (V_O \bullet [1 - D]) / f_S \Delta I_O \quad (1)$$

V_O is the forward voltage of the LED string, f_S is the switching frequency, $D = V_O/V_{IN}$ is the switching duty cycle.

The output current in the LED string (I_O) is calculated as:

$$I_O = (V_{REF} / R_{SENSE}) - 1/2 \bullet \Delta I_O \quad (2)$$

where V_{REF} is the voltage at REF1-3, and R_{SENSE} is the current sense resistor at RSENSE1-3. (The ripple current introduces a peak-to-average error in the output current setting that needs to be accounted for.)

Adding a filter capacitor across the LED string can reduce the output current ripple yielding a reduced value of *L*. However, one must keep in mind that the peak-to-average current error is affected by the variation of the input and output voltage. Therefore, the line and load regulation of the LED current might be sacrificed at large ripple current in *L*.

Another important aspect of designing an LED driver with the HV9980 is related to certain parasitic elements of the circuit, including distributed coil capacitance of L1, junction capacitance and reverse recovery of the rectifier diode D1, capacitance of the printed circuit board traces C_{PCB} and output capacitance C_{DRAIN} of the controller itself. These parasitic elements affect the efficiency of the switching converter and could potentially cause false triggering of the current sense comparator if not properly managed. Minimizing these parasitics is essential for efficient and reliable operation of the HV9980.

Coil capacitance of inductors is typically provided in the manufacturer's data books either directly or in terms of the self-resonant frequency (SRF).

$$SRF = 1 / (2\pi\sqrt{L \bullet C_L})$$

where *L* is the inductance value, and C_L is the coil capacitance.) Charging and discharging this capacitance every switching cycle causes high-current spikes in the LED string. Therefore, connecting a small capacitor C_O (~10nF) is recommended to bypass these spikes.

Using an ultra-fast rectifier diode for D1 is recommended to achieve high efficiency and reduce the risk of false triggering of the current sense comparator. Using diodes with shorter reverse recovery time t_{rr} and lower junction capacitance C_J achieves better performance. The reverse voltage rating V_R of the diode must be greater than the maximum input voltage of the LED lamp.

The total parasitic capacitance present at the DRAIN output of the HV9980 can be calculated as:

$$C_P = C_{DRAIN} + C_{PCB} + C_L + C_J \quad (3)$$

When the switch turns on, the capacitance C_P is discharged into the DRAIN output of the IC. The discharge current is limited to about 300mA typically. However, it may become lower at increased junction temperature. The duration of the leading edge current spike can be estimated as:

$$T_{SPIKE} = [(V_{IN} \bullet C_P) / I_{SAT}] = t_{rr} \quad (4)$$

In order to avoid false triggering of the current sense comparator, C_P must be minimized in accordance with the following expression:

$$C_P < [I_{SAT} \bullet (T_{BLANK(MIN)} - t_{rr})] / V_{IN(MAX)} \quad (5)$$

where $T_{BLANK(MIN)}$ is the minimum blanking time of 120ns, and $V_{IN(MAX)}$ is the maximum instantaneous input voltage.

Layout Considerations

The HV9980 provides three independent power ground connections PGND1-3 for each channel. The PGND pins must be wired together on the printed circuit board (PCB). To minimize interference between the channels, the PGND pins should be wired to the negative terminal of the input filter capacitor CIN using separate tracks. All four power supply inputs VDD, VDD1-3 must be connected together on the PCB also.

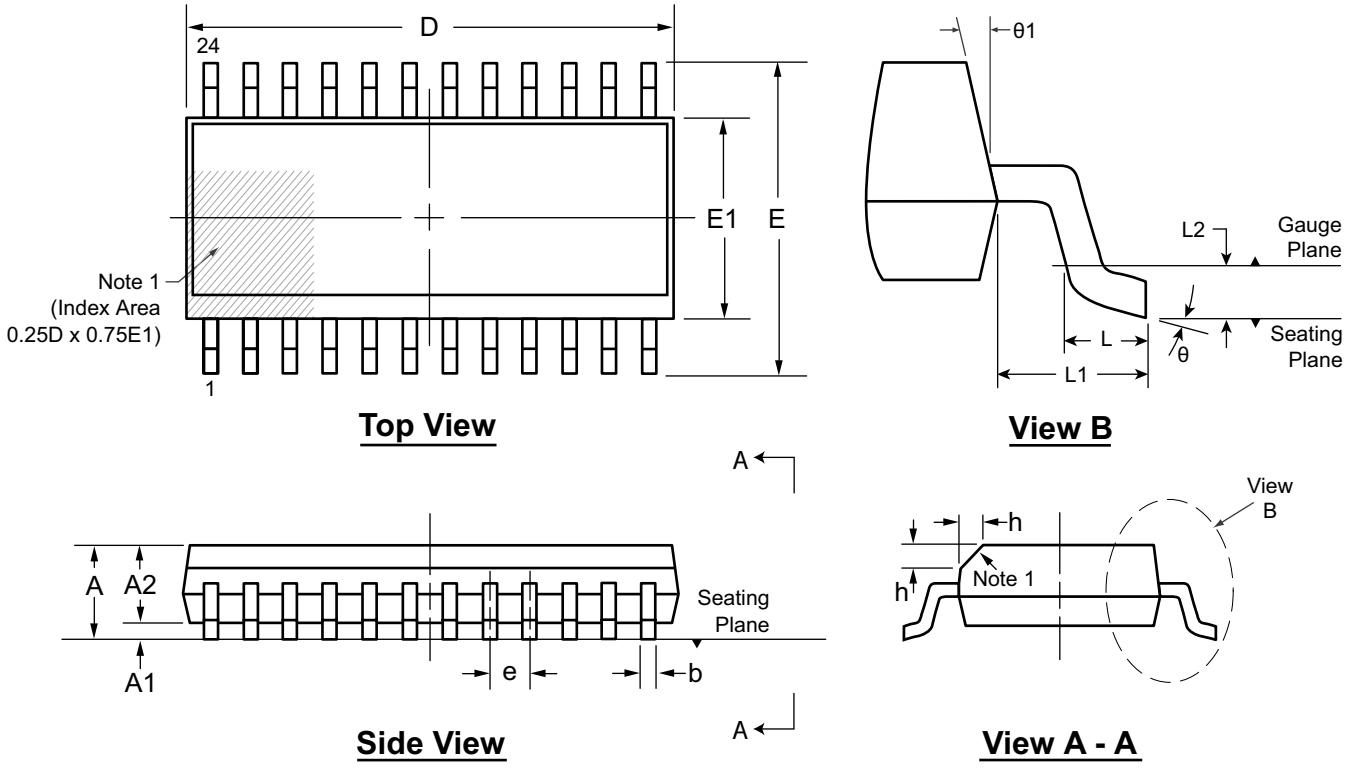
Although in many layout arrangements wiring the reference pins REF1-3 together is acceptable, further reduction of the "cross-talk" between the channels is possible by adding low-pass RC filters with the filter capacitors referenced to the corresponding PGND pins. These filters composed from R_{REF1-3} and C_{REF1-3} are shown in the Typical Application Circuit diagram.

Pin Description

Pin #	Name	Description
1	REF1	Voltage reference inputs to the current sense comparators. For best noise immunity, connect an RC filter at each of these pins referenced to the corresponding PGND pin. The filter can consist of a 1.0nF low impedance capacitor and a 1.0kΩ resistor.
7	REF2	
10	REF3	
2	VDD1	Power supply inputs. For best noise immunity, bypass each of these pins to the corresponding PGND pin with a 0.1uF low impedance capacitor. The VDD pins must be tied together on the PCB.
8	VDD2	
11	VDD3	
3	CLK	Input to an external clock signal common to all three channels. Programs the switching frequency of the power MOSFET outputs at 1/6 of the clock signal frequency.
4	PWMD1	Dedicated PWM dimming inputs for each individual LED string driver channel.
9	PWMD2	
12	PWMD3	
5	AGND	Common return pin for CLK, POL and PWMD inputs.
6	POL	Must be connected to AGND.
13	PGND3	Power return terminals for corresponding DRAIN outputs. The PGND and AGND pins must be tied together on the PCB.
20	PGND2	
24	PGND1	
14	CS3	Signal inputs to the current sense comparators. Connect these pins to the corresponding RSENSE outputs directly when the slope compensation feature is not used. When the slope compensation is needed, connect a capacitor between each RSENSE and its corresponding CS pin, and connect a resistor between each CS pin and VDD.
19	CS2	
23	CS1	
15	RSENSE3	Open source outputs of the switching power MOSFETs. Connect a current sense resistor between each of the RSENSE pins and its corresponding PGND pin.
18	RSENSE2	
22	RSENSE1	
16	DRAIN3	Open drain outputs of the switching power MOSFETs.
17	DRAIN2	
21	DRAIN1	

24-Lead SOW (Wide Body) Package Outline (WG)

15.40x7.50 body, 2.65mm height (max), 1.27mm pitch



Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 Identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.15*	0.10	2.05	0.31	15.20*	9.97*	7.40*	1.27 BSC	0.25	0.40	1.40 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	15.40	10.30	7.50		-	-			-	-
	MAX	2.65	0.30	2.55*	0.51	15.60*	10.63*	7.60*		0.75	1.27			8°	15°

JEDEC Registration MS-013, Variation AD, Issue E, Sep. 2005.

** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*

Drawings are not to scale.

***Supertex Doc. #:** DSPD-24SOWWG, Version D090408.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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