HM5116400 Series
HM5117400 Series

4,194,304-word × 4-bit Dynamic RAM

HITACHI

ADE-203-648C (Z)
Rev. 3.0
Feb. 27, 1997

Description

The Hitachi HM5116400 Series, HM5117400 Series are CMOS dynamic RAMs organized 4,194,304-word × 4-bit. They employ the most advanced 0.5 µm CMOS technology for high performance and low power. The HM5116400 Series, HM5117400 Series offer Fast Page Mode as a high speed access mode. They have package variations of standard 300-mil 26-pin plastic SOJ and standard 300-mil 26-pin plastic TSOP.

Features

- Single 5 V (±10%)
- Access time: 50 ns/60 ns/70 ns (max)
- Power dissipation
  - Active mode : 495 mW/440 mW/385 mW (max) (HM5116400 Series)
    : 550 mW/495 mW/440 mW (max) (HM5117400 Series)
  - Standby mode : 11 mW (max)
    : 0.83 mW (max) (L-version)
- Fast page mode capability
- Long refresh period
  - 4096 refresh cycles : 64 ms (HM5116400 Series)
    : 128 ms (L-version)
  - 2048 refresh cycles : 32 ms (HM5117400 Series)
    : 128 ms (L-version)
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- Battery backup operation (L-version)
- Test function
  - 16-bit parallel test mode

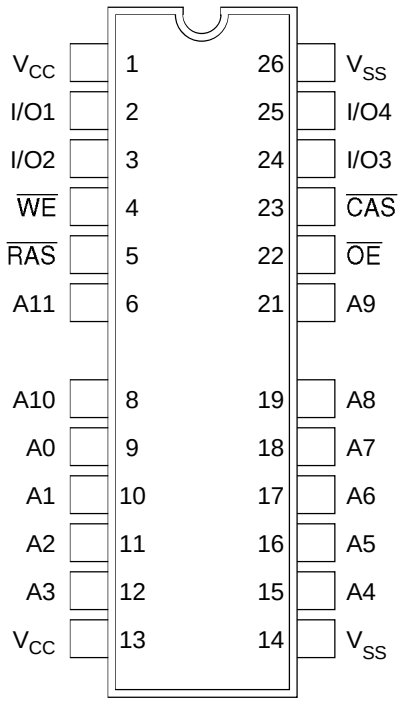
Hitachi semiconductor

Ordering Information

Type No.	Access time	Package
HM5116400S-5	50 ns	300-mil 26-pin plastic SOJ (CP-26/24DB)
HM5116400S-6	60 ns	
HM5116400S-7	70 ns	
HM5116400LS-5	50 ns	
HM5116400LS-6	60 ns	
HM5116400LS-7	70 ns	
HM5117400S-5	50 ns	
HM5117400S-6	60 ns	
HM5117400S-7	70 ns	
HM5117400LS-5	50 ns	
HM5117400LS-6	60 ns	
HM5117400LS-7	70 ns	
HM5116400TS-5	50 ns	300-mil 26-pin plastic TSOP II (TTP-26/24DA)
HM5116400TS-6	60 ns	
HM5116400TS-7	70 ns	
HM5116400LTS-5	50 ns	
HM5116400LTS-6	60 ns	
HM5116400LTS-7	70 ns	
HM5117400TS-5	50 ns	
HM5117400TS-6	60 ns	
HM5117400TS-7	70 ns	
HM5117400LTS-5	50 ns	
HM5117400LTS-6	60 ns	
HM5117400LTS-7	70 ns	

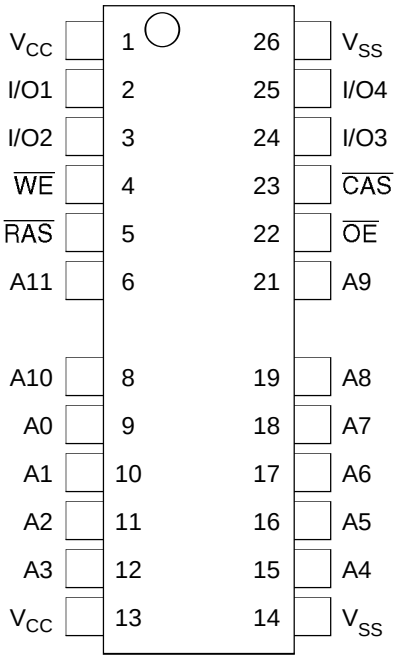
Pin Arrangement

HM5116400S/LS Series



(Top view)

HM5116400TS/LTS Series



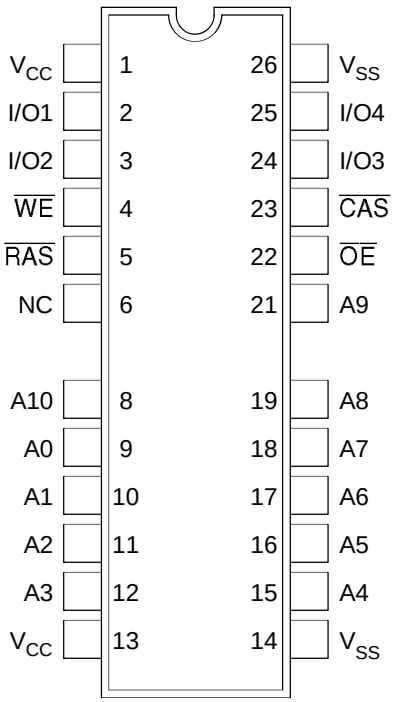
(Top view)

Pin Description

Pin name	Function	
A0 to A11	Address input	
	— Row/Refresh address	A0 to A11
	— Column address	A0 to A9
I/O1 to I/O4	Data input/Data output	
$\overline{RAS}$	Row address strobe	
$\overline{CAS}$	Column address strobe	
$\overline{WE}$	Write enable	
$\overline{OE}$	Output enable	
V_{CC}	Power supply	
V_{SS}	Ground	

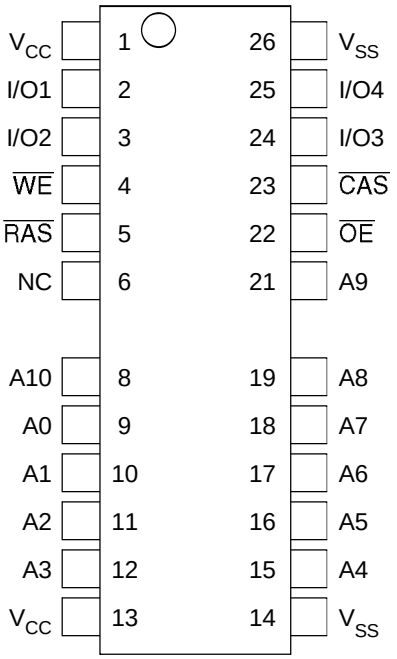
Pin Arrangement

HM5117400S/LS Series



(Top view)

HM5117400TS/LTS Series

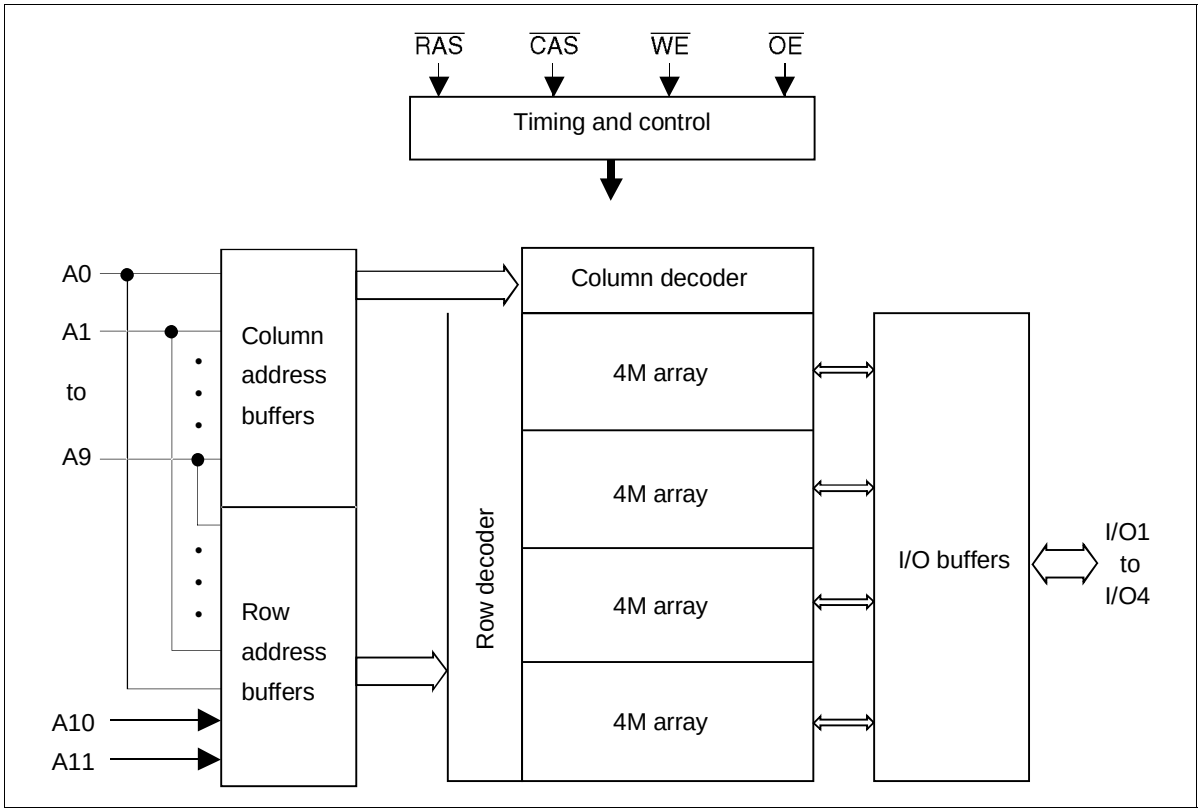


(Top view)

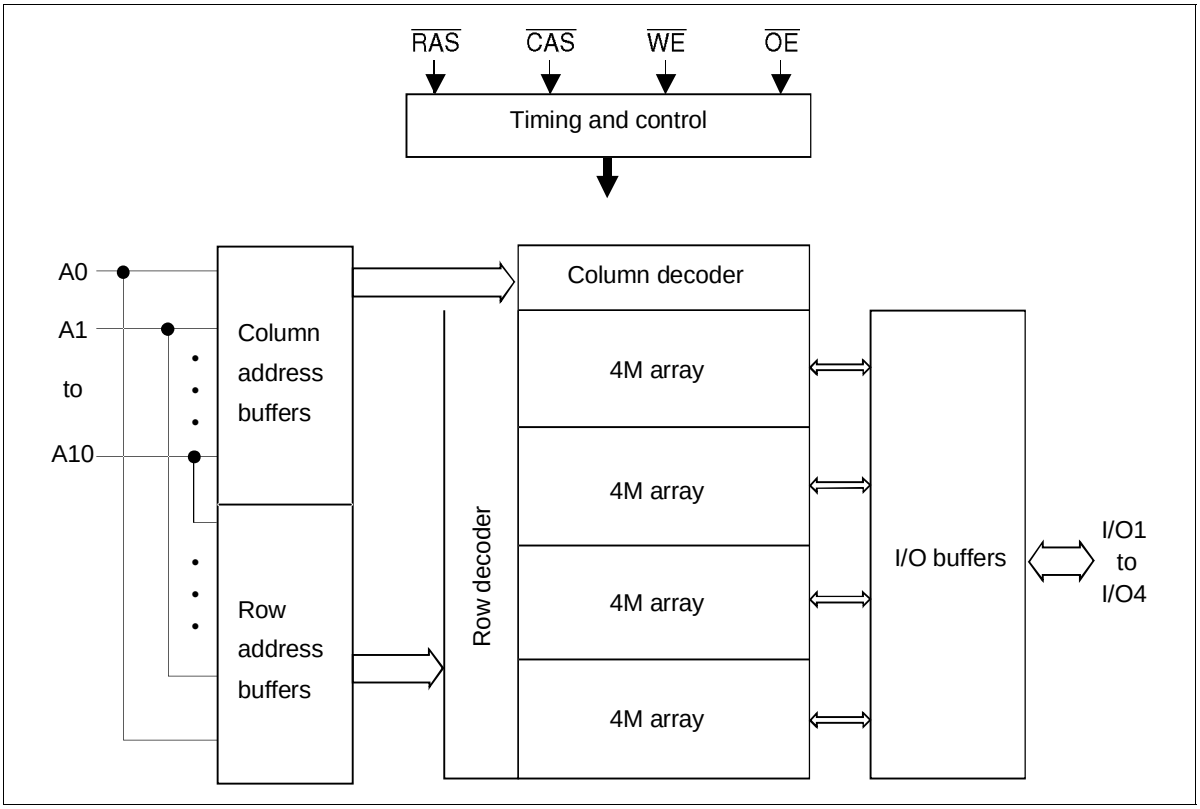
Pin Description

Pin name	Function
A0 to A10	Address input — Row/Refresh address A0 to A10 — Column address A0 to A10
I/O1 to I/O4	Data input/Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram (HM5116400 Series)



Block Diagram (HM5117400 Series)



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70˚C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics

(Ta = 0 to +70˚C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (HM5116400 Series)

		HM5116400							
		-5		-6		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current*1, *2	I_{CC1}	—	90	—	80	—	70	mA	t_{RC} = min
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
Standby current (L-version)	I_{CC2}	—	150	—	150	—	150	µA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*2	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = min
Standby current*1	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = min
Fast page mode current*1, *3	I_{CC7}	—	80	—	70	—	60	mA	t_{PC} = min
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	350	—	350	—	350	µA	CMOS interface Dout = High-Z, CBR refresh: t_{RC} = 31.3 µs t_{RAS} ≤ 0.3 µs
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

DC Characteristics

(Ta = 0 to +70˚C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (HM5117400 Series)

		HM5117400							
		-5		-6		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current*1, *2	I_{CC1}	—	100	—	90	—	80	mA	t_{RC} = min
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
Standby current (L-version)	I_{CC2}	—	150	—	150	—	150	µA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*2	I_{CC3}	—	100	—	90	—	80	mA	t_{RC} = min
Standby current*1	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	100	—	90	—	80	mA	t_{RC} = min
Fast page mode current*1, *3	I_{CC7}	—	90	—	80	—	70	mA	t_{PC} = min
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	350	—	350	—	350	µA	CMOS interface Dout = High-Z, CBR refresh: t_{RC} = 62.5 µs t_{RAS} ≤ 0.3 µs
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25˚C, V_{CC} = 5 V ±10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70˚C, V_{CC} = 5 V ±10%, V_{SS} = 0 V) *1, *2, *18, *19

Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM5116400/HM5117400							
		-5		-6		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	90	—	110	—	130	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10000	15	10000	18	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	7	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	7	—	10	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	20	52	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	15	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	13	—	15	—	18	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	50	—	60	—	70	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	13	—	15	—	18	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7

Read Cycle

		HM5116400/HM5117400							
		-5		-6		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	8, 9, 20
Access time from $\overline{CAS}$	t_{CAC}	—	13	—	15	—	18	ns	9, 10, 17, 20
Access time from address	t_{AA}	—	25	—	30	—	35	ns	9, 11, 17, 20
Access time from $\overline{OE}$	t_{OEA}	—	13	—	15	—	18	ns	9, 20
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	—	30	—	35	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	25	—	30	—	35	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	—	15	ns	13
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	13	—	15	—	15	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	13	—	15	—	18	—	ns	5

Write Cycle

		HM5116400/HM5117400							
		-5		-6		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t_{WCH}	7	—	10	—	15	—	ns	
Write command pulse width	t_{WP}	7	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	—	15	—	18	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	—	15	—	18	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t_{DH}	7	—	10	—	15	—	ns	15

Read-Modify-Write Cycle

		HM5116400/HM5117400							
		-5		-6		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	131	—	155	—	181	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	73	—	85	—	98	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	36	—	40	—	46	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	48	—	55	—	63	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	13	—	15	—	18	—	ns	

Refresh Cycle

		HM5116400/HM5117400							
		-5		-6		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	7	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	7	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	5	—	ns	

Fast Page Mode Cycle

		HM5116400/HM5117400							
		-5		-6		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode cycle time	t_{PC}	35	—	40	—	45	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	30	—	35	—	40	ns	9, 17, 20
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	30	—	35	—	40	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HM5116400/HM5117400							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode read-modify-write cycle time	t_{PRWC}	76	—	85	—	96	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	53	—	60	—	68	—	ns	14

Test Mode Cycle *[19]

		HM5116400/HM5117400							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Test mode $\overline{WE}$ setup time	t_{WTS}	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WTH}	7	—	10	—	10	—	ns	

Refresh (HM5116400 Series)

Parameter	Symbol	Max	Unit	Notes
Refresh	t_{REF}	64	ms	4096 cycles
Refresh (L-version)	t_{REF}	128	ms	4096 cycles

Refresh (HM5117400 Series)

Parameter	Symbol	Max	Unit	Notes
Refresh period	t_{REF}	32	ms	2048 cycles
Refresh period (L-version)	t_{REF}	128	ms	2048 cycles

Notes:
1. AC measurements assume t_T = 5 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in Fast page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
19. The 16M DRAM offers a 16-bit time saving parallel test mode. Address CA0 and CA1 for the 4M × 4 are don't care during test mode. Test mode is set by performing a $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) cycle. In 16-bit parallel test mode, data is written into 4 bits in parallel at each I/O (I/O1 to I/O4) and read out from each I/O.

    If 4 bits of each I/O are equal (all 1s or 0s), data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed.

    Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.

    To get out of test mode and enter a normal operation mode, perform either a regular $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle or $\overline{RAS}$-only refresh cycle.
20. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

21. XXX: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))
    ///////: Invalid Dout
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

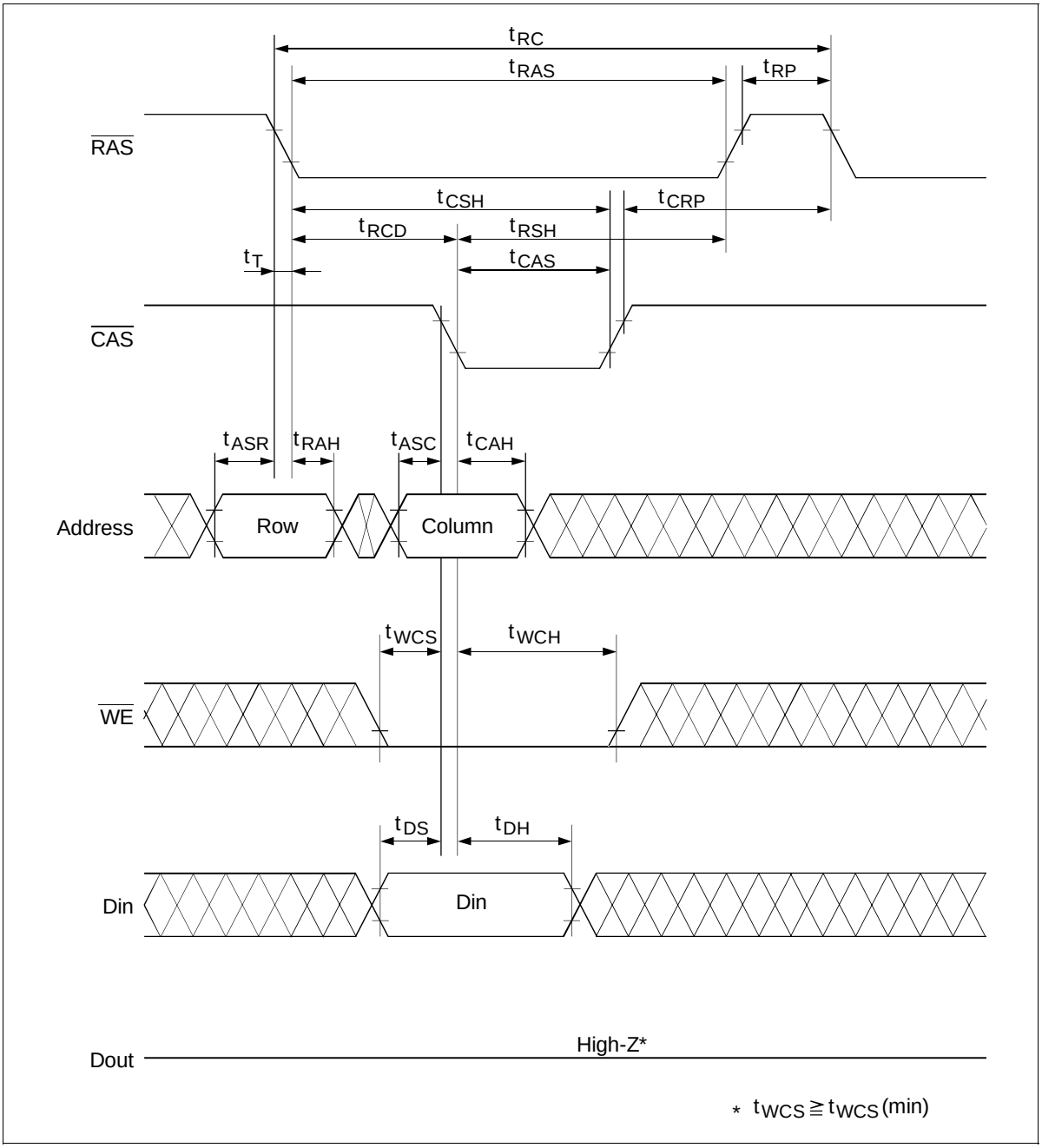
Notes:
1. AC measurements assume t_T = 5 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in Fast page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
19. The 16M DRAM offers a 16-bit time saving parallel test mode. Address CA0 and CA1 for the 4M × 4 are don't care during test mode. Test mode is set by performing a $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) cycle. In 16-bit parallel test mode, data is written into 4 bits in parallel at each I/O (I/O1 to I/O4) and read out from each I/O.

    If 4 bits of each I/O are equal (all 1s or 0s), data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed.

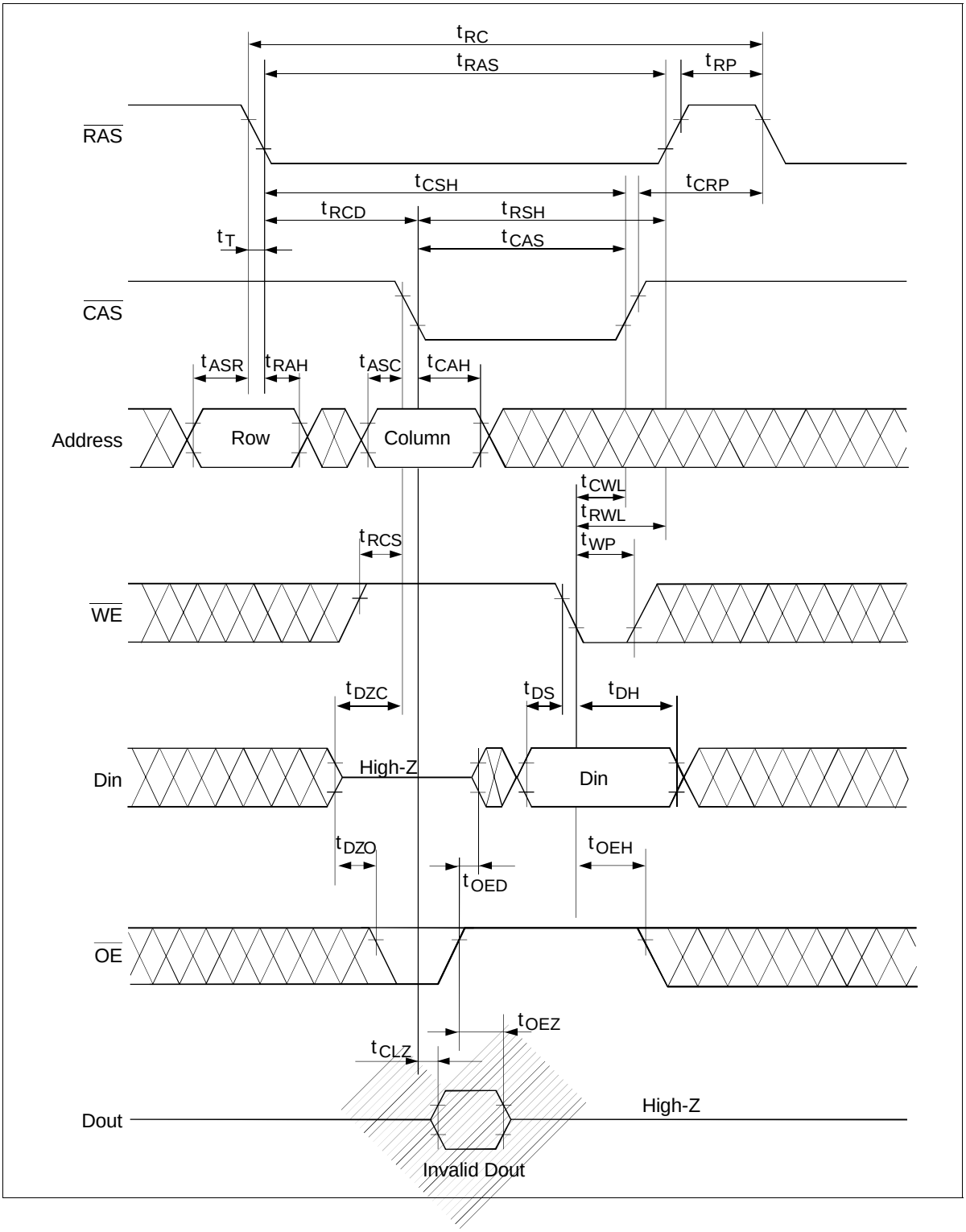
    Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.

    To get out of test mode and enter a normal operation mode, perform either a regular $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle or $\overline{RAS}$-only refresh cycle.
20. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

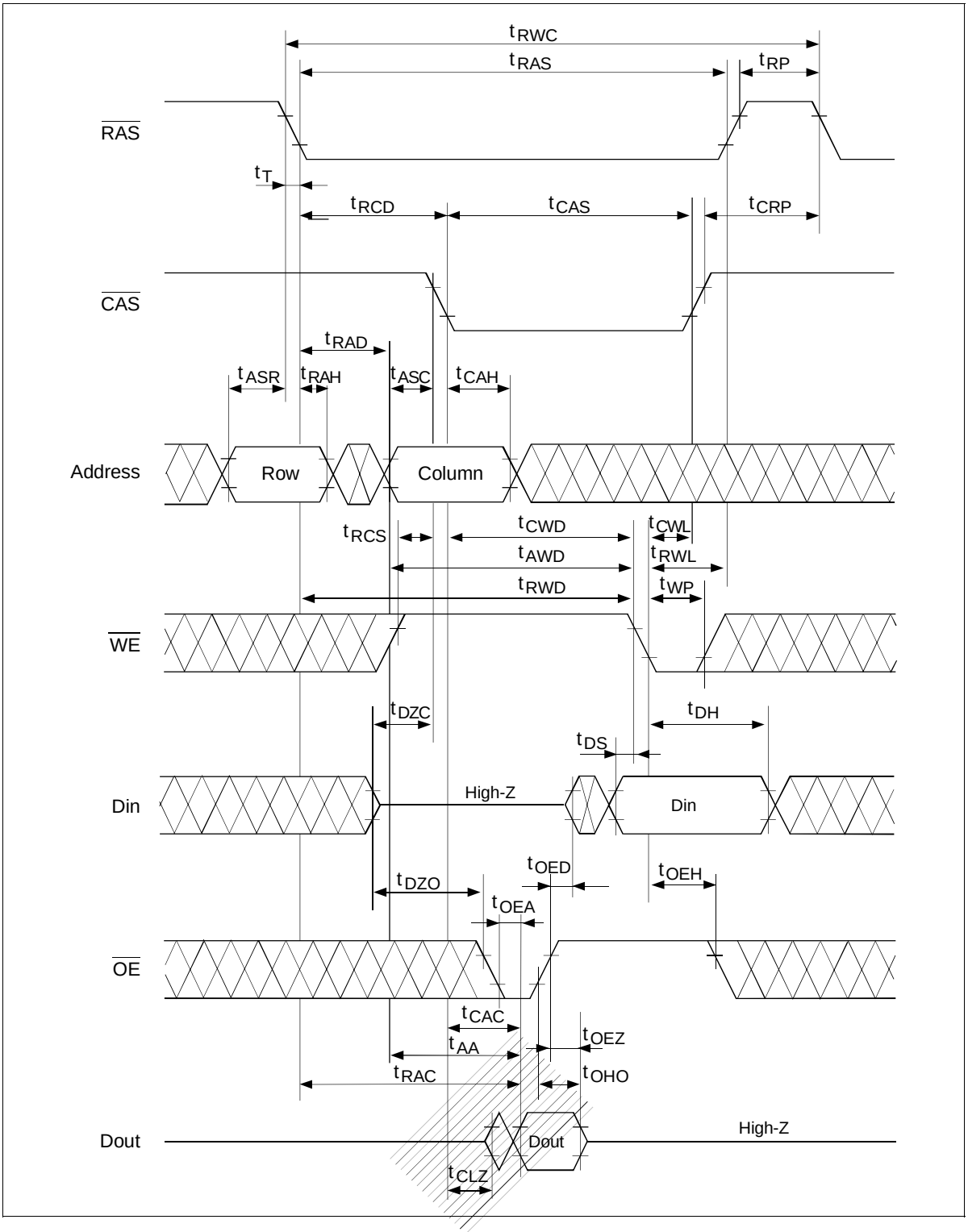
Early Write Cycle



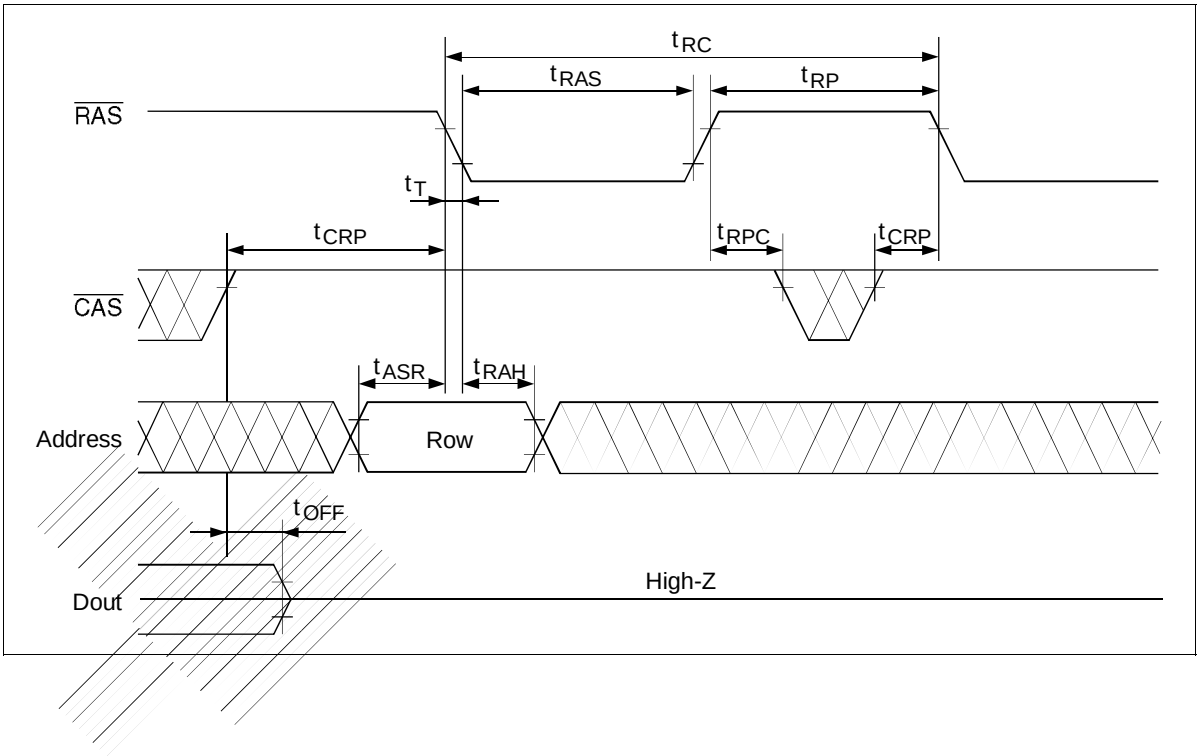
Delayed Write Cycle*[18]



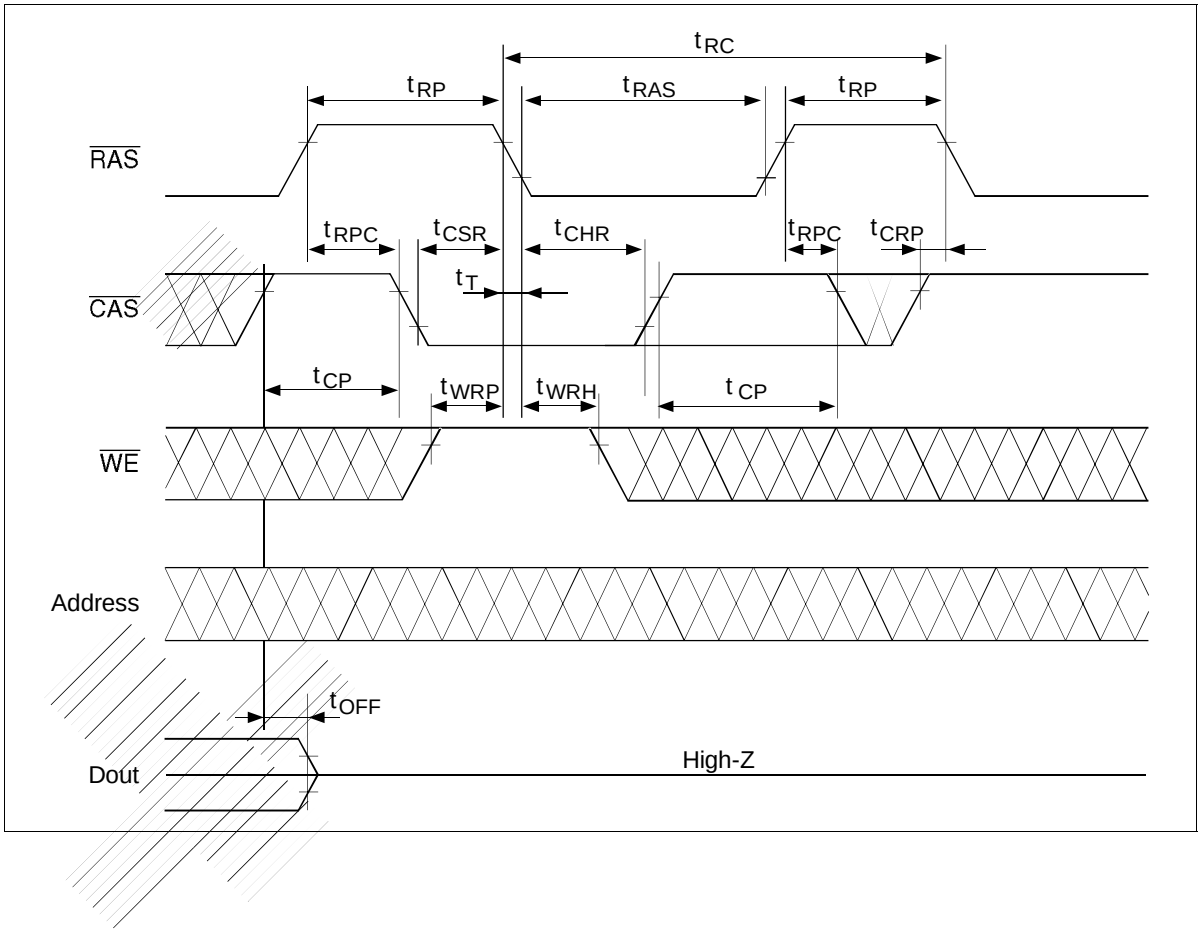
Read-Modify-Write Cycle*[18]



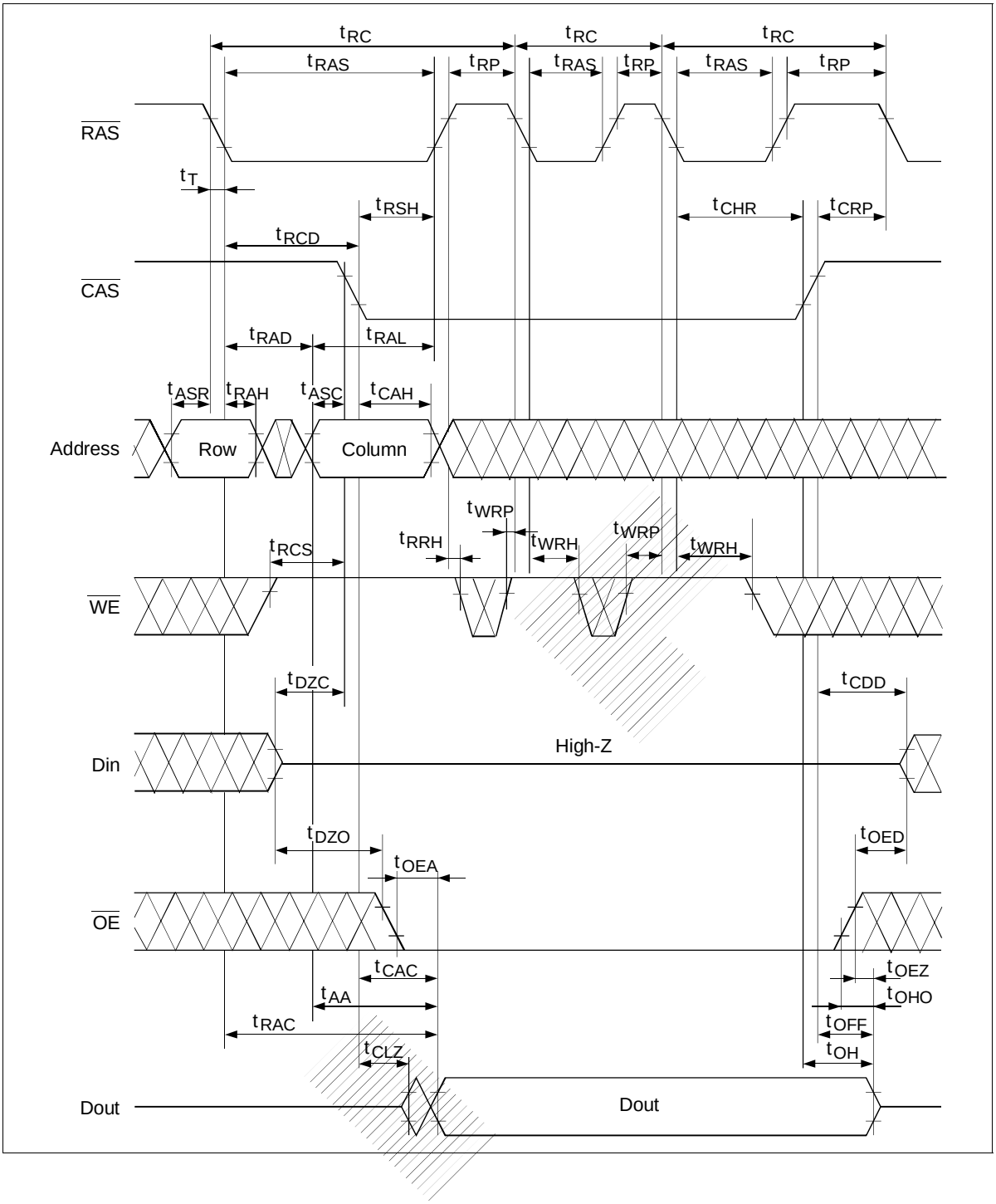
$\overline{\text{RAS}}$-Only Refresh Cycle



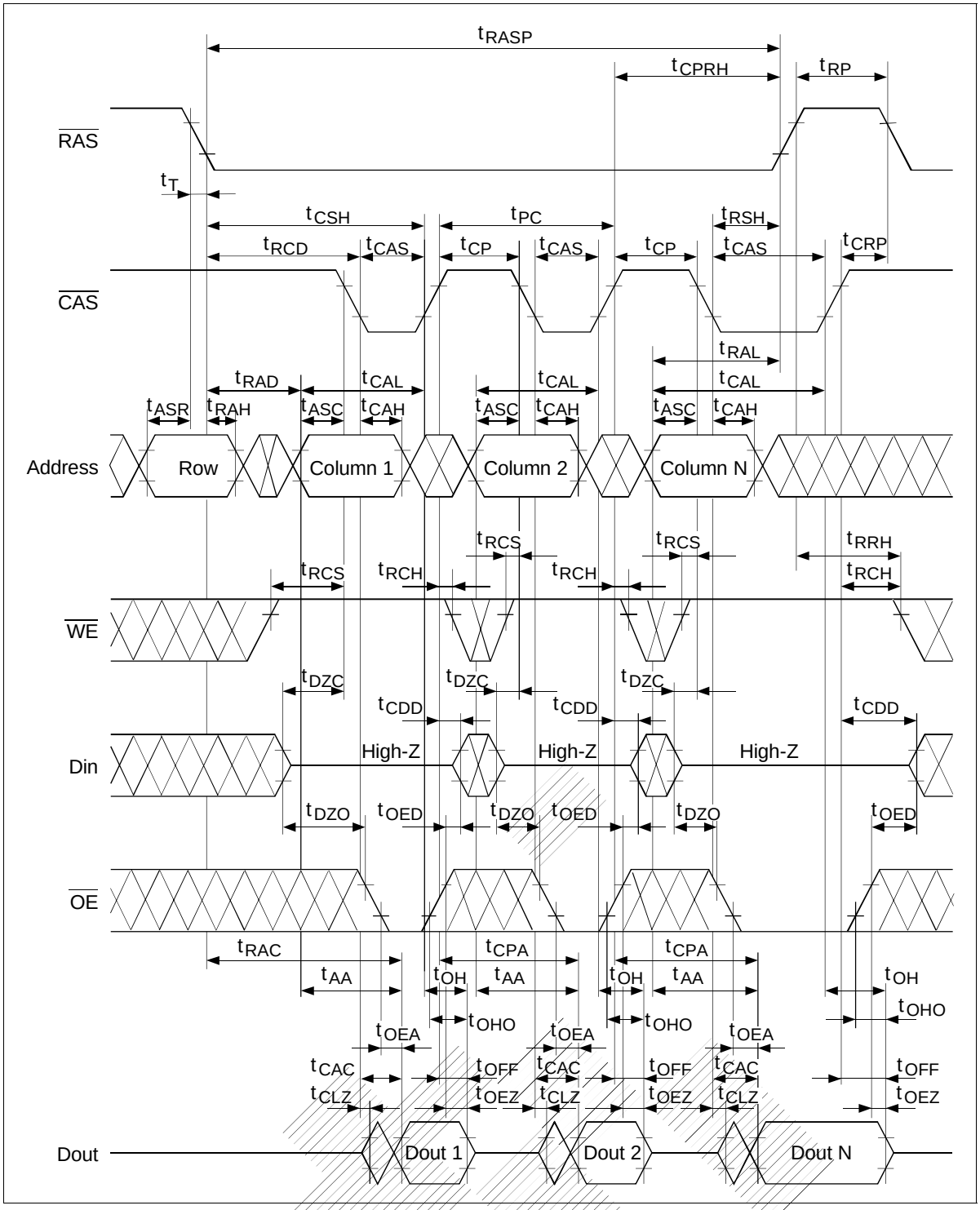
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



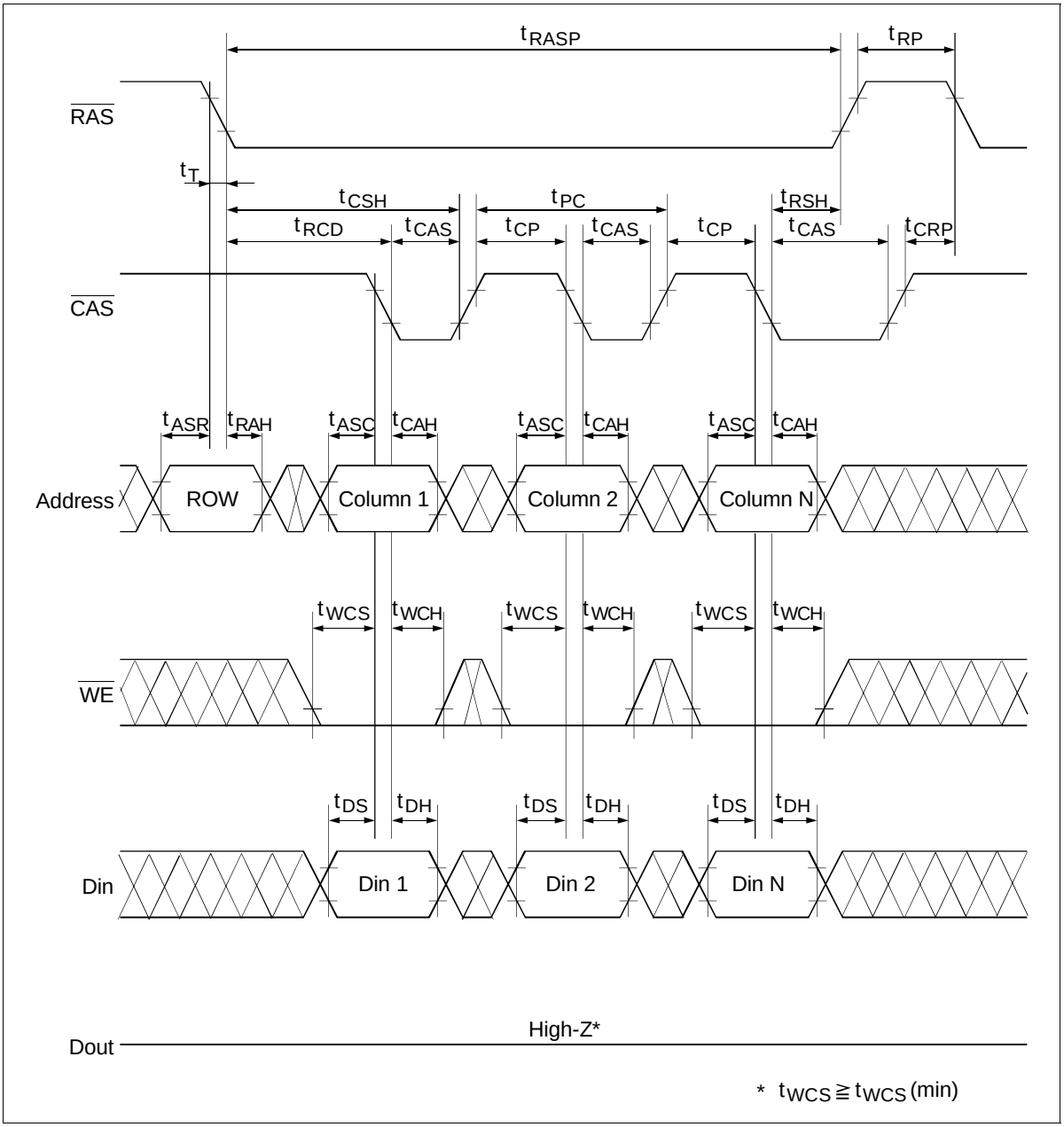
Hidden Refresh Cycle



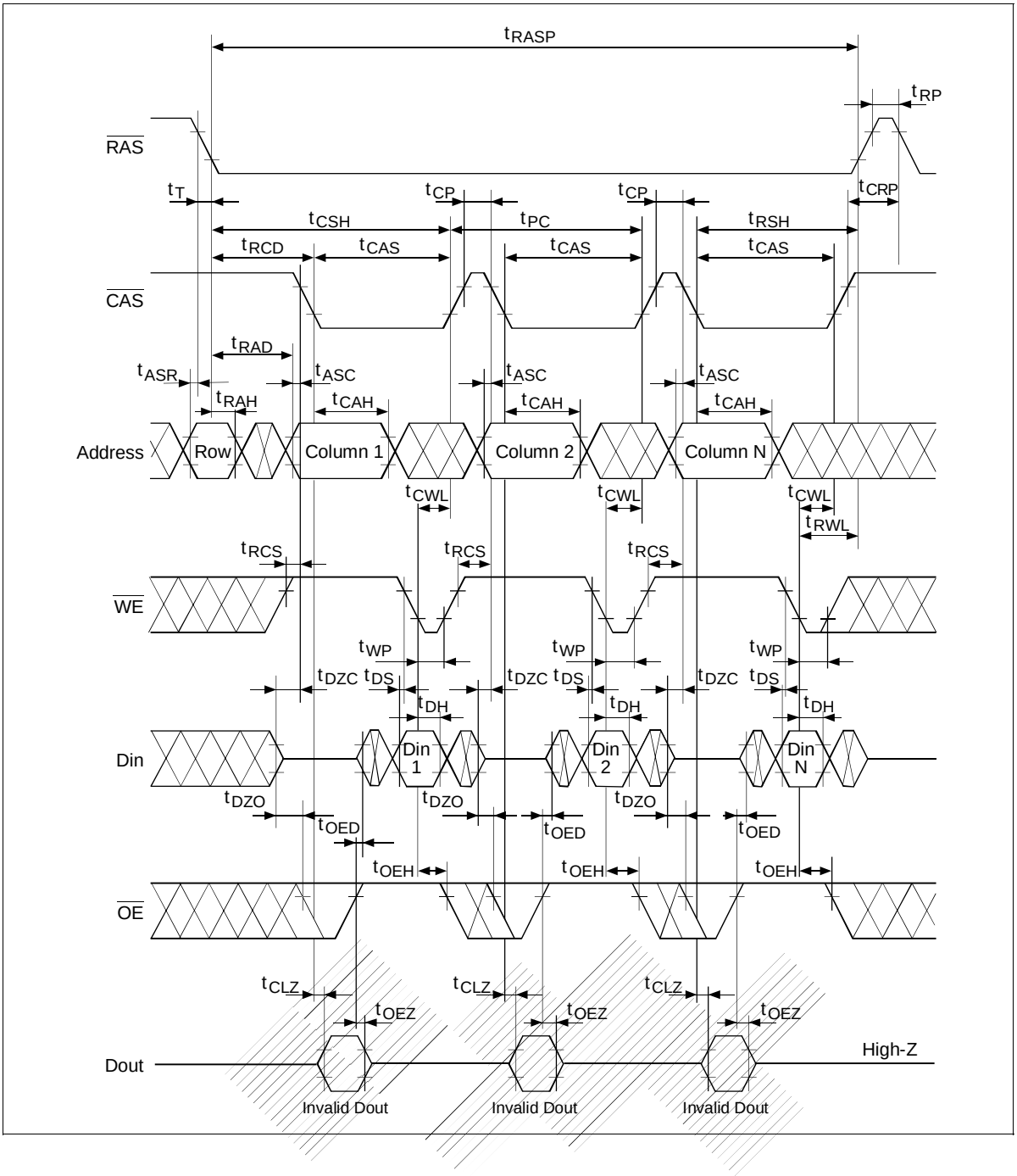
Fast Page Mode Read Cycle



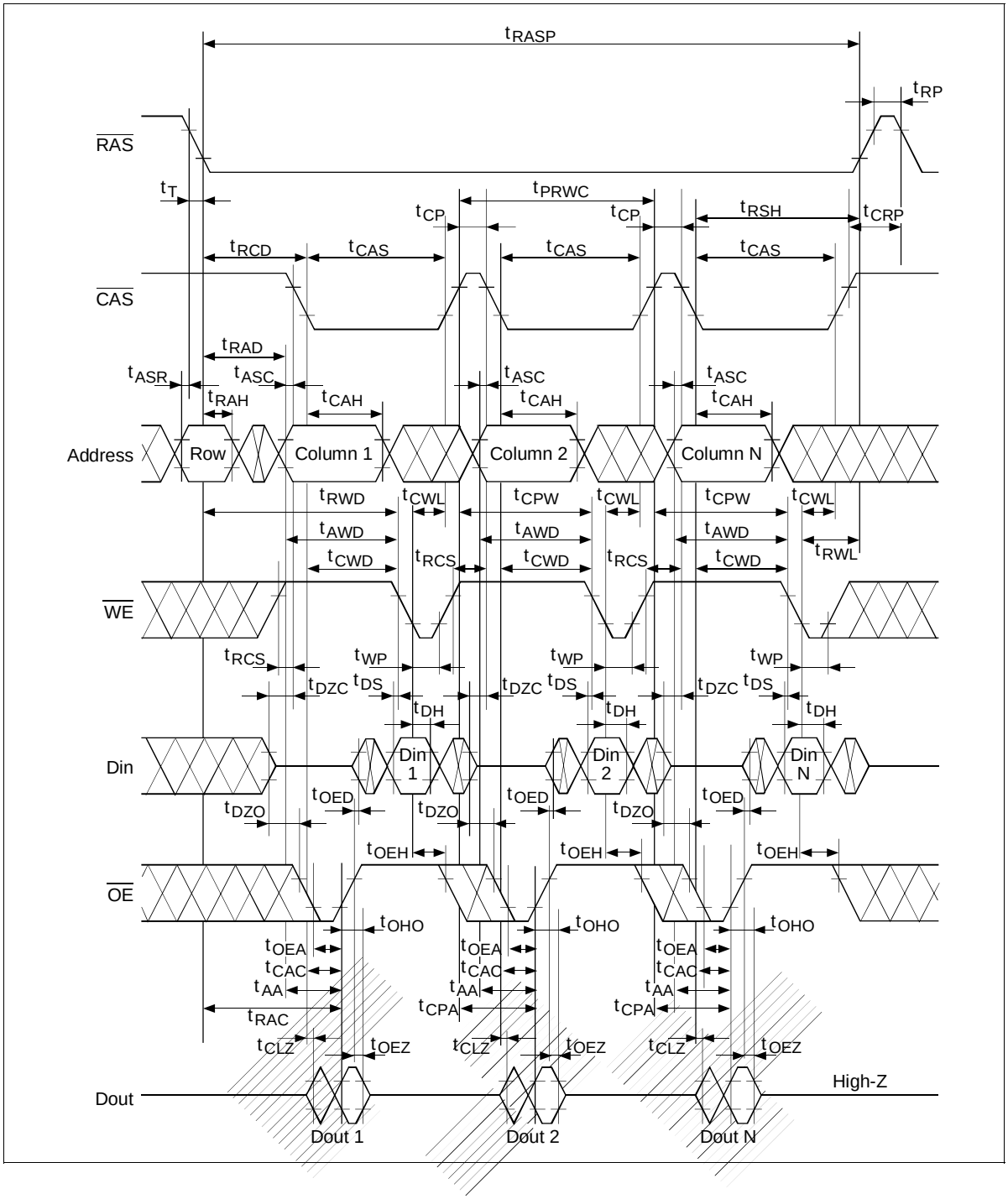
Fast Page Mode Early Write Cycle



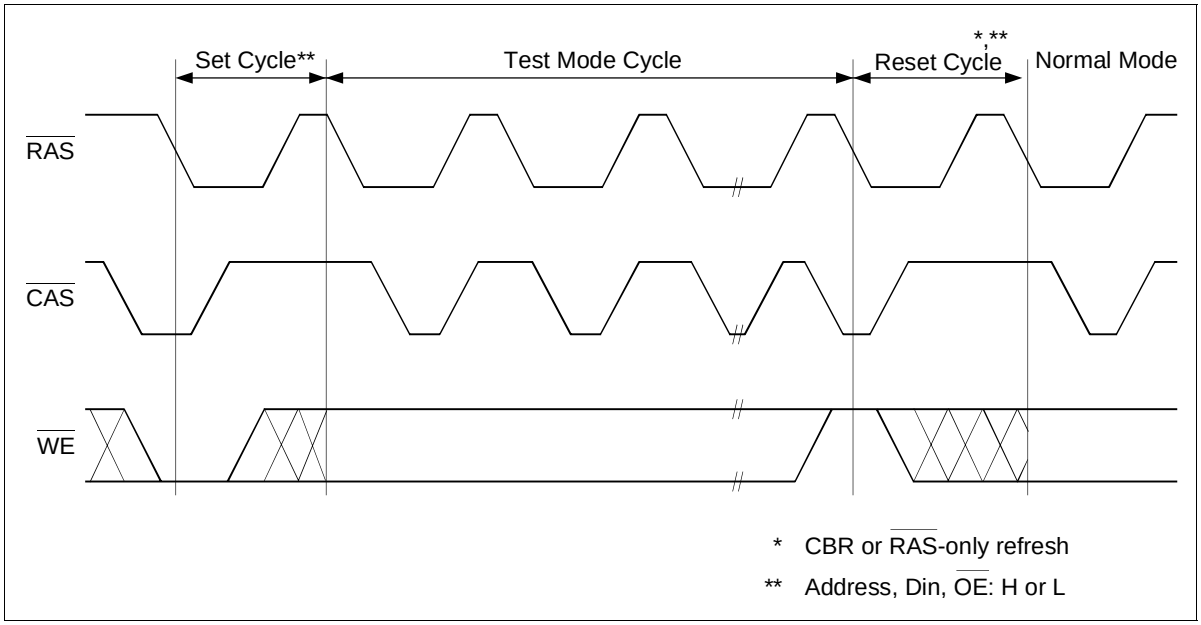
Fast Page Mode Delayed Write Cycle*[18]



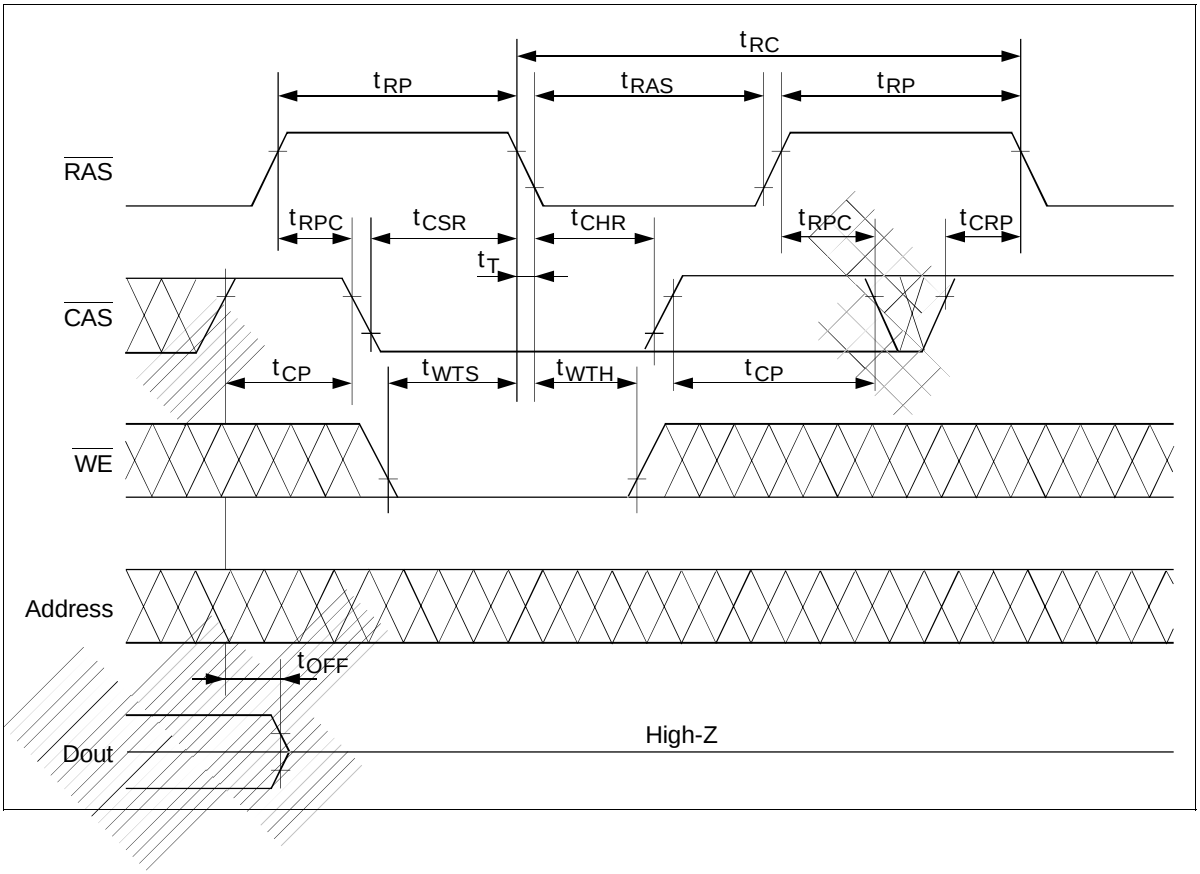
Fast Page Mode Read-Modify-Write Cycle*[18]



Test Mode Cycle*[19]

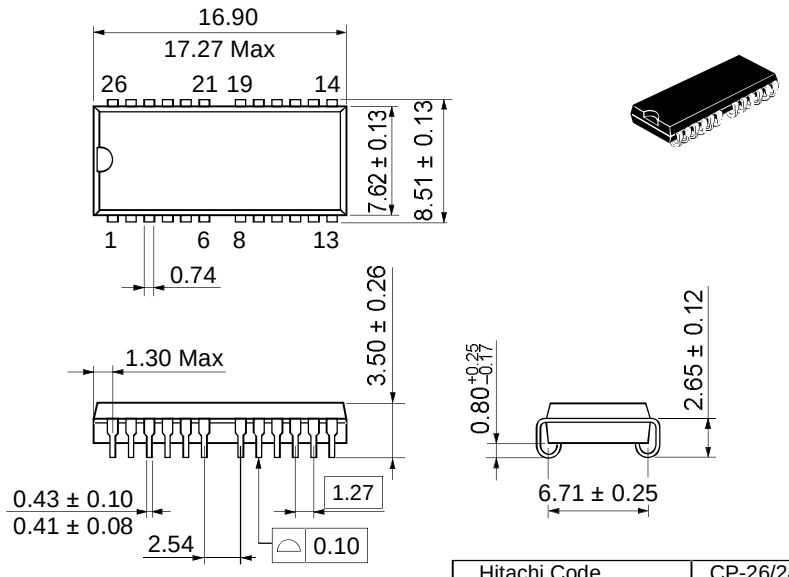


Test Mode Set Cycle



Package Dimensions

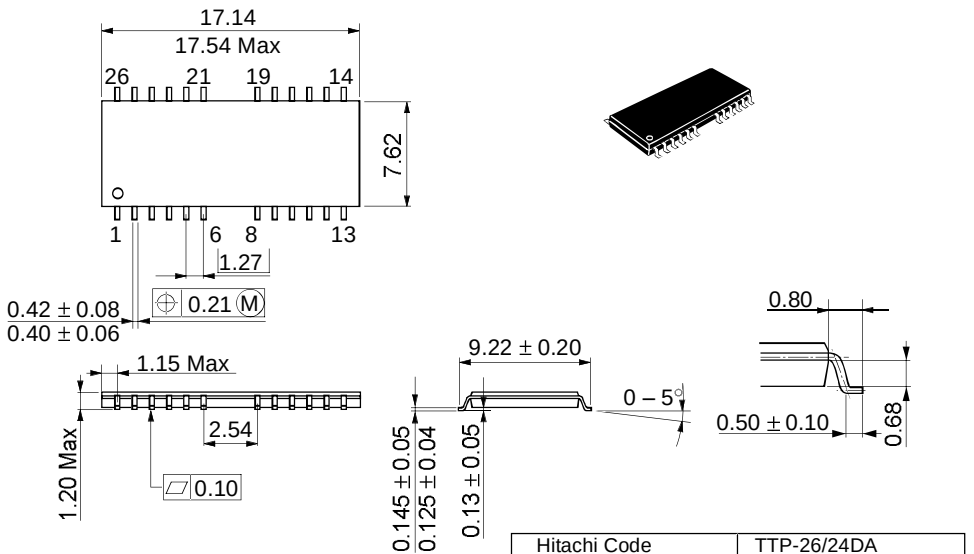
HM5116400S/LS Series
HM5117400S/LS Series (CP-26/24DB) **Unit: mm**



Hitachi Code	CP-26/24DB
JEDEC Code	MO-077-AA
EIAJ Code	SC-632-A
Weight	0.8 g

HM5116400TS/LTS Series

HM5117400TS/LTS Series (TTP-26/24DA) **Unit: mm**



Hitachi Code	TTP-26/24DA
JEDEC Code	MO-132AB
EIAJ Code	—
Weight	0.30 g

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Oct. 14, 1996	Initial issue	Y. Kasama	M. Mishima
2.0	Nov. 14, 1996	Addition of HM5116400-5 Series Addition of HM5117400-5 Series Power dissipation (active) 605/550 mW(max) to 550/495/440 mW (max) (HM5117400 Series) DC Characteristics (HM5117400 Series) I_{CC1} max: 110/100 mA to 100/90/80 mA I_{CC3} max: 110/100 mA to 100/90/80 mA I_{CC6} max: 110/100 mA to 100/90/80 mA	Y. Kasama	Y. Matsuno
3.0	Feb. 27, 1997	AC Characteristics t_{RRH} min: 5/5/5 ns to 0/0/0 ns		