REJ03B0046-0110Z
Rev.1.10
Jun. 28, 2004

1. Overview

The M32C/85 group (M32C/85, M32C/85T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/85 group (M32C/85, M32C/85T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It incorporates a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.2 Performance Outline

Tables 1.1 and 1.2 list performance outlines of the M32C/85 group (M32C/85, M32C/85T).

Table 1.1 M32C/85 Group (M32C/85, M32C/85T) Performance (144-Pin Package)

Characteristic		Performance	
		M32C/85	M32C/85T
CPU	Basic Instructions	108 instructions	
	Shortest Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V) 41.7 ns (f(BCLK)=24 MHz, V_{CC1}=3.0 V to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V)
	Operation Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	123 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I^2C bus(2)	
	CAN Module	2 channels Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 1 circuit, 34 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	XY Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	39 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generating Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
	Supply Voltage Detect Circuit	Available (optional)	Not available
Electrical Characteristics	Supply Voltage	V_{CC1}=4.2 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=32 MHz) V_{CC1}=3.0 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=24 MHz)	V_{CC1}=V_{CC2}=4.2 V to 5.5 V, (f(BCLK)=32 MHz)(3)
	Power Consumption	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 22 mA (V_{CC1}=V_{CC2}=3.3 V, f(BCLK)=24 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(X_{CIN})=32 kHz, in wait mode)	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(X_{CIN})=32 kHz, in wait mode)
Flash Memory	Program/Erase Supply Voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V	5.0 V ± 0.5 V
	Program and Erase Endurance	100 cycles (all space)	
Operating Ambient Temperature		–20 to 85°C –40 to 85°C (optional)	–40 to 85°C (T version)
Package		144-pin plastic molded LQFP	

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. The supply voltage of M32C/85T (High-reliability version) must be V_{CC1}=V_{CC2}.

All options are on a request basis.

Table 1.2 M32C/85 Group (M32C/85, M32C/85T) Performance (100-Pin Package)

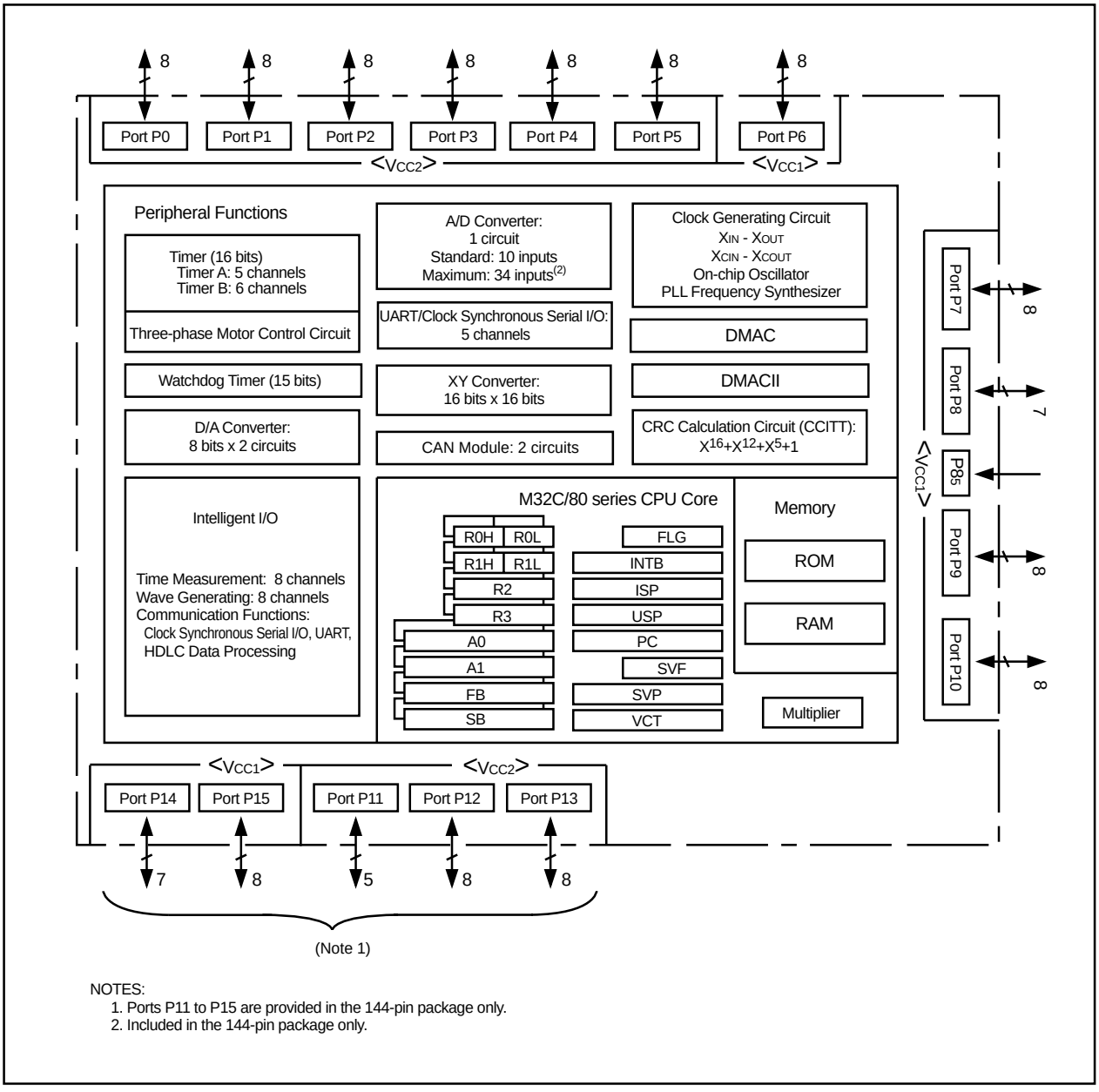
Characteristic		Performance	
		M32C/85	M32C/85T
CPU	Basic Instructions	108 instructions	
	Shortest Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V) 41.7 ns (f(BCLK)=24 MHz, V_{CC1}=3.0 V to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V)
	Operation Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	87 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I^2C bus(2)	
	CAN Module	2 channels Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	XY Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	39 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generating Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
	Supply Voltage Detect Circuit	Available (optional)	Not available
Electrical Characteristics	Supply Voltage	V_{CC1}=4.2 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=32 MHz) V_{CC1}=3.0 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=24 MHz)	V_{CC1}=V_{CC2}=4.2 V to 5.5 V, (f(BCLK)=32 MHz)(3)
	Power Consumption	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 22 mA (V_{CC1}=V_{CC2}=3.3 V, f(BCLK)=24 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(X_{CIN})=32 kHz, wait mode)	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(X_{CIN})=32 kHz, wait mode)
Flash Memory	Program/Erase Supply Voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V	5.0 V ± 0.5 V
	Program and Erase Endurance	100 cycles (all space)	
Operating Ambient Temperature		–20 to 85°C –40 to 85°C (optional)	–40 to 85°C (T version)
Package		100-pin plastic molded LQFP/QFP	

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. The supply voltage of M32C/85T (High-reliability version) must be V_{CC1}=V_{CC2}.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/85 group (M32C/85, M32C/85T) microcomputer.



NOTES:
1. Ports P11 to P15 are provided in the 144-pin package only.
2. Included in the 144-pin package only.

Figure 1.1 M32C/85 Group (M32C/85, M32C/85T) Block Diagram

1.4 Product Information

Table 1.3 lists product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/85 Group (1) (M32C/85) **As of June, 2004**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks
M30852FJGP (D)	512K+4K	16K	144P6Q-A	Flash Memory
M30850FJGP (D)			100P6Q-A	
M30850FJFP (D)			100P6S-A	
M30855FHGP (D)	384K+4K	24K	144P6Q-A	
M30853FHGP (D)			100P6Q-A	
M30853FHFP (D)			100P6S-A	
M30855FWGP (D)	320K+4K	24K	144P6Q-A	
M30853FWGP (D)			100P6Q-A	
M30853FWFP (D)			100P6S-A	
M30855MW-XXXGP (D)	320K	24K	144P6Q-A	Masked ROM
M30853MW-XXXGP (D)			100P6Q-A	
M30853MW-XXXFP (D)			100P6S-A	

(D): Under development

Table 1.3 M32C/85 Group (2) (T Version, M32C/85T) **As of June, 2004**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	
M30852FJTGP (D)	512K+4K	16K	144P6Q-A	Flash Memory	T version (High-reliability 85°C version)
M30850FJTGP (D)			100P6Q-A		
M30855FHTGP (D)	384K+4K	24K	144P6Q-A		
M30853FHTGP (D)			100P6Q-A		
M30855FWTGP (D)	320K+4K	24K	144P6Q-A		
M30853FWTGP (D)			100P6Q-A		

(D): Under development

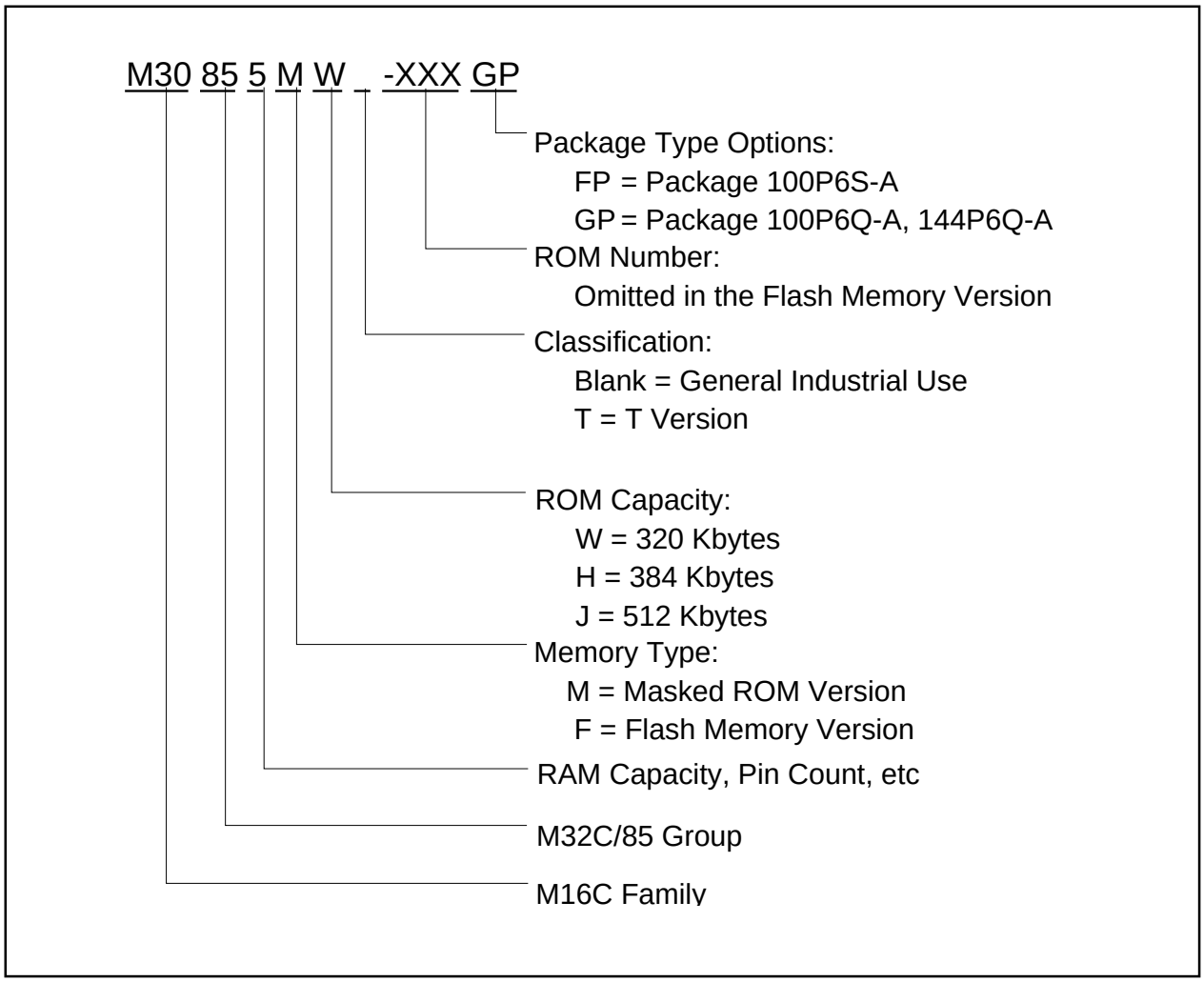


Figure 1.2 Product Numbering System

1.5 Pin Assignments and Descriptions

Figures 1.3 to 1.5 show pin assignments (top view).

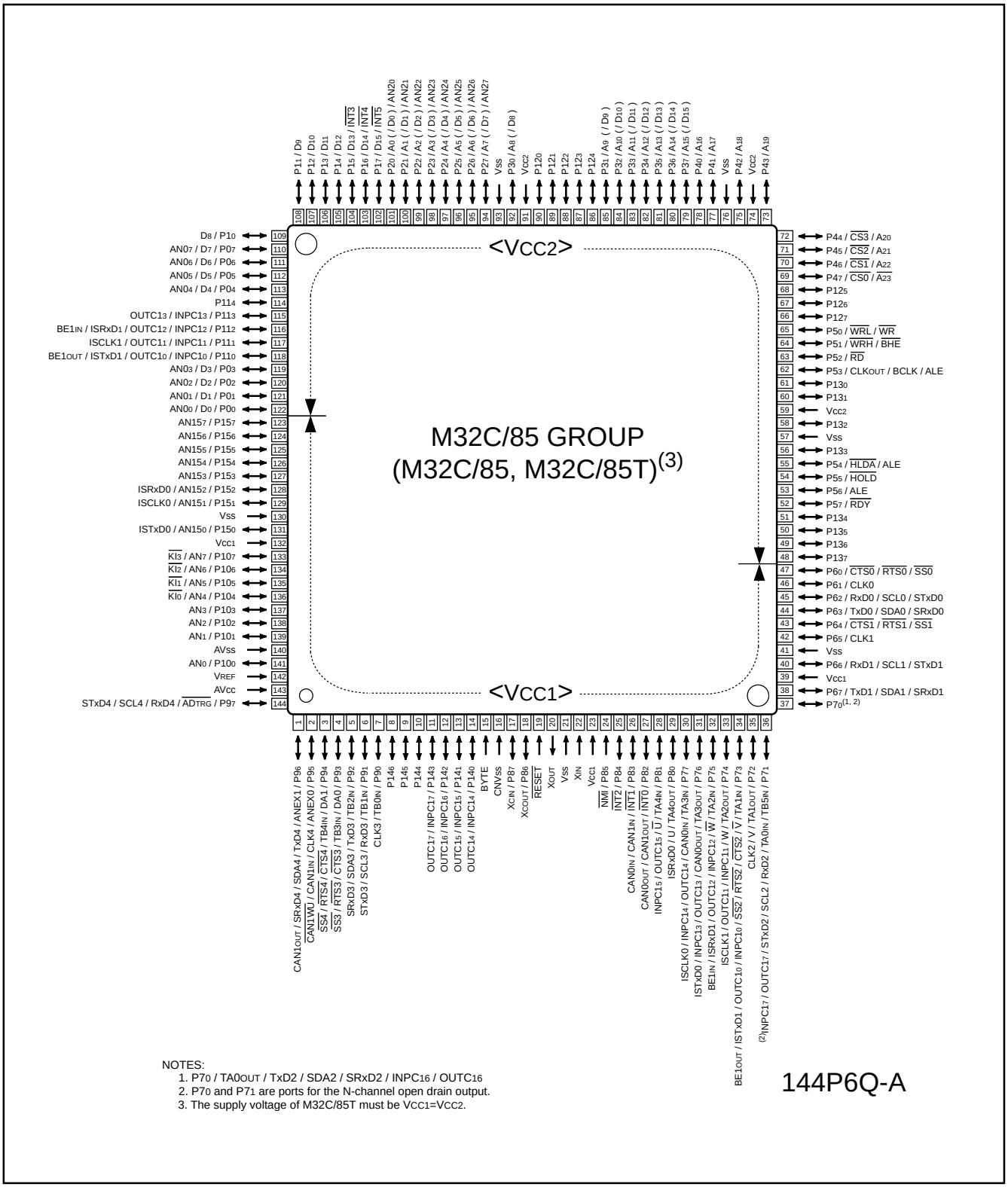


Figure 1.3 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
1		P9$_6$			TxD4/SDA4/SRxD4/CAN1$_{OUT}$		ANEX1	
2		P9$_5$			CLK4/CAN1$_{IN}$/$\overline{CAN1WU}$		ANEX0	
3		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1	
4		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0	
5		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3			
6		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3			
7		P9$_0$		TB0$_{IN}$	CLK3			
8		P14$_6$						
9		P14$_5$						
10		P14$_4$						
11		P14$_3$				INPC17/OUTC17		
12		P14$_2$				INPC16/OUTC16		
13		P14$_1$				INPC15/OUTC15		
14		P14$_0$				INPC14/OUTC14		
15	BYTE							
16	CNV$_{SS}$							
17	X$_{CIN}$	P8$_7$						
18	X$_{COUT}$	P8$_6$						
19	$\overline{RESET}$							
20	X$_{OUT}$							
21	V$_{SS}$							
22	X$_{IN}$							
23	V$_{CC1}$							
24		P8$_5$	$\overline{NMI}$					
25		P8$_4$	$\overline{INT2}$					
26		P8$_3$	$\overline{INT1}$		CAN0$_{IN}$/CAN1$_{IN}$			
27		P8$_2$	$\overline{INT0}$		CAN0$_{OUT}$/CAN1$_{OUT}$			
28		P8$_1$		TA4$_{IN}$/$\overline{U}$		INPC15/OUTC15		
29		P8$_0$		TA4$_{OUT}$/U		ISRxD0		
30		P7$_7$		TA3$_{IN}$	CAN0$_{IN}$	INPC14/OUTC14/ISCLK0		
31		P7$_6$		TA3$_{OUT}$	CAN0$_{OUT}$	INPC13/OUTC13/ISTxD0		
32		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC12/OUTC12/ISRxD1/BE1$_{IN}$		
33		P7$_4$		TA2$_{OUT}$/W		INPC11/OUTC11/ISCLK1		
34		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	INPC10/OUTC10/ISTxD1/BE1$_{OUT}$		
35		P7$_2$		TA1$_{OUT}$/V	CLK2			
36		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	INPC17/OUTC17		
37		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	INPC16/OUTC16		
38		P6$_7$			TxD1/SDA1/SRxD1			
39	V$_{CC1}$							
40		P6$_6$			RxD1/SCL1/STxD1			
41	V$_{SS}$							
42		P6$_5$			CLK1			
43		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$			
44		P6$_3$			TxD0/SDA0/SRxD0			
45		P6$_2$			RxD0/SCL0/STxD0			
46		P6$_1$			CLK0			
47		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
48		P13$_7$						

NOTES:

1. Bus control pins in M32C/85T cannot be used.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
49		P136						
50		P135						
51		P134						
52		P57						$\overline{\text{RDY}}$
53		P56						ALE
54		P55						$\overline{\text{HOLD}}$
55		P54						$\overline{\text{HLDA}}$/ALE
56		P133						
57	VSS							
58		P132						
59	VCC2							
60		P131						
61		P130						
62		P53						CLKOUT/BCLK/ALE
63		P52						$\overline{\text{RD}}$
64		P51						$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
65		P50						$\overline{\text{WRL}}$/$\overline{\text{WR}}$
66		P127						
67		P126						
68		P125						
69		P47						$\overline{\text{CS0}}$/A23
70		P46						$\overline{\text{CS1}}$/A22
71		P45						$\overline{\text{CS2}}$/A21
72		P44						$\overline{\text{CS3}}$/A20
73		P43						A19
74	VCC2							
75		P42						A18
76	VSS							
77		P41						A17
78		P40						A16
79		P37						A15(/D15)
80		P36						A14(/D14)
81		P35						A13(/D13)
82		P34						A12(/D12)
83		P33						A11(/D11)
84		P32						A10(/D10)
85		P31						A9(/D9)
86		P124						
87		P123						
88		P122						
89		P121						
90		P120						
91	VCC2							
92		P30						A8(/D8)
93	VSS							
94		P27					AN27	A7(/D7)
95		P26					AN26	A6(/D6)
96		P25					AN25	A5(/D5)

NOTES:

1. Bus control pins in M32C/85T cannot be used.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
97		$P2_4$					$AN2_4$	A_4(/D_4)
98		$P2_3$					$AN2_3$	A_3(/D_3)
99		$P2_2$					$AN2_2$	A_2(/D_2)
100		$P2_1$					$AN2_1$	A_1(/D_1)
101		$P2_0$					$AN2_0$	A_0(/D_0)
102		$P1_7$	$\overline{INT5}$					D_{15}
103		$P1_6$	$\overline{INT4}$					D_{14}
104		$P1_5$	$\overline{INT3}$					D_{13}
105		$P1_4$						D_{12}
106		$P1_3$						D_{11}
107		$P1_2$						D_{10}
108		$P1_1$						D_9
109		$P1_0$						D_8
110		$P0_7$					$AN0_7$	D_7
111		$P0_6$					$AN0_6$	D_6
112		$P0_5$					$AN0_5$	D_5
113		$P0_4$					$AN0_4$	D_4
114		$P11_4$						
115		$P11_3$				$INPC1_3$/$OUTC1_3$		
116		$P11_2$				$INPC1_2$/$OUTC1_2$/ISRxD1/$BE1_{IN}$		
117		$P11_1$				$INPC1_1$/$OUTC1_1$/ISCLK1		
118		$P11_0$				$INPC1_0$/$OUTC1_0$/ISTxD1/$BE1_{OUT}$		
119		$P0_3$					$AN0_3$	D_3
120		$P0_2$					$AN0_2$	D_2
121		$P0_1$					$AN0_1$	D_1
122		$P0_0$					$AN0_0$	D_0
123		$P15_7$					$AN15_7$	
124		$P15_6$					$AN15_6$	
125		$P15_5$					$AN15_5$	
126		$P15_4$					$AN15_4$	
127		$P15_3$					$AN15_3$	
128		$P15_2$				ISRxD0	$AN15_2$	
129		$P15_1$				ISCLK0	$AN15_1$	
130	V_{SS}							
131		$P15_0$				ISTxD0	$AN15_0$	
132	V_{CC1}							
133		$P10_7$	$\overline{KI_3}$				AN_7	
134		$P10_6$	$\overline{KI_2}$				AN_6	
135		$P10_5$	$\overline{KI_1}$				AN_5	
136		$P10_4$	$\overline{KI_0}$				AN_4	
137		$P10_3$					AN_3	
138		$P10_2$					AN_2	
139		$P10_1$					AN_1	
140	AV_{SS}							
141		$P10_0$					AN_0	
142	V_{REF}							
143	AV_{CC}							
144		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

NOTES:

1. Bus control pins in M32C/85T cannot be used,

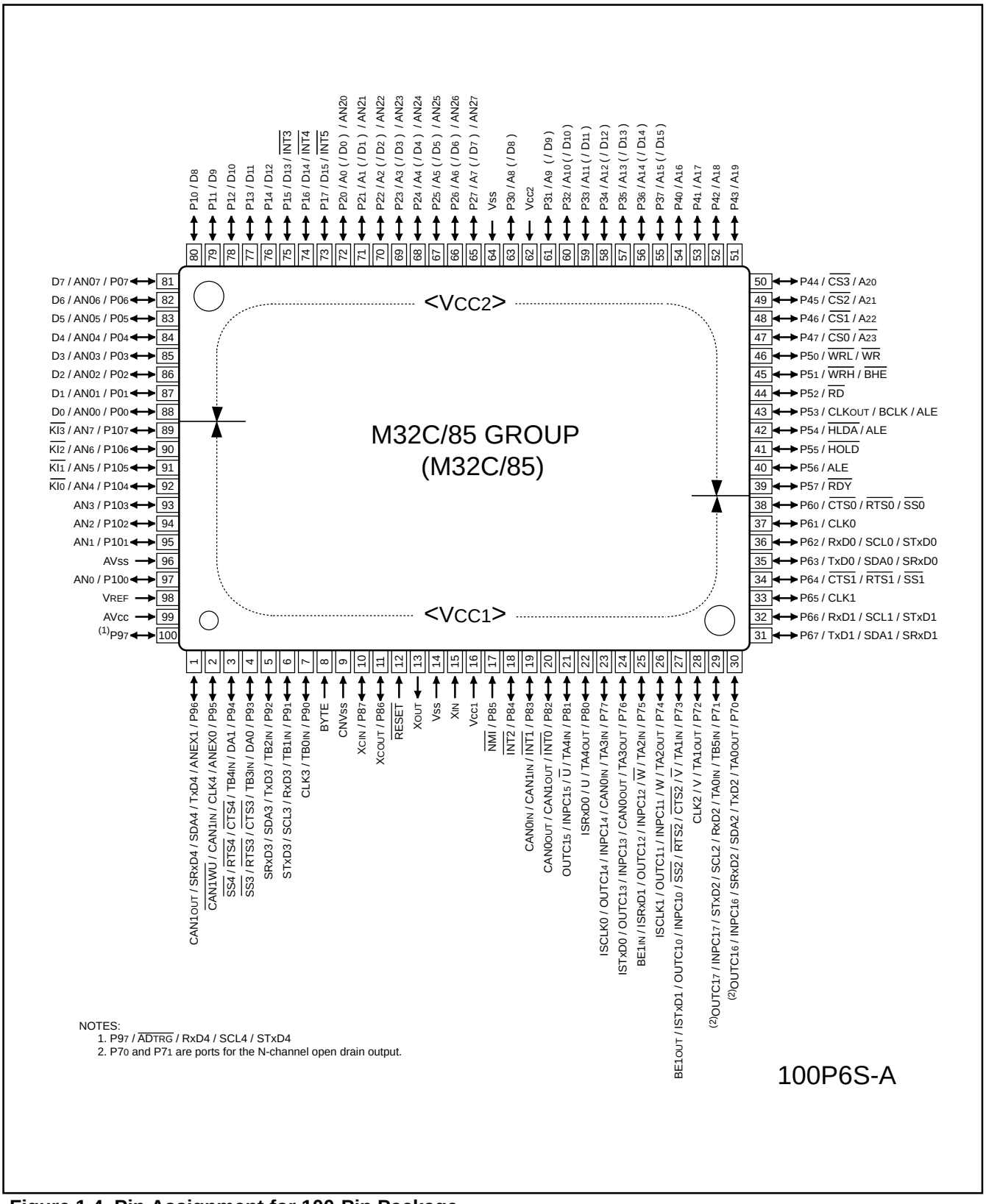


Figure 1.4 Pin Assignment for 100-Pin Package

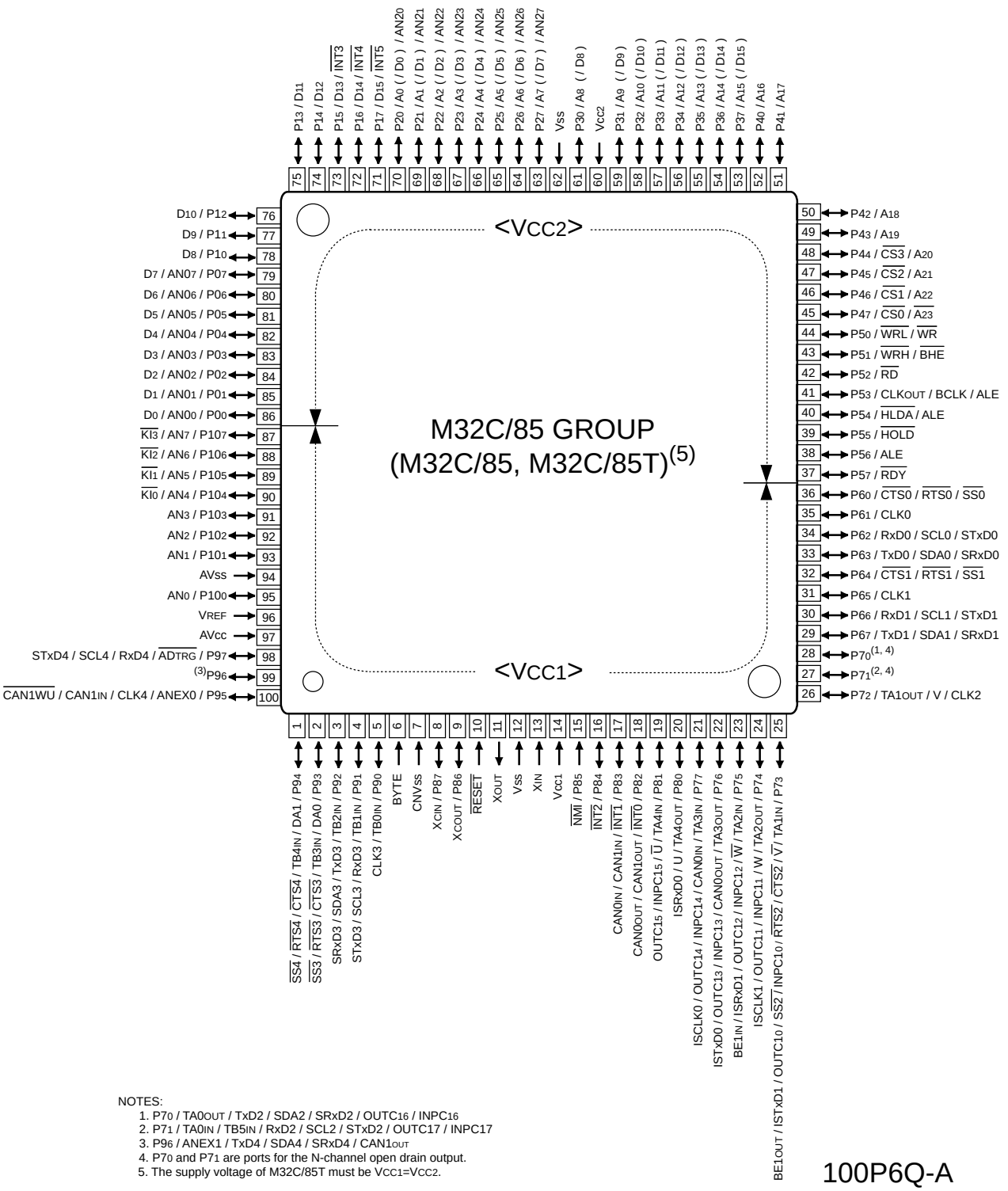


Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
FP	GP								
1	99		P9$_6$			TxD4/SDA4/SRxD4/CAN1$_{OUT}$		ANEX1	
2	100		P9$_5$			CLK4/CAN1IN/$\overline{CAN1WU}$		ANEX0	
3	1		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1	
4	2		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0	
5	3		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3			
6	4		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3			
7	5		P9$_0$		TB0$_{IN}$	CLK3			
8	6	BYTE							
9	7	CNV$_{SS}$							
10	8	X$_{CIN}$	P8$_7$						
11	9	X$_{COUT}$	P8$_6$						
12	10	$\overline{RESET}$							
13	11	X$_{OUT}$							
14	12	V$_{SS}$							
15	13	X$_{IN}$							
16	14	V$_{CC1}$							
17	15		P8$_5$	$\overline{NMI}$					
18	16		P8$_4$	$\overline{INT2}$					
19	17		P8$_3$	$\overline{INT1}$		CAN0$_{IN}$/CAN1$_{IN}$			
20	18		P8$_2$	$\overline{INT0}$		CAN0$_{OUT}$/CAN1$_{OUT}$			
21	19		P8$_1$		TA4$_{IN}$/$\overline{U}$		INPC1$_5$/OUTC1$_5$		
22	20		P8$_0$		TA4$_{OUT}$/U		ISRxD0		
23	21		P7$_7$		TA3$_{IN}$	CAN0$_{IN}$	INPC1$_4$/OUTC1$_4$/ISCLK0		
24	22		P7$_6$		TA3$_{OUT}$	CAN0$_{OUT}$	INPC1$_3$/OUTC1$_3$/ISTxD0		
25	23		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$		
26	24		P7$_4$		TA2$_{OUT}$/W		INPC1$_1$/OUTC1$_1$/ISCLK1		
27	25		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	INPC1$_0$/OUTC1$_0$/ISTxD1/BE1$_{OUT}$		
28	26		P7$_2$		TA1$_{OUT}$/V	CLK2			
29	27		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	INPC1$_7$/OUTC1$_7$		
30	28		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	INPC1$_6$/OUTC1$_6$		
31	29		P6$_7$			TxD1/SDA1/SRxD1			
32	30		P6$_6$			RxD1/SCL1/STxD1			
33	31		P6$_5$			CLK1			
34	32		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$			
35	33		P6$_3$			TxD0/SDA0/SRxD0			
36	34		P6$_2$			RxD0/SCL0/STxD0			
37	35		P6$_1$			CLK0			
38	36		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
39	37		P5$_7$						$\overline{RDY}$
40	38		P5$_6$						ALE
41	39		P5$_5$						$\overline{HOLD}$
42	40		P5$_4$						$\overline{HLDA}$/ALE
43	41		P5$_3$						CLK$_{OUT}$/BCLK/ALE
44	42		P5$_2$						$\overline{RD}$
45	43		P5$_1$						$\overline{WRH}$/$\overline{BHE}$
46	44		P5$_0$						$\overline{WRL}$/$\overline{WR}$
47	45		P4$_7$						$\overline{CS0}$/A$_{23}$
48	46		P4$_6$						$\overline{CS1}$/A$_{22}$
49	47		P4$_5$						$\overline{CS2}$/A$_{21}$
50	48		P4$_4$						$\overline{CS3}$/A$_{20}$

NOTES:

1. Bus control pins in M32C/85T cannot be used.

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
FP	GP								
51	49		$P4_3$						A_{19}
52	50		$P4_2$						A_{18}
53	51		$P4_1$						A_{17}
54	52		$P4_0$						A_{16}
55	53		$P3_7$						A_{15}(/D_{15})
56	54		$P3_6$						A_{14}(/D_{14})
57	55		$P3_5$						A_{13}(/D_{13})
58	56		$P3_4$						A_{12}(/D_{12})
59	57		$P3_3$						A_{11}(/D_{11})
60	58		$P3_2$						A_{10}(/D_{10})
61	59		$P3_1$						A_9(/D_9)
62	60	V_{CC2}							
63	61		$P3_0$						A_8(/D_8)
64	62	V_{SS}							
65	63		$P2_7$					$AN2_7$	A_7(/D_7)
66	64		$P2_6$					$AN2_6$	A_6(/D_6)
67	65		$P2_5$					$AN2_5$	A_5(/D_5)
68	66		$P2_4$					$AN2_4$	A_4(/D_4)
69	67		$P2_3$					$AN2_3$	A_3(/D_3)
70	68		$P2_2$					$AN2_2$	A_2(/D_2)
71	69		$P2_1$					$AN2_1$	A_1(/D_1)
72	70		$P2_0$					$AN2_0$	A_0(/D_0)
73	71		$P1_7$	$\overline{INT5}$					D_{15}
74	72		$P1_6$	$\overline{INT4}$					D_{14}
75	73		$P1_5$	$\overline{INT3}$					D_{13}
76	74		$P1_4$						D_{12}
77	75		$P1_3$						D_{11}
78	76		$P1_2$						D_{10}
79	77		$P1_1$						D_9
80	78		$P1_0$						D_8
81	79		$P0_7$					$AN0_7$	D_7
82	80		$P0_6$					$AN0_6$	D_6
83	81		$P0_5$					$AN0_5$	D_5
84	82		$P0_4$					$AN0_4$	D_4
85	83		$P0_3$					$AN0_3$	D_3
86	84		$P0_2$					$AN0_2$	D_2
87	85		$P0_1$					$AN0_1$	D_1
88	86		$P0_0$					$AN0_0$	D_0
89	87		$P10_7$	$\overline{KI_3}$				AN_7	
90	88		$P10_6$	$\overline{KI_2}$				AN_6	
91	89		$P10_5$	$\overline{KI_1}$				AN_5	
92	90		$P10_4$	$\overline{KI_0}$				AN_4	
93	91		$P10_3$					AN_3	
94	92		$P10_2$					AN_2	
95	93		$P10_1$					AN_1	
96	94	AV_{SS}							
97	95		$P10_0$					AN_0	
98	96	V_{REF}							
99	97	AV_{CC}							
100	98		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

NOTES:

1. Bus control pins in M32C/85T cannot be used.

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
Power Supply	V_{CC1}, V_{CC2} V_{SS}	I I	–	Apply 3.0 to 5.5V to both V_{CC1} and V_{CC2} pins. Apply 0V to the V_{SS} pin. $V_{CC1} \geq V_{CC2}$(1, 2)
Analog Power Supply	AVCC AVSS	I	V_{CC1}	Supplies power to the A/D converter and D/A converter. Connect the AVCC pin to V_{CC1} and the AVSS pin to V_{SS}.
Reset Input	$\overline{RESET}$	I	V_{CC1}	The microcomputer is in a reset state when "L" is applied to the $\overline{RESET}$ pin
CNVSS	CNVSS	I	V_{CC1}	Switches processor mode. Connect the CNVSS pin to V_{SS} to start up in single-chip mode or to V_{CC1} to start up in microprocessor mode
Input to Switch External Data Bus Width(3)	BYTE	I	V_{CC1}	Switches data bus width in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when it is held "H". Set to either. Connect the BYTE pin to V_{SS} to use the microcomputer in single-chip mode
Bus Control Pins(3)	D_0 to D_7	I/O	V_{CC2}	Inputs and outputs data (D_0 to D_7) while accessing an external memory space with the separate bus
	D_8 to D_{15}	I/O	V_{CC2}	Inputs and outputs data (D_8 to D_{15}) while accessing an external memory space with 16-bit separate bus
	A_0 to A_{22}	O	V_{CC2}	Outputs address bits A_0 to A_{22}
	$\overline{A_{23}}$	O	V_{CC2}	Outputs inversed address bit A_{23}
	A_0/D_0 to A_7/D_7	I/O	V_{CC2}	Inputs and outputs data (D_0 to D_7) and outputs 8 low-order address bits (A_0 to A_7) by time-sharing while accessing an external memory space with the multiplexed bus
	A_8/D_8 to A_{15}/D_{15}	I/O	V_{CC2}	Inputs and outputs data (D_8 to D_{15}) and outputs 8 middle-order address bits (A_8 to A_{15}) by time-sharing while accessing an external memory space with 16-bit multiplexed bus
	$\overline{CS0}$ to $\overline{CS3}$	O	V_{CC2}	Outputs $\overline{CS0}$ to $\overline{CS3}$ that are chip-select signals specifying an external space
	$\overline{WRL}$ / $\overline{WR}$ $\overline{WRH}$ / $\overline{BHE}$ $\overline{RD}$	O	V_{CC2}	Outputs $\overline{WRL}$, $\overline{WRH}$, ($\overline{WR}$, $\overline{BHE}$) and $\overline{RD}$ signals. $\overline{WRL}$ and $\overline{WRH}$ can be switched with $\overline{WR}$ and $\overline{BHE}$ by program. ■ $\overline{WRL}$, $\overline{WRH}$ and $\overline{RD}$ selected: If external data bus is 16 bits wide, data is written to an even address in external memory space when $\overline{WRL}$ is held "L". Data is written to an odd address when $\overline{WRH}$ is held "L". Data is read when $\overline{RD}$ is held "L". ■ $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ selected: Data is written to external memory space when $\overline{WR}$ is held "L". Data in an external memory space is read when $\overline{RD}$ is held "L". An odd address is accessed when $\overline{BHE}$ is held "L". Select $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ for external 8-bit data bus.
	ALE	O	V_{CC2}	ALE is a signal latching the address.
	$\overline{HOLD}$	I	V_{CC2}	The microcomputer is placed in a hold state while the $\overline{HOLD}$ pin is held "L".
	$\overline{HLDA}$	O	V_{CC2}	Outputs an "L" signal while the microcomputer is placed in a hold state.
	$\overline{RDY}$	I	V_{CC2}	Bus is placed in a wait state while the $\overline{RDY}$ pin is held "L".

I : Input O : Output I/O : Input and output

NOTES:
1. V_{CC1} is hereinafter referred to as V_{CC} unless otherwise noted.
2. Apply 4.2 to 5.5V to the V_{CC1} and V_{CC2} pins when using M32C/85T. V_{CC1}=V_{CC2}.
3. Bus cotrol pins in M32C/85T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
Main Clock Input	XIN	I	VCC1	I/O pins for the main clock oscillation circuit.Connect a crystal oscillator between XIN and XOUT. To apply externally-generated clock, apply it to XIN and leave XOUT open.
Main Clock Output	XOUT	O	VCC1	
Sub Clock Input	XCIN	I	VCC1	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To apply externally-gener-ated clock, apply it to XCIN and leave XCOUT open.
Sub Clock Output	XCOUT	O	VCC1	
BCLK Output(1)	BCLK	O	VCC2	Outputs BCLK signal
Clock Output	CLKOUT	O	VCC2	Outputs the clock having the same frequency as fC, f8 or f32
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	Input pins for the $\overline{\text{INT}}$ interrupt
	$\overline{\text{INT3}}$ to $\overline{\text{INT5}}$	I	VCC2	
$\overline{\text{NMI}}$ Interrupt Input	$\overline{\text{NMI}}$	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	VCC1	I/O pins for timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	Input pins for timer A0 to A4
Timer B	TB0IN to TB5IN	I	VCC1	Input pins for timer B0 to B5
Three-phase Motor Control Timer Output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	VCC1	Output pins for the three-phase motor control timer
Serial I/O	$\overline{\text{CTS0}}$ to $\overline{\text{CTS4}}$	I	VCC1	Iutput pins for data transmission control
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS4}}$	O	VCC1	Output pins for data reception control
	CLK0 to CLK4	I/O	VCC1	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	VCC1	Inputs serial data
	TxD0 to TxD4	O	VCC1	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I^2C Mode	SDA0 to SDA4	I/O	VCC1	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4	I/O	VCC1	Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)
Serial I/O Special Function	STxD0 to STxD4	O	VCC1	Outputs serial data when slave mode is selected (STxD2 is a pin for the N-channel open drain output.)
	SRxD0 to SRxD4	I	VCC1	Inputs serial data when slave mode is selected
	$\overline{\text{SS0}}$ to $\overline{\text{SS4}}$	I	VCC1	Input pins to control serial I/O special function

I : Input O : Output I/O : Input and output

NOTES:

1. Bus control pins in M32C/85T cannot be used.
2. Apply 4.2 to 5.5V to the VCC1 and VCC2 pins when using M32C/85T. VCC1 = VCC2.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
Reference Voltage Input	V_{REF}	I	-	Supplies reference voltage to the A/D converter and D/A converter
A/D Converter	AN_0 to AN_7 $AN0_0$ to $AN0_7$ $AN2_0$ to $AN2_7$	I	V_{CC1}	Analog input pins for the A/D converter
	$\overline{ADTRG}$	I	V_{CC1}	Input pin for an external A/D trigger
	ANEX0	I/O	V_{CC1}	Extended analog input pin for the A/D converter and output pin in external op-amp connection mode
	ANEX1	I	V_{CC1}	Extended analog input pin for the A/D converter
D/A Converter	DA0, DA1	O	V_{CC1}	Output pin for the D/A converter
Intelligent I/O	$INPC1_0$ to $INPC1_3$	I	V_{CC1}/V_{CC2}(1)	Input pins for the time measurement function
	$INPC1_4$ to $INPC1_7$	I	V_{CC1}	
	$OUTC1_0$ to $OUTC1_3$	O	V_{CC1}/V_{CC2}(1)	Output pins for the waveform generating function
	$OUTC1_4$ to $OUTC1_7$	O	V_{CC1}	($OUTC1_6$ and $OUTC1_7$ assgined to $P7_0$ and $P7_1$ are pins for the N-channel open drain output.)
	ISCLK0	I/O	V_{CC1}	Inputs and outputs the clock for the intellignet I/O communication function
	ISCLK1	I/O	V_{CC1}/V_{CC2}(1)	
	ISRXD0	I	V_{CC1}	Inputs data for the intellignet I/O communication function
	ISRXD1	I	V_{CC1}/V_{CC2}(1)	
	ISTXD0	O	V_{CC1}	Outputs data for the intellignet I/O communication function
	ISTXD1	O	V_{CC1}/V_{CC2}(1)	
	$BE1_{IN}$	I	V_{CC1}/V_{CC2}(1)	Inputs data for the intellignet I/O communication function
	$BE1_{OUT}$	O	V_{CC1}/V_{CC2}(1)	Outputs data for the intellignet I/O communication function
CAN	$CAN0_{IN}$	I	V_{CC1}	Input pin for the CAN communication function
	$CAN0_{OUT}$	O	V_{CC1}	Output pin for the CAN communication function
I/O Ports	$P0_0$ to $P0_7$ $P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$ $P4_0$ to $P4_7$ $P5_0$ to $P5_7$	I/O	V_{CC2}	8-bit I/O ports in CMOS. Each port can be programmed to input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	$P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P9_0$ to $P9_7$ $P10_0$ to $P10_7$	I/O	V_{CC1}	8-bit I/O ports having equivalent functions to P0 ($P7_0$ and $P7_1$ are ports for the N-channel open drain output.)
	$P8_0$ to $P8_4$ $P8_6$, $P8_7$	I/O	V_{CC1}	I/O ports having equivalent functions to P0
Input Port	$P8_5$	I	V_{CC1}	Shares a pin with $\overline{NMI}$. $\overline{NMI}$ input state can be got by reading $P8_5$

I : Input O : Output I/O : Input and output

NOTES:

1. V_{CC2} is not available in the 100-pin package. V_{CC1} only available.
2. Apply 4.2 to 5.5V to the V_{CC1} and V_{CC2} pins when using M32C/85T. $V_{CC1} = V_{CC2}$.

Table 1.6 Pin Description (144-Pin Package only) (Continued)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
A/D Converter	$AN15_0$ to $AN15_7$	I	V_{CC1}	Analog input pins for the A/D converter
I/O Ports	$P11_0$ to $P11_4$ $P12_0$ to $P12_7$ $P13_0$ to $P13_7$	I/O	V_{CC2}	8-bit I/O ports having equivalent functions to P0
	$P14_0$ to $P14_6$ $P15_0$ to $P15_7$	I/O	V_{CC1}	8-bit I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

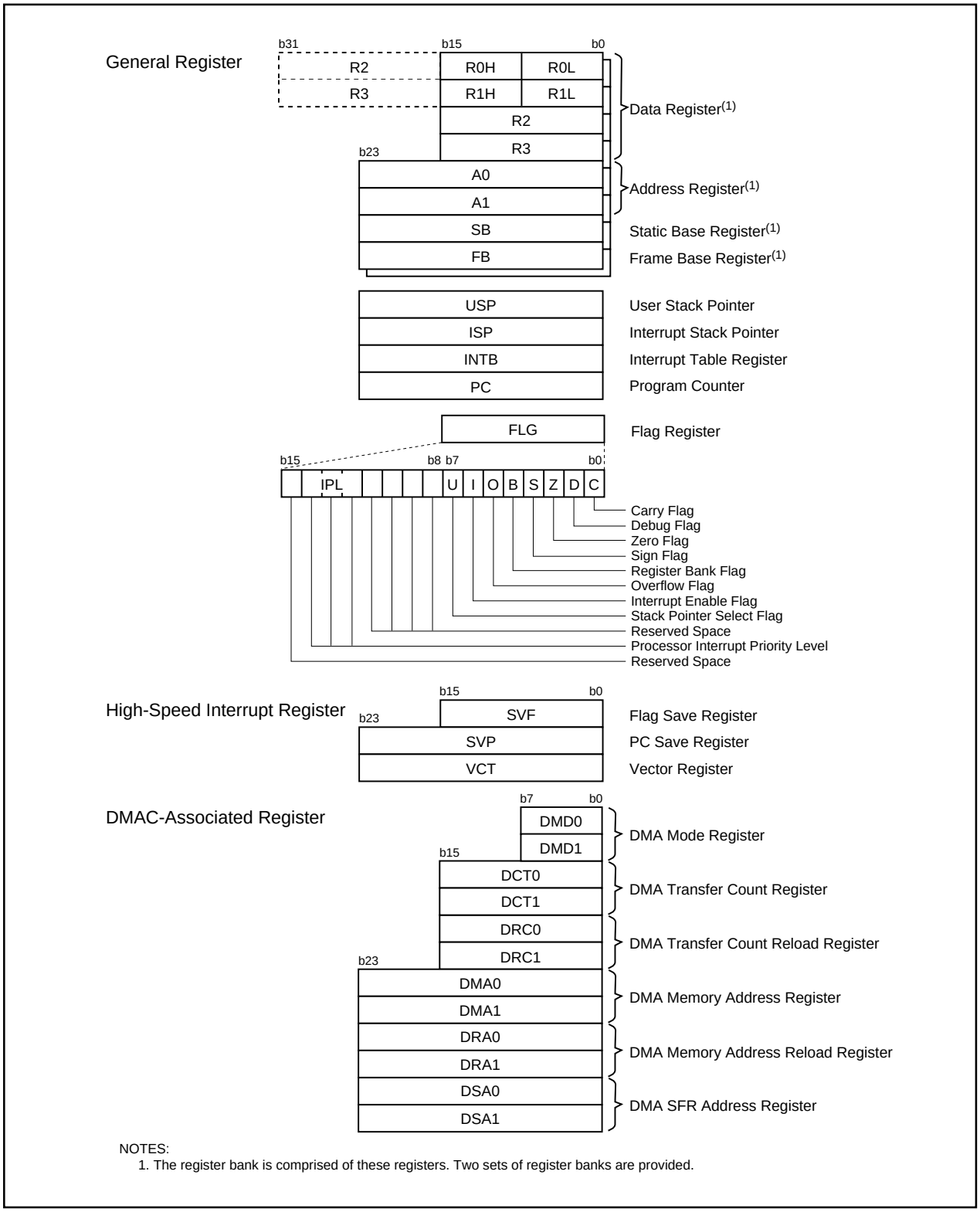
NOTES:

1. Apply 4.2 to 5.5V to the V_{CC1} and V_{CC2} pins when using M32C/85T. $V_{CC1} = V_{CC2}$.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

The register bank is comprised of 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.



NOTES:
1. The register bank is comprised of these registers. Two sets of register banks are provided.

Figure 2.1 CPU Register

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an relocatable interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to "2.1.8 Flag Register (FLG)" for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic calculation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic calculation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
Interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".
The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When reading, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows:

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows:

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/85 group (M32C/85, M32C/85T).

The M32C/85 group (M32C/85, M32C/85T) provides 16-Mbyte address space from addresses 000000$_{16}$ to FFFFFF$_{16}$.

The internal ROM is allocated lower addresses beginning with address FFFFFF$_{16}$. For example, a 64-Kbyte internal ROM is allocated addresses FF0000$_{16}$ to FFFFFF$_{16}$.

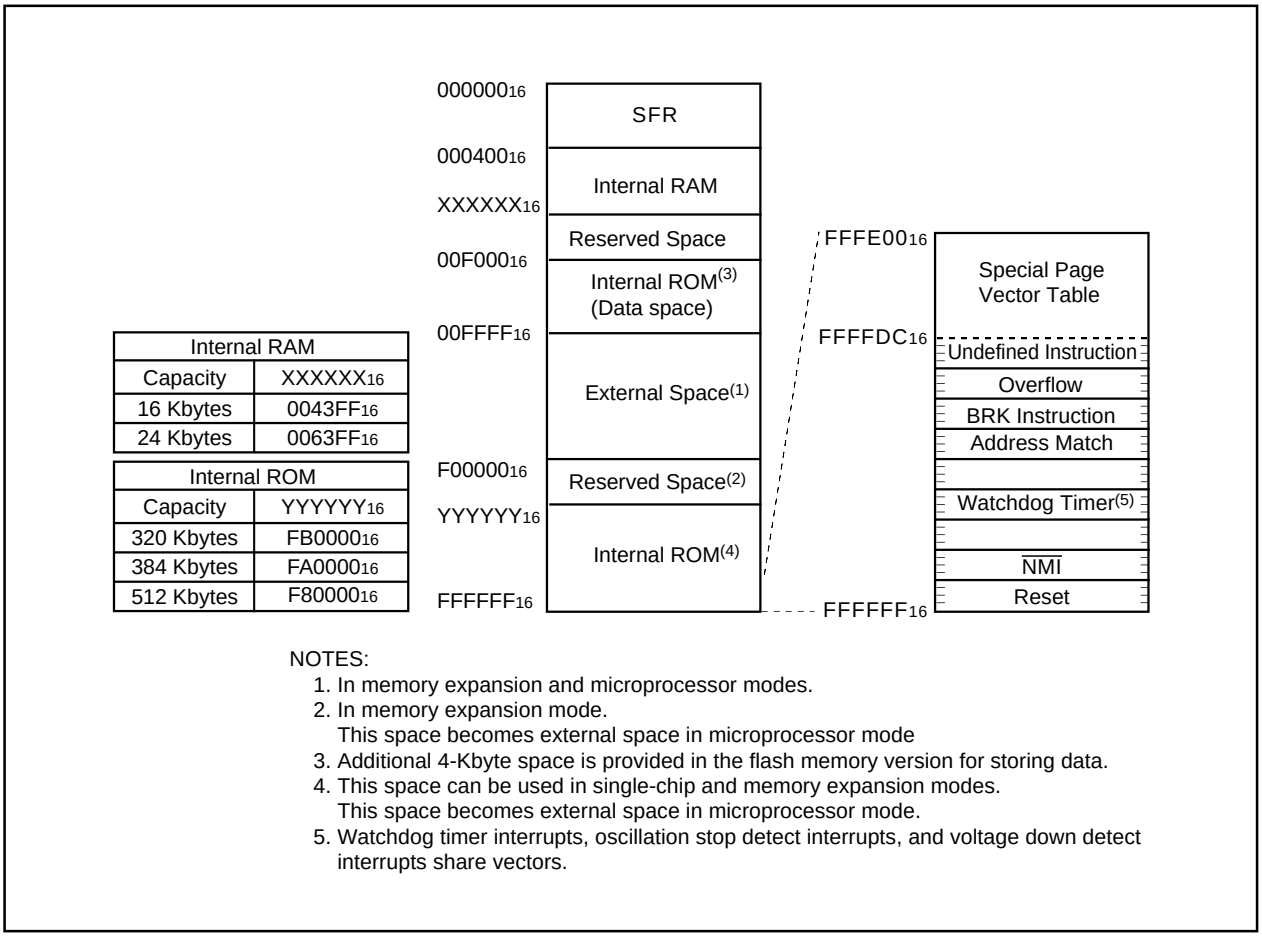
The fixed interrupt vectors are allocated addresses FFFFDC$_{16}$ to FFFFFF$_{16}$. It stores the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 000400$_{16}$. For example, a 10-Kbyte internal RAM is allocated addresses 000400$_{16}$ to 002BFF$_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D conversion, serial I/O, timers, is allocated addresses 000000$_{16}$ to 0003FF$_{16}$. All blank spaces within SFR are reserved spaces and cannot be accessed by users.

The special page vectors are allocated addresses FFFE00$_{16}$ to FFFFDB$_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **Software Manual** for details.

In memory expansion mode and microprocessor mode, some spaces are reserved and cannot be accessed by users.



Internal RAM	
Capacity	XXXXXX$_{16}$
16 Kbytes	0043FF$_{16}$
24 Kbytes	0063FF$_{16}$

Internal ROM	
Capacity	YYYYYY$_{16}$
320 Kbytes	FB0000$_{16}$
384 Kbytes	FA0000$_{16}$
512 Kbytes	F80000$_{16}$

NOTES:
1. In memory expansion and microprocessor modes.
2. In memory expansion mode.
   This space becomes external space in microprocessor mode
3. Additional 4-Kbyte space is provided in the flash memory version for storing data.
4. This space can be used in single-chip and memory expansion modes.
   This space becomes external space in microprocessor mode.
5. Watchdog timer interrupts, oscillation stop detect interrupts, and voltage down detect interrupts share vectors.

Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
000016			
000116			
000216			
000316			
000416	Processor Mode Register(1)	PM0	1000 00002(CNVss pin ="L") 0000 00112(CNVss pin ="H")
000516	Processor Mode Register 1	PM1	0016
000616	System Clock Control Register 0	CM0	0000 10002
000716	System Clock Control Register 1	CM1	0010 00002
000816			
000916	Address Match Interrupt Enable Register	AIER	0016
000A16	Protect Register	PRCR	XXXX 00002
000B16	External Data Bus Width Control Register(2)	DS	XXXX 10002(BYTE pin ="L") XXXX 00002(BYTE pin ="H")
000C16	Main Clock Division Register	MCD	XXX0 10002
000D16	Oscillation Stop Detection Register	CM2	0016
000E16	Watchdog Timer Start Register	WDTS	XX16
000F16	Watchdog Timer Control Register	WDC	000X XXXX2
001016 001116 001216	Address Match Interrupt Register 0	RMAD0	00000016
001316	Processor Mode Register 2	PM2	0016
001416 001516 001616	Address Match Interrupt Register 1	RMAD1	00000016
001716	Voltage Detection Register 2(2)	VCR2	0016
001816 001916 001A16	Address Match Interrupt Register 2	RMAD2	00000016
001B16	Voltage Detection Register 1(2)	VCR1	0000 10002
001C16 001D16 001E16	Address Match Interrupt Register 3	RMAD3	00000016
001F16			
002016			
002116			
002216			
002316			
002416			
002516			
002616	PLL Control Register 0	PLC0	0001 X0102
002716	PLL Control Register 1	PLC1	000X 00002
002816 002916 002A16	Address Match Interrupt Register 4	RMAD4	00000016
002B16			
002C16 002D16 002E16	Address Match Interrupt Register 5	RMAD5	00000016

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The PM00 and PM01 bits in the PM0 register maintain values set before reset, even after software reset or watch-dog timer reset has been performed.
2. These registers cannot be used in M32C/85T.

Address	Register	Symbol	Value after RESET
002F16	Voltage Down Detection Interrupt Register(1)	D4INT	0016
003016			
003116			
003216			
003316			
003416			
003516			
003616			
003716			
003816 003916 003A16	Address Match Interrupt Register 6	RMAD6	00000016
003B16			
003C16 003D16 003E16	Address Match Interrupt Register 7	RMAD7	00000016
003F16			
004016			
004116			
004216			
004316			
004416			
004516			
004616			
004716			
004816	External Space Wait Control Register 0(1)	EWCR0	X0X0 00112
004916	External Space Wait Control Register 1(1)	EWCR1	X0X0 00112
004A16	External Space Wait Control Register 2(1)	EWCR2	X0X0 00112
004B16	External Space Wait Control Register 3(1)	EWCR3	X0X0 00112
004C16			
004D16			
004E16			
004F16			
005016			
005116			
005216			
005316			
005416			
005516	Flash Memory Control Register 1	FMR1	0000 01012
005616			
005716	Flash Memory Control Register 0	FMR0	0000 00012(Flash memory version) XXXX XXX02(Masked ROM version)
005816			
005916			
005A16			
005B16			
005C16			
005D16			
005E16			
005F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. These registers cannot be used in M32C/85T.

Address	Register	Symbol	Value after RESET
006016			
006116			
006216			
006316			
006416			
006516			
006616			
006716			
006816	DMA0 Interrupt Control Register	DM0IC	XXXX X0002
006916	Timer B5 Interrupt Control Register	TB5IC	XXXX X0002
006A16	DMA2 Interrupt Control Register	DM2IC	XXXX X0002
006B16	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X0002
006C16	Timer A0 Interrupt Control Register	TA0IC	XXXX X0002
006D16	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X0002
006E16	Timer A2 Interrupt Control Register	TA2IC	XXXX X0002
006F16	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X0002
007016	Timer A4 Interrupt Control Register	TA4IC	XXXX X0002
007116	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X0002
007216	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X0002
007316	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X0002
007416	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X0002
007516	Intelligent I/O Interrupt Control Register 0 CAN Interrupt 3 Control Register	IIO0IC CAN3IC	XXXX X0002
007616	Timer B1 Interrupt Control Register	TB1IC	XXXX X0002
007716	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X0002
007816	Timer B3 Interrupt Control Register	TB3IC	XXXX X0002
007916	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X0002
007A16	INT5 Interrupt Control Register	INT5IC	XX00 X0002
007B16			
007C16	INT3 Interrupt Control Register	INT3IC	XX00 X0002
007D16	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X0002
007E16	INT1 Interrupt Control Register	INT1IC	XX00 X0002
007F16	Intelligent I/O Interrupt Control Register 10/ CAN Interrupt 1 Control Register	IIO10IC CAN1IC	XXXX X0002
008016			
008116	CAN Interrupt 2 Control Register	CAN2IC	XXXX X0002
008216			
008316			
008416			
008516			
008616			
008716			
008816	DMA1 Interrupt Control Register	DM1IC	XXXX X0002
008916	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X0002
008A16	DMA3 Interrupt Control Register	DM3IC	XXXX X0002
008B16	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X0002
008C16	Timer A1 Interrupt Control Register	TA1IC	XXXX X0002
008D16	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X0002
008E16	Timer A3 Interrupt Control Register	TA3IC	XXXX X0002
008F16	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X0002

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
009016	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X0002
009116	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X0002
009216	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X0002
009316	Key Input Interrupt Control Register	KUPIC	XXXX X0002
009416	Timer B0 Interrupt Control Register	TB0IC	XXXX X0002
009516	Intelligent I/O Interrupt Control Register 1 CAN Interrupt 4 Control Register	IIO1IC CAN4IC	XXXX X0002
009616	Timer B2 Interrupt Control Register	TB2IC	XXXX X0002
009716	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X0002
009816	Timer B4 Interrupt Control Register	TB4IC	XXXX X0002
009916	CAN Interrupt 5 Control Register	CAN5IC	XXXX X0002
009A16	INT4 Interrupt Control Register	INT4IC	XX00 X0002
009B16			
009C16	INT2 Interrupt Control Register	INT2IC	XX00 X0002
009D16	Intelligent I/O Interrupt Control Register 9/ CAN Interrupt 0 Control Register	IIO9IC CAN0IC	XXXX X0002
009E16	INT0 Interrupt Control Register	INT0IC	XX00 X0002
009F16	Exit Priority Control Register	RLVL	XXXX 00002
00A016	Interrupt Request Register 0	IIO0IR	0000 000X2
00A116	Interrupt Request Register 1	IIO1IR	0000 000X2
00A216	Interrupt Request Register 2	IIO2IR	0000 000X2
00A316	Interrupt Request Register 3	IIO3IR	0000 000X2
00A416	Interrupt Request Register 4	IIO4IR	0000 000X2
00A516	Interrupt Request Register 5	IIO5IR	0000 000X2
00A616			
00A716			
00A816	Interrupt Request Register 8	IIO8IR	0000 000X2
00A916	Interrupt Request Register 9	IIO9IR	0000 000X2
00AA16	Interrupt Request Register 10	IIO10IR	0000 000X2
00AB16	Interrupt Request Register 11	IIO11IR	0000 000X2
00AC16			
00AD16			
00AE16			
00AF16			
00B016	Interrupt Enable Register 0	IIO0IE	0016
00B116	Interrupt Enable Register 1	IIO1IE	0016
00B216	Interrupt Enable Register 2	IIO2IE	0016
00B316	Interrupt Enable Register 3	IIO3IE	0016
00B416	Interrupt Enable Register 4	IIO4IE	0016
00B516	Interrupt Enable Register 5	IIO5IE	0016
00B616			
00B716			
00B816	Interrupt Enable Register 8	IIO8IE	0016
00B916	Interrupt Enable Register 9	IIO9IE	0016
00BA16	Interrupt Enable Register 10	IIO10IE	0016
00BB16	Interrupt Enable Register 11	IIO11IE	0016
00BC16			
00BD16			
00BE16			
00BF16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0₁₆			
00C1₁₆			
00C2₁₆			
00C3₁₆			
00C4₁₆			
00C5₁₆			
00C6₁₆			
00C7₁₆			
00C8₁₆			
00C9₁₆			
00CA₁₆			
00CB₁₆			
00CC₁₆			
00CD₁₆			
00CE₁₆			
00CF₁₆			
00D0₁₆			
00D1₁₆			
00D2₁₆			
00D3₁₆			
00D4₁₆			
00D5₁₆			
00D6₁₆			
00D7₁₆			
00D8₁₆			
00D9₁₆			
00DA₁₆			
00DB₁₆			
00DC₁₆			
00DD₁₆			
00DE₁₆			
00DF₁₆			
00E0₁₆			
00E1₁₆			
00E2₁₆			
00E3₁₆			
00E4₁₆			
00E5₁₆			
00E6₁₆			
00E7₁₆			
00E8₁₆ 00E9₁₆	SI/O Receive Buffer Register 0	G0RB	XXXX XXXX₂ XX00 XXXX₂
00EA₁₆	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX₁₆
00EB₁₆			
00EC₁₆	Receive Input Register 0	G0RI	XX₁₆
00ED₁₆	SI/O Communication Mode Register 0	G0MR	00₁₆
00EE₁₆	Transmit Output Register 0	G0TO	XX₁₆
00EF₁₆	SI/O Communication Control Register 0	G0CR	0000 X011₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00F016	Data Compare Register 00	G0CMP0	XX16
00F116	Data Compare Register 01	G0CMP1	XX16
00F216	Data Compare Register 02	G0CMP2	XX16
00F316	Data Compare Register 03	G0CMP3	XX16
00F416	Data Mask Register 00	G0MSK0	XX16
00F516	Data Mask Register 01	G0MSK1	XX16
00F616	Communication Clock Select Register	CCS	XXXX 00002
00F716			
00F816	Receive CRC Code Register 0	G0RCRC	XX16
00F916			XX16
00FA16	Transmit CRC Code Register 0	G0TCRC	0016
00FB16			0016
00FC16	SI/O Extended Mode Register 0	G0EMR	0016
00FD16	SI/O Extended Receive Control Register 0	G0ERC	0016
00FE16	SI/O Special Communication Interrupt Detect Register 0	G0IRF	0016
00FF16	SI/O Extended Transmit Control Register 0	G0ETC	0000 0XXX2
010016	Time Measurement/Waveform Generating Register 10	G1TM0/G1PO0	XX16
010116			XX16
010216	Time Measurement/Waveform Generating Register 11	G1TM1/G1PO1	XX16
010316			XX16
010416	Time Measurement/Waveform Generating Register 12	G1TM2/G1PO2	XX16
010516			XX16
010616	Time Measurement/Waveform Generating Register 13	G1TM3/G1PO3	XX16
010716			XX16
010816	Time Measurement/Waveform Generating Register 14	G1TM4/G1PO4	XX16
010916			XX16
010A16	Time Measurement/Waveform Generating Register 15	G1TM5/G1PO5	XX16
010B16			XX16
010C16	Time Measurement/Waveform Generating Register 16	G1TM6/G1PO6	XX16
010D16			XX16
010E16	Time Measurement/Waveform Generating Register 17	G1TM7/G1PO7	XX16
010F16			XX16
011016	Waveform Generating Control Register 10	G1POCR0	0000 X0002
011116	Waveform Generating Control Register 11	G1POCR1	0X00 X0002
011216	Waveform Generating Control Register 12	G1POCR2	0X00 X0002
011316	Waveform Generating Control Register 13	G1POCR3	0X00 X0002
011416	Waveform Generating Control Register 14	G1POCR4	0X00 X0002
011516	Waveform Generating Control Register 15	G1POCR5	0X00 X0002
011616	Waveform Generating Control Register 16	G1POCR6	0X00 X0002
011716	Waveform Generating Control Register 17	G1POCR7	0X00 X0002
011816	Time Measurement Control Register 10	G1TMCR0	0016
011916	Time Measurement Control Register 11	G1TMCR1	0016
011A16	Time Measurement Control Register 12	G1TMCR2	0016
011B16	Time Measurement Control Register 13	G1TMCR3	0016
011C16	Time Measurement Control Register 14	G1TMCR4	0016
011D16	Time Measurement Control Register 15	G1TMCR5	0016
011E16	Time Measurement Control Register 16	G1TMCR6	0016
011F16	Time Measurement Control Register 17	G1TMCR7	0016

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
012016	Base Timer Register 1	G1BT	XX16
012116			XX16
012216	Base Timer Control Register 10	G1BCR0	0016
012316	Base Timer Control Register 11	G1BCR1	0016
012416	Time Measurement Prescaler Register 16	G1TPR6	0016
012516	Time Measurement Prescaler Register 17	G1TPR7	0016
012616	Function Enable Register 1	G1FE	0016
012716	Function Select Register 1	G1FS	0016
012816	SI/O Receive Buffer Register 1	G1RB	XXXX XXXX2
012916			XX00 XXXX2
012A16	Transmit Buffer/Receive Data Register 1	G1TB/G1DR	XX16
012B16			
012C16	Receive Input Register 1	G1RI	XX16
012D16	SI/O Communication Mode Register 1	G1MR	0016
012E16	Transmit Output Register 1	G1TO	XX16
012F16	SI/O Communication Control Register 1	G1CR	0000 X0112
013016	Data Compare Register 10	G1CMP0	XX16
013116	Data Compare Register 11	G1CMP1	XX16
013216	Data Compare Register 12	G1CMP2	XX16
013316	Data Compare Register 13	G1CMP3	XX16
013416	Data Mask Register 10	G1MSK0	XX16
013516	Data Mask Register 11	G1MSK1	XX16
013616			
013716			
013816	Receive CRC Code Register 1	G1RCRC	XX16
013916			XX16
013A16	Transmit CRC Code Register 1	G1TCRC	0016
013B16			0016
013C16	SI/O Extended Mode Register 1	G1EMR	0016
013D16	SI/O Extended Receive Control Register 1	G1ERC	0016
013E16	SI/O Special Communication Interrupt Detect Register 1	G1IRF	0016
013F16	SI/O Extended Transmit Control Register 1	G1ETC	0000 0XXX2
014016			
014116			
014216			
014316			
014416			
014516			
014616			
014716			
014816			
014916			
014A16			
014B16			
014C16			
014D16			
014E16			
014F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0150₁₆			
0151₁₆			
0152₁₆			
0153₁₆			
0154₁₆			
0155₁₆			
0156₁₆			
0157₁₆			
0158₁₆			
0159₁₆			
015A₁₆			
015B₁₆			
015C₁₆			
015D₁₆			
015E₁₆			
015F₁₆			
0160₁₆			
0161₁₆			
0162₁₆			
0163₁₆			
0164₁₆			
0165₁₆			
0166₁₆			
0167₁₆			
0168₁₆			
0169₁₆			
016A₁₆			
016B₁₆			
016C₁₆			
016D₁₆			
016E₁₆			
016F₁₆			
0170₁₆			
0171₁₆			
0172₁₆			
0173₁₆			
0174₁₆			
0175₁₆			
0176₁₆			
0177₁₆			
0178₁₆	Input Function Select Register	IPS	00₁₆
0179₁₆	Input Function Select Register A	IPSA	00₁₆
017A₁₆			
017B₁₆			
017C₁₆			
017D₁₆ to 01DF₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
01E016	CAN0 Message Slot Buffer 0 Standard ID0	C0SLOT0_0	XX16
01E116	CAN0 Message Slot Buffer 0 Standard ID1	C0SLOT0_1	XX16
01E216	CAN0 Message Slot Buffer 0 Extended ID0	C0SLOT0_2	XX16
01E316	CAN0 Message Slot Buffer 0 Extended ID1	C0SLOT0_3	XX16
01E416	CAN0 Message Slot Buffer 0 Extended ID2	C0SLOT0_4	XX16
01E516	CAN0 Message Slot Buffer 0 Data Length Code	C0SLOT0_5	XX16
01E616	CAN0 Message Slot Buffer 0 Data 0	C0SLOT0_6	XX16
01E716	CAN0 Message Slot Buffer 0 Data 1	C0SLOT0_7	XX16
01E816	CAN0 Message Slot Buffer 0 Data 2	C0SLOT0_8	XX16
01E916	CAN0 Message Slot Buffer 0 Data 3	C0SLOT0_9	XX16
01EA16	CAN0 Message Slot Buffer 0 Data 4	C0SLOT0_10	XX16
01EB16	CAN0 Message Slot Buffer 0 Data 5	C0SLOT0_11	XX16
01EC16	CAN0 Message Slot Buffer 0 Data 6	C0SLOT0_12	XX16
01ED16	CAN0 Message Slot Buffer 0 Data 7	C0SLOT0_13	XX16
01EE16	CAN0 Message Slot Buffer 0 Time Stamp High-Order	C0SLOT0_14	XX16
01EF16	CAN0 Message Slot Buffer 0 Time Stamp Low-Order	C0SLOT0_15	XX16
01F016	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XX16
01F116	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XX16
01F216	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XX16
01F316	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XX16
01F416	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XX16
01F516	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XX16
01F616	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XX16
01F716	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XX16
01F816	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XX16
01F916	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XX16
01FA16	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XX16
01FB16	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XX16
01FC16	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XX16
01FD16	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XX16
01FE16	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XX16
01FF16	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XX16
020016 020116	CAN0 Control Register 0	C0CTLR0	XX01 0X012(1) XXXX 00002(1)
020216 020316	CAN0 Status Register	C0STR	0000 00002(1) X000 0X012(1)
020416 020516	CAN0 Extended ID Register	C0IDR	0016(1) 0016(1)
020616 020716	CAN0 Configuration Register	C0CONR	0000 XXXX2(1) 0000 00002(1)
020816 020916	CAN0 Time Stamp Register	C0TSR	0016(1) 0016(1)
020A16	CAN0 Transmit Error Count Register	C0TEC	0016(1)
020B16	CAN0 Receive Error Count Register	C0REC	0016(1)
020C16 020D16	CAN0 Slot Interrupt Status Register	C0SISTR	0016(1) 0016(1)
020E16			
020F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
021016 021116	CAN0 Slot Interrupt Mask Register	C0SIMKR	0016(2) 0016(2)
021216			
021316			
021416	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X0002(2)
021516	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X0002(2)
021616	CAN0 Error Cause Register	C0EFR	0016(2)
021716	CAN0 Baud Rate Prescaler	C0BRP	0000 00012(2)
021816			
021916	CAN0 Mode Register	C0MDR	XXXX XX002(2)
021A16			
021B16			
021C16			
021D16			
021E16			
021F16			
022016 022116	CAN0 Single Shot Control Register	C0SSCTLR	0016(2) 0016(2)
022216			
022316			
022416 022516	CAN0 Single Shot Status Register	C0SSSTR	0016(2) 0016(2)
022616			
022716			
022816	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 00002(2)
022916	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 00002(2)
022A16	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 00002(2)
022B16	CAN0 Global Mask Register Extended ID1	C0GMR3	0016(2)
022C16	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 00002(2)
022D16			
022E16			
022F16			
023016	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 00002(2) XXX0 00002(2)
023116	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 00002(2) XX00 00002(2)
023216	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 00002(2) XXXX 00002(2)
023316	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	0016(2) 0016(2)
023416	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 00002(2) XX00 00002(2)
023516	CAN0 Message Slot 5 Control Register	C0MCTL5	0016(2)
023616	CAN0 Message Slot 6 Control Register	C0MCTL6	0016(2)
023716	CAN0 Message Slot 7 Control Register	C0MCTL7	0016(2)
023816	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 00002(2) XXX0 00002(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
023916	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 00002(2) XX00 00002(2)
023A16	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10/ C0LMBR2	0000 00002(2) XXXX 00002(2)
023B16	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11/ C0LMBR3	0016(2) 0016(2)
023C16	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12/ C0LMBR4	0000 00002(2) XX00 00002(2)
023D16	CAN0 Message Slot 13 Control Register	C0MCTL13	0016(2)
023E16	CAN0 Message Slot 14 Control Register	C0MCTL14	0016(2)
023F16	CAN0 Message Slot 15 Control Register	C0MCTL15	0016(2)
024016	CAN0 Slot Buffer Select Register	C0SBS	0016(2)
024116	CAN0 Control Register 1	C0CTLR1	X000 00XX2(2)
024216	CAN0 Sleep Control Register	C0SLPR	XXXX XXX02
024316			
024416 024516	CAN0 Acceptance Filter Support Register	C0AFS	0016(2) 0116(2)
024616			
024716			
024816			
024916			
024A16			
024B16			
024C16			
024D16			
024E16			
024F16			
025016	CAN1 Slot Buffer Select Register	C1SBS	0016(3)
025116	CAN1 Control Register 1	C1CTLR1	X000 00XX2(3)
025216	CAN1 Sleep Control Register	C1SLPR	XXXX XXX02(3)
025316			
025416 025516	CAN1 Acceptance Filter Support Register	C1AFS	0016(2) 0116(2)
025616			
025716			
025816			
025916			
025A16			
025B16			
025C16			
025D16			
025E16			
025F16			

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.
3. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
026016	CAN1 Message Slot Buffer 0 Standard ID0	C1SLOT0_0	XX16
026116	CAN1 Message Slot Buffer 0 Standard ID1	C1SLOT0_1	XX16
026216	CAN1 Message Slot Buffer 0 Extended ID0	C1SLOT0_2	XX16
026316	CAN1 Message Slot Buffer 0 Extended ID1	C1SLOT0_3	XX16
026416	CAN1 Message Slot Buffer 0 Extended ID2	C1SLOT0_4	XX16
026516	CAN1 Message Slot Buffer 0 Data Length Code	C1SLOT0_5	XX16
026616	CAN1 Message Slot Buffer 0 Data 0	C1SLOT0_6	XX16
026716	CAN1 Message Slot Buffer 0 Data 1	C1SLOT0_7	XX16
026816	CAN1 Message Slot Buffer 0 Data 2	C1SLOT0_8	XX16
026916	CAN1 Message Slot Buffer 0 Data 3	C1SLOT0_9	XX16
026A16	CAN1 Message Slot Buffer 0 Data 4	C1SLOT0_10	XX16
026B16	CAN1 Message Slot Buffer 0 Data 5	C1SLOT0_11	XX16
026C16	CAN1 Message Slot Buffer 0 Data 6	C1SLOT0_12	XX16
026D16	CAN1 Message Slot Buffer 0 Data 7	C1SLOT0_13	XX16
026E16	CAN1 Message Slot Buffer 0 Time Stamp High-Order	C1SLOT0_14	XX16
026F16	CAN1 Message Slot Buffer 0 Time Stamp Low-Order	C1SLOT0_15	XX16
027016	CAN1 Message Slot Buffer 1 Standard ID0	C1SLOT1_0	XX16
027116	CAN1 Message Slot Buffer 1 Standard ID1	C1SLOT1_1	XX16
027216	CAN1 Message Slot Buffer 1 Extended ID0	C1SLOT1_2	XX16
027316	CAN1 Message Slot Buffer 1 Extended ID1	C1SLOT1_3	XX16
027416	CAN1 Message Slot Buffer 1 Extended ID2	C1SLOT1_4	XX16
027516	CAN1 Message Slot Buffer 1 Data Length Code	C1SLOT1_5	XX16
027616	CAN1 Message Slot Buffer 1 Data 0	C1SLOT1_6	XX16
027716	CAN1 Message Slot Buffer 1 Data 1	C1SLOT1_7	XX16
027816	CAN1 Message Slot Buffer 1 Data 2	C1SLOT1_8	XX16
027916	CAN1 Message Slot Buffer 1 Data 3	C1SLOT1_9	XX16
027A16	CAN1 Message Slot Buffer 1 Data 4	C1SLOT1_10	XX16
027B16	CAN1 Message Slot Buffer 1 Data 5	C1SLOT1_11	XX16
027C16	CAN1 Message Slot Buffer 1 Data 6	C1SLOT1_12	XX16
027D16	CAN1 Message Slot Buffer 1 Data 7	C1SLOT1_13	XX16
027E16	CAN1 Message Slot Buffer 1 Time Stamp High-Order	C1SLOT1_14	XX16
027F16	CAN1 Message Slot Buffer 1 Time Stamp Low-Order	C1SLOT1_15	XX16
028016 028116	CAN1 Control Register 0	C1CTLR0	XX01 0X012(1) XXXX 00002(1)
028216 028316	CAN1 Status Register	C1STR	0000 00002(1) X000 0X012(1)
028416 028516	CAN1 Extended ID Register	C1IDR	0016(1) 0016(1)
028616 028716	CAN1 Configuration Register	C1CONR	0000 XXXX2(1) 0000 00002(1)
028816 028916	CAN1 Time Stamp Register	C1TSR	0016(1) 0016(1)
028A16	CAN1 Transmit Error Count Register	C1TEC	0016(1)
028B16	CAN1 Receive Error Count Register	C1REC	0016(1)
028C16 028D16	CAN1 Slot Interrupt Status Register	C1SISTR	0016(1) 0016(1)
028E16			
028F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
029016 029116	CAN1 Slot Interrupt Mask Register	C1SIMKR	0016(2) 0016(2)
029216			
029316			
029416	CAN1 Error Interrupt Mask Register	C1EIMKR	XXXX X0002(2)
029516	CAN1 Error Interrupt Status Register	C1EISTR	XXXX X0002(2)
029616	CAN1 Error Factor Register	C1EFR	0016(2)
029716	CAN1 Baud Rate Prescaler	C1BRP	0000 00012(2)
029816			
029916	CAN1 Mode Register	C1MDR	XXXX XX002(2)
029A16			
029B16			
029C16			
029D16			
029E16			
029F16			
02A016 02A116	CAN1 Single Shot Control Register	C1SSCTLR	0016(2) 0016(2)
02A216			
02A316			
02A416 02A516	CAN1 Single Shot Status Register	C1SSSTR	0016(2) 0016(2)
02A616			
02A716			
02A816	CAN1 Global Mask Register Standard ID0	C1GMR0	XXX0 00002(2)
02A916	CAN1 Global Mask Register Standard ID1	C1GMR1	XX00 00002(2)
02AA16	CAN1 Global Mask Register Extended ID0	C1GMR2	XXXX 00002(2)
02AB16	CAN1 Global Mask Register Extended ID1	C1GMR3	0016(2)
02AC16	CAN1 Global Mask Register Extended ID2	C1GMR4	XX00 00002(2)
02AD16			
02AE16			
02AF16			
02B016	CAN1 Message Slot 0 Control Register / CAN1 Local Mask Register A Standard ID0	C1MCTL0/ C1LMAR0	0000 00002(2) XXX0 00002(2)
02B116	CAN1 Message Slot 1 Control Register / CAN1 Local Mask Register A Standard ID1	C1MCTL1/ C1LMAR1	0000 00002(2) XX00 00002(2)
02B216	CAN1 Message Slot 2 Control Register / CAN1 Local Mask Register A Extended ID0	C1MCTL2/ C1LMAR2	0000 00002(2) XXXX 00002(2)
02B316	CAN1 Message Slot 3 Control Register / CAN1 Local Mask Register A Extended ID1	C1MCTL3/ C1LMAR3	0016(2) 0016(2)
02B416	CAN1 Message Slot 4 Control Register / CAN1 Local Mask Register A Extended ID2	C1MCTL4/ C1LMAR4	0000 00002(2) XX00 00002(2)
02B516	CAN1 Message Slot 5 Control Register	C1MCTL5	0016(2)
02B616	CAN1 Message Slot 6 Control Register	C1MCTL6	0016(2)
02B716	CAN1 Message Slot 7 Control Register	C1MCTL7	0016(2)
02B816	CAN1 Message Slot 8 Control Register / CAN1 Local Mask Register B Standard ID0	C1MCTL8/ C1LMBR0	0000 00002(2) XXX0 00002(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C1CTLR1 register switches functions for addresses 02A016 to 02BF16.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02B9₁₆	CAN1 Message Slot 9 Control Register / CAN1 Local Mask Register B Standard ID1	C1MCTL9/ C1LMBR1	0000 0000₂(2) XX00 0000₂(2)
02BA₁₆	CAN1 Message Slot 10 Control Register / CAN1 Local Mask Register B Extended ID0	C1MCTL10/ C1LMBR2	0000 0000₂(2) XXXX 0000₂(2)
02BB₁₆	CAN1 Message Slot 11 Control Register / CAN1 Local Mask Register B Extended ID1	C1MCTL11/ C1LMBR3	00₁₆(2) 00₁₆(2)
02BC₁₆	CAN1 Message Slot 12 Control Register / CAN1 Local Mask Register B Extended ID2	C1MCTL12/ C1LMBR4	0000 0000₂(2) XX00 0000₂(2)
02BD₁₆	CAN1 Message Slot 13 Control Register	C1MCTL13	00₁₆(2)
02BE₁₆	CAN1 Message Slot 14 Control Register	C1MCTL14	00₁₆(2)
02BF₁₆	CAN1 Message Slot 15 Control Register	C1MCTL15	00₁₆(2)
02C0₁₆ 02C1₁₆	X0 Register Y0 Register	X0R,Y0R	XX₁₆ XX₁₆
02C2₁₆ 02C3₁₆	X1 Register Y1 Register	X1R,Y1R	XX₁₆ XX₁₆
02C4₁₆ 02C5₁₆	X2 Register Y2 Register	X2R,Y2R	XX₁₆ XX₁₆
02C6₁₆ 02C7₁₆	X3 Register Y3 Register	X3R,Y3R	XX₁₆ XX₁₆
02C8₁₆ 02C9₁₆	X4 Register Y4 Register	X4R,Y4R	XX₁₆ XX₁₆
02CA₁₆ 02CB₁₆	X5 Register Y5 Register	X5R,Y5R	XX₁₆ XX₁₆
02CC₁₆ 02CD₁₆	X6 Register Y6 Register	X6R,Y6R	XX₁₆ XX₁₆
02CE₁₆ 02CF₁₆	X7 Register Y7 Register	X7R,Y7R	XX₁₆ XX₁₆
02D0₁₆ 02D1₁₆	X8 Register Y8 Register	X8R,Y8R	XX₁₆ XX₁₆
02D2₁₆ 02D3₁₆	X9 Register Y9 Register	X9R,Y9R	XX₁₆ XX₁₆
02D4₁₆ 02D5₁₆	X10 Register Y10 Register	X10R,Y10R	XX₁₆ XX₁₆
02D6₁₆ 02D7₁₆	X11 Register Y11 Register	X11R,Y11R	XX₁₆ XX₁₆
02D8₁₆ 02D9₁₆	X12 Register Y12 Register	X12R,Y12R	XX₁₆ XX₁₆
02DA₁₆ 02DB₁₆	X13 Register Y13 Register	X13R,Y13R	XX₁₆ XX₁₆
02DC₁₆ 02DD₁₆	X14 Register Y14 Register	X14R,Y14R	XX₁₆ XX₁₆
02DE₁₆ 02DF₁₆	X15 Register Y15 Register	X15R,Y15R	XX₁₆ XX₁₆

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C1CTLR1 register switches functions for addresses 02A0₁₆ to 02BF₁₆.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02E0₁₆	XY Control Register	XYC	XXXX XX00₂
02E1₁₆			
02E2₁₆			
02E3₁₆			
02E4₁₆	UART1 Special Mode Register 4	U1SMR4	00₁₆
02E5₁₆	UART1 Special Mode Register 3	U1SMR3	00₁₆
02E6₁₆	UART1 Special Mode Register 2	U1SMR2	00₁₆
02E7₁₆	UART1 Special Mode Register	U1SMR	00₁₆
02E8₁₆	UART1 Transmit/Receive Mode Register	U1MR	00₁₆
02E9₁₆	UART1 Baud Rate Register	U1BRG	XX₁₆
02EA₁₆	UART1 Transmit Buffer Register	U1TB	XX₁₆
02EB₁₆			XX₁₆
02EC₁₆	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000₂
02ED₁₆	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010₂
02EE₁₆	UART1 Receive Buffer Register	U1RB	XX₁₆
02EF₁₆			XX₁₆
02F0₁₆			
02F1₁₆			
02F2₁₆			
02F3₁₆			
02F4₁₆	UART4 Special Mode Register 4	U4SMR4	00₁₆
02F5₁₆	UART4 Special Mode Register 3	U4SMR3	00₁₆
02F6₁₆	UART4 Special Mode Register 2	U4SMR2	00₁₆
02F7₁₆	UART4 Special Mode Register	U4SMR	00₁₆
02F8₁₆	UART4 Transmit/Receive Mode Register	U4MR	00₁₆
02F9₁₆	UART4 Baud Rate Register	U4BRG	XX₁₆
02FA₁₆	UART4 Transmit Buffer Register	U4TB	XX₁₆
02FB₁₆			XX₁₆
02FC₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000₂
02FD₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010₂
02FE₁₆	UART4 Receive Buffer Register	U4RB	XX₁₆
02FF₁₆			XX₁₆
0300₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX₂
0301₁₆			
0302₁₆	Timer A1-1 Register	TA11	XX₁₆
0303₁₆			XX₁₆
0304₁₆	Timer A2-1 Register	TA21	XX₁₆
0305₁₆			XX₁₆
0306₁₆	Timer A4-1 Register	TA41	XX₁₆
0307₁₆			XX₁₆
0308₁₆	Three-Phase PWM Control Register 0	INVC0	00₁₆
0309₁₆	Three-Phase PWM Control Register 1	INVC1	00₁₆
030A₁₆	Three-Phase Output Buffer Register 0	IDB0	0011 1111₂
030B₁₆	Three-Phase Output Buffer Register 1	IDB1	0011 1111₂
030C₁₆	Dead Time Timer	DTT	XX₁₆
030D₁₆	Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	XX₁₆
030E₁₆			
030F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
031016 031116	Timer B3 Register	TB3	XX16 XX16
031216 031316	Timer B4 Register	TB4	XX16 XX16
031416 031516	Timer B5 Register	TB5	XX16 XX16
031616			
031716			
031816			
031916			
031A16			
031B16	Timer B3 Mode Register	TB3MR	00XX 00002
031C16	Timer B4 Mode Register	TB4MR	00XX 00002
031D16	Timer B5 Mode Register	TB5MR	00XX 00002
031E16			
031F16	External Interrupt Cause Select Register	IFSR	0016
032016			
032116			
032216			
032316			
032416	UART3 Special Mode Register 4	U3SMR4	0016
032516	UART3 Special Mode Register 3	U3SMR3	0016
032616	UART3 Special Mode Register 2	U3SMR2	0016
032716	UART3 Special Mode Register	U3SMR	0016
032816	UART3 Transmit/Receive Mode Register	U3MR	0016
032916	UART3 Baud Rate Register	U3BRG	XX16
032A16 032B16	UART3 Transmit Buffer Register	U3TB	XX16 XX16
032C16	UART3 Transmit/Receive Control Register 0	U3C0	0000 10002
032D16	UART3 Transmit/Receive Control Register 1	U3C1	0000 00102
032E16 032F16	UART3 Receive Buffer Register	U3RB	XX16 XX16
033016			
033116			
033216			
033316			
033416	UART2 Special Mode Register 4	U2SMR4	0016
033516	UART2 Special Mode Register 3	U2SMR3	0016
033616	UART2 Special Mode Register 2	U2SMR2	0016
033716	UART2 Special Mode Register	U2SMR	0016
033816	UART2 Transmit/Receive Mode Register	U2MR	0016
033916	UART2 Baud Rate Register	U2BRG	XX16
033A16 033B16	UART2 Transmit Buffer Register	U2TB	XX16 XX16
033C16	UART2 Transmit/Receive Control Register 0	U2C0	0000 10002
033D16	UART2 Transmit/Receive Control Register 1	U2C1	0000 00102
033E16 033F16	UART2 Receive Buffer Register	U2RB	XX16 XX16

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
034016	Count Start Flag	TABSR	0016
034116	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX2
034216	One-Shot Start Flag	ONSF	0016
034316	Trigger Select Register	TRGSR	0016
034416	Up-Down Flag	UDF	0016
034516			
034616	Timer A0 Register	TA0	XX16
034716			XX16
034816	Timer A1 Register	TA1	XX16
034916			XX16
034A16	Timer A2 Register	TA2	XX16
034B16			XX16
034C16	Timer A3 Register	TA3	XX16
034D16			XX16
034E16	Timer A4 Register	TA4	XX16
034F16			XX16
035016	Timer B0 Register	TB0	XX16
035116			XX16
035216	Timer B1 Register	TB1	XX16
035316			XX16
035416	Timer B2 Register	TB2	XX16
035516			XX16
035616	Timer A0 Mode Register	TA0MR	0016
035716	Timer A1 Mode Register	TA1MR	0016
035816	Timer A2 Mode Register	TA2MR	0016
035916	Timer A3 Mode Register	TA3MR	0016
035A16	Timer A4 Mode Register	TA4MR	0016
035B16	Timer B0 Mode Register	TB0MR	00XX 00002
035C16	Timer B1 Mode Register	TB1MR	00XX 00002
035D16	Timer B2 Mode Register	TB2MR	00XX 00002
035E16	Timer B2 Special Mode Register	TB2SC	XXXX XXX02
035F16	Count Source Prescaler Register(1)	TCSPR	0016
036016			
036116			
036216			
036316			
036416	UART0 Special Mode Register 4	U0SMR4	0016
036516	UART0 Special Mode Register 3	U0SMR3	0016
036616	UART0 Special Mode Register 2	U0SMR2	0016
036716	UART0 Special Mode Register	U0SMR	0016
036816	UART0 Transmit/Receive Mode Register	U0MR	0016
036916	UART0 Baud Rate Register	U0BRG	XX16
036A16	UART0 Transmit Buffer Register	U0TB	XX16
036B16			XX16
036C16	UART0 Transmit/Receive Control Register 0	U0C0	0000 10002
036D16	UART0 Transmit/Receive Control Register 1	U0C1	0000 00102
036E16	UART0 Receive Buffer Register	U0RB	XX16
036F16			XX16

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. TCSPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed

Address	Register	Symbol	Value after RESET
037016			
037116			
037216			
037316			
037416			
037516			
037616			
037716			
037816	DMA0 Factor Select Register	DM0SL	0016
037916	DMA1 Factor Select Register	DM1SL	0016
037A16	DMA2 Factor Select Register	DM2SL	0016
037B16	DMA3 Factor Select Register	DM3SL	0016
037C16 037D16	CRC Data Register	CRCD	XX16 XX16
037E16	CRC Input Register	CRCIN	XX16
037F16			
038016 038116	A/D0 Register 0	AD00	XXXX XXXX2 0000 00002
038216 038316	A/D0 Register 1	AD01	XX16 XX16
038416 038516	A/D0 Register 2	AD02	XX16 XX16
038616 038716	A/D0 Register 3	AD03	XX16 XX16
038816 038916	A/D0 Register 4	AD04	XX16 XX16
038A16 038B16	A/D0 Register 5	AD05	XX16 XX16
038C16 038D16	A/D0 Register 6	AD06	XX16 XX16
038E16 038F16	A/D0 Register 7	AD07	XX16 XX16
039016			
039116			
039216	A/D0 Control Register 4	AD0CON4	XXXX 00XX2
039316			
039416	A/D0 Control Register 2	AD0CON2	XX0X X0002
039516	A/D0 Control Register 3	AD0CON3	XXXX X0002
039616	A/D0 Control Register 0	AD0CON0	0016
039716	A/D0 Control Register 1	AD0CON1	0016
039816	D/A Register 0	DA0	XX16
039916			
039A16	D/A Register 1	DA1	XX16
039B16			
039C16	D/A Control Register	DACON	XXXX XX002
039D16			
039E16			
039F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$	Function Select Register A8	PS8	X000 0000$_2$
03A1$_{16}$	Function Select Register A9	PS9	00$_{16}$
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function Select Register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function Select Register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function Select Register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function Select Register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function Select Register A0	PS0	00$_{16}$
03B1$_{16}$	Function Select Register A1	PS1	00$_{16}$
03B2$_{16}$	Function Select Register B0	PSL0	00$_{16}$
03B3$_{16}$	Function Select Register B1	PSL1	00$_{16}$
03B4$_{16}$	Function Select Register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function Select Register A3	PS3	00$_{16}$
03B6$_{16}$	Function Select Register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function Select Register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$	Function Select Register A5	PS5	XXX0 0000$_2$
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 Register	P6	XX$_{16}$
03C1$_{16}$	Port P7 Register	P7	XX$_{16}$
03C2$_{16}$	Port P6 Direction Register	PD6	00$_{16}$
03C3$_{16}$	Port P7 Direction Register	PD7	00$_{16}$
03C4$_{16}$	Port P8 Register	P8	XX$_{16}$
03C5$_{16}$	Port P9 Register	P9	XX$_{16}$
03C6$_{16}$	Port P8 Direction Register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 Direction Register	PD9	00$_{16}$
03C8$_{16}$	Port P10 Register	P10	XX$_{16}$
03C9$_{16}$	Port P11 Register	P11	XX$_{16}$
03CA$_{16}$	Port P10 Direction Register	PD10	00$_{16}$
03CB$_{16}$	Port P11 Direction Register	PD11	XXX0 0000$_2$
03CC$_{16}$	Port P12 Register	P12	XX$_{16}$
03CD$_{16}$	Port P13 Register	P13	XX$_{16}$
03CE$_{16}$	Port P12 Direction Register	PD12	00$_{16}$
03CF$_{16}$	Port P13 Direction Register	PD13	00$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03D0₁₆	Port P14 Register	P14	XX₁₆
03D1₁₆	Port P15 Register	P15	XX₁₆
03D2₁₆	Port P14 Direction Register	PD14	X000 0000₂
03D3₁₆	Port P15 Direction Register	PD15	00₁₆
03D4₁₆			
03D5₁₆			
03D6₁₆			
03D7₁₆			
03D8₁₆			
03D9₁₆			
03DA₁₆	Pull-Up Control Register 2	PUR2	00₁₆
03DB₁₆	Pull-Up Control Register 3	PUR3	00₁₆
03DC₁₆	Pull-Up Control Register 4	PUR4	XXXX 0000₂
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 Register	P0	XX₁₆
03E1₁₆	Port P1 Register	P1	XX₁₆
03E2₁₆	Port P0 Direction Register	PD0	00₁₆
03E3₁₆	Port P1 Direction Register	PD1	00₁₆
03E4₁₆	Port P2 Register	P2	XX₁₆
03E5₁₆	Port P3 Register	P3	XX₁₆
03E6₁₆	Port P2 Direction Register	PD2	00₁₆
03E7₁₆	Port P3 Direction Register	PD3	00₁₆
03E8₁₆	Port P4 Register	P4	XX₁₆
03E9₁₆	Port P5 Register	P5	XX₁₆
03EA₁₆	Port P4 Direction Register	PD4	00₁₆
03EB₁₆	Port P5 Direction Register	PD5	00₁₆
03EC₁₆			
03ED₁₆			
03EE₁₆			
03EF₁₆			
03F0₁₆	Pull-Up Control Register 0	PUR0	00₁₆
03F1₁₆	Pull-Up Control Register 1	PUR1	XXXX 0000₂
03F2₁₆			
03F3₁₆			
03F4₁₆			
03F5₁₆			
03F6₁₆			
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆			
03FD₁₆			
03FE₁₆			
03FF₁₆	Port Control Register	PCR	XXXX XXX0₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$			
03A1$_{16}$			
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function Select Register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function Select Register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function Select Register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function Select Register C	PSC	0X00 0000$_2$
03B0$_{16}$	Function Select Register A0	PS0	00$_{16}$
03B1$_{16}$	Function Select Register A1	PS1	00$_{16}$
03B2$_{16}$	Function Select Register B0	PSL0	00$_{16}$
03B3$_{16}$	Function Select Register B1	PSL1	00$_{16}$
03B4$_{16}$	Function Select Register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function Select Register A3	PS3	00$_{16}$
03B6$_{16}$	Function Select Register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function Select Register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$			
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 Register	P6	XX$_{16}$
03C1$_{16}$	Port P7 Register	P7	XX$_{16}$
03C2$_{16}$	Port P6 Direction Register	PD6	00$_{16}$
03C3$_{16}$	Port P7 Direction Register	PD7	00$_{16}$
03C4$_{16}$	Port P8 Register	P8	XX$_{16}$
03C5$_{16}$	Port P9 Register	P9	XX$_{16}$
03C6$_{16}$	Port P8 Direction Register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 Direction Register	PD9	00$_{16}$
03C8$_{16}$	Port P10 Register	P10	XX$_{16}$
03C9$_{16}$			
03CA$_{16}$	Port P10 Direction Register	PD10	00$_{16}$
03CB$_{16}$	Set default value to "FF$_{16}$"		
03CC$_{16}$			
03CD$_{16}$			
03CE$_{16}$	Set default value to "FF$_{16}$"		
03CF$_{16}$	Set default value to "FF$_{16}$"		

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin package>

Address	Register	Symbol	Value after RESET
03D0$_{16}$			
03D1$_{16}$			
03D2$_{16}$	Set default value to "FF$_{16}$"		
03D3$_{16}$	Set default value to "FF$_{16}$"		
03D4$_{16}$			
03D5$_{16}$			
03D6$_{16}$			
03D7$_{16}$			
03D8$_{16}$			
03D9$_{16}$			
03DA$_{16}$	Pull-Up Control Register 2	PUR2	00$_{16}$
03DB$_{16}$	Pull-Up Control Register 3	PUR3	00$_{16}$
03DC$_{16}$	Set default value to "00$_{16}$"		
03DD$_{16}$			
03DE$_{16}$			
03DF$_{16}$			
03E0$_{16}$	Port P0 Register	P0	XX$_{16}$
03E1$_{16}$	Port P1 Register	P1	XX$_{16}$
03E2$_{16}$	Port P0 Direction Register	PD0	00$_{16}$
03E3$_{16}$	Port P1 Direction Register	PD1	00$_{16}$
03E4$_{16}$	Port P2 Register	P2	XX$_{16}$
03E5$_{16}$	Port P3 Register	P3	XX$_{16}$
03E6$_{16}$	Port P2 Direction Register	PD2	00$_{16}$
03E7$_{16}$	Port P3 Direction Register	PD3	00$_{16}$
03E8$_{16}$	Port P4 Register	P4	XX$_{16}$
03E9$_{16}$	Port P5 Register	P5	XX$_{16}$
03EA$_{16}$	Port P4 Direction Register	PD4	00$_{16}$
03EB$_{16}$	Port P5 Direction Register	PD5	00$_{16}$
03EC$_{16}$			
03ED$_{16}$			
03EE$_{16}$			
03EF$_{16}$			
03F0$_{16}$	Pull-up Control Register 0	PUR0	00$_{16}$
03F1$_{16}$	Pull-up Control Register 1	PUR1	XXXX 0000$_2$
03F2$_{16}$			
03F3$_{16}$			
03F4$_{16}$			
03F5$_{16}$			
03F6$_{16}$			
03F7$_{16}$			
03F8$_{16}$			
03F9$_{16}$			
03FA$_{16}$			
03FB$_{16}$			
03FC$_{16}$			
03FD$_{16}$			
03FE$_{16}$			
03FF$_{16}$	Port Control Register	PCR	XXXX XXX0$_2$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

5. Electrical Characteristics

5.1 Electrical Characteristics (M32C/85)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V_{CC1}, V_{CC2}	Supply Voltage		V_{CC1}=AV$_{CC}$	-0.3 to 6.0	V
V_{CC2}	Supply Voltage		-	-0.3 to V_{CC1}	V
AV$_{CC}$	Analog Supply Voltage		V_{CC1}=AV$_{CC}$	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNV$_{SS}$, BYTE, P6$_0$-P6$_7$, P7$_2$-P7$_7$, P8$_0$-P8$_7$, P9$_0$-P9$_7$, P10$_0$-P10$_7$, P14$_0$-P14$_6$, P15$_0$-P15$_7$(1), V_{REF}, X$_{IN}$		-0.3 to V_{CC1}+0.3	V
		P0$_0$-P0$_7$, P1$_0$-P1$_7$, P2$_0$-P2$_7$, P3$_0$-P3$_7$, P4$_0$-P4$_7$, P5$_0$-P5$_7$, P11$_0$-P11$_4$, P12$_0$-P12$_7$, P13$_0$-P13$_7$(1)		-0.3 to V_{CC2}+0.3	
		P7$_0$, P7$_1$		-0.3 to 6.0	
V_O	Output Voltage	P6$_0$-P6$_7$, P7$_2$-P7$_7$, P8$_0$-P8$_4$, P8$_6$, P8$_7$, P9$_0$-P9$_7$, P10$_0$-P10$_7$, P14$_0$-P14$_6$, P15$_0$-P15$_7$(1), X$_{OUT}$		-0.3 to V_{CC1}+0.3	V
		P0$_0$-P0$_7$, P1$_0$-P1$_7$, P2$_0$-P2$_7$, P3$_0$-P3$_7$, P4$_0$-P4$_7$, P5$_0$-P5$_7$, P11$_0$-P11$_4$, P12$_0$-P12$_7$, P13$_0$-P13$_7$(1)		-0.3 to V_{CC2}+0.3	
Pd	Power Dissipation		Topr=25° C	500	mW
Topr	Operating Ambient Temperature	during CPU operation		-20 to 85/ -40 to 85(2)	° C
		during flash memory program and erase operation		0 to 60	
Tstg	Storage Temperature			-65 to 150	° C

NOTES:
1. P11 to P15 are provided in the 144-pin package only.
2. Contact Renesas Technology Sales Co., Ltd, if temperature range of -40 to 85° C is required.

Table 5.2 Recommended Operating Conditions

(V_{CC1}= V_{CC2}=3.0V to 5.5V at Topr=– 20 to 85°C unless otherwise specified)

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply Voltage ($V_{CC1} \geq V_{CC2}$)	3.0	5.0	5.5	V
AVcc	Analog Supply Voltage		V_{CC1}		V
Vss	Supply Voltage		0		V
AVss	Analog Supply Voltage		0		V

Table 5.2 Recommended Operating Conditions (Continued)

(V_{CC1}=V_{CC2}=3.0V to 5.5V at Topr=–20 to 85°C unless otherwise specified)

Symbol	Parameter	Accommodating Pins	Standard			Unit
			Min.	Typ.	Max.	
V_{IH}	Input High ("H") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0.8V_{CC2}		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0.8V_{CC1}		V_{CC1}	
		$P7_0$, $P7_1$	0.8V_{CC1}		6.0	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)	0.8V_{CC2}		V_{CC2}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)	0.5V_{CC2}		V_{CC2}	V
V_{IL}	Input Low ("L") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0		0.2V_{CC2}	V
		$P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0		0.2V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)	0		0.2V_{CC2}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)	0		0.16V_{CC2}	V
$I_{OH(peak)}$	Peak Output High ("H") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			5.0	mA

NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, and P11 must be -40mA or less.
   Total $I_{OH(peak)}$ for $P8_6$, $P8_7$, P9, P10, P14 and P15 must be -40mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P12 and P13 must be -40mA or less.
   Total $I_{OH(peak)}$ for P6, P7, and $P8_0$ to $P8_4$ must be -40mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply when $P8_7$ is used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

Table 5.2 Recommended Operating Conditions (Continued)

(V_{CC1}=V_{CC2}=3.0V to 5.5V at Topr=–20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f(X_{IN})$	Main Clock Input Frequency	V_{CC1}=4.2 to 5.5V	0		32	MHz
		V_{CC1}=3.0 to 5.5V	0		24	MHz
$f(X_{CIN})$	Sub Clock Frequency			32.768	50	kHz
$f(_{Ring})$	On-chip Oscillator Frequency			1		MHz
$f(_{PLL})$	PLL Clock Frequency	V_{CC1}=4.2 to 5.5V	10		32	MHz
		V_{CC1}=3.0 to 5.5V	10		24	MHz
$t_{SU(PLL)}$	PLL Lock Time	V_{CC1}=5.0V			5	ms
		V_{CC1}=3.3V			10	ms

$V_{CC1}=V_{CC2}=5V$

Table 5.3 Electrical Characteristics

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= –20 to 85°C, $f(X_{IN})=32MHz$ unless otherwise specified)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$	I_{OH}=-5mA		3.0		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-5mA		3.0		V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$	I_{OH}=-200µA		4.7		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$,$P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-200µA		4.7		V_{CC1}	
		X_{OUT}	I_{OH}=-1mA		3.0			V
		X_{COUT}	High Power	No load applied		2.5		V
			Low Power	No load applied		1.6		
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=5mA				2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=200µA				0.45	V
		X_{OUT}	I_{OL}=1mA				2.0	V
		X_{COUT}	High Power	No load applied		0		V
			Low Power	No load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4			0.2		1.0	V
		$\overline{RESET}$			0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5V				5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V				-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_I=0V	Flash Memory	30	50	167	kΩ
				Masked ROM	20	40	167	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}				1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}				10		MΩ
V_{RAM}	RAM Standby Voltage	In stop mode			2.0			V
I_{CC}	Power Supply Current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	$f(X_{IN})$=32 MHz, square wave, no division			28	45	mA
			$f(X_{CIN})$=32 kHz, in wait mode, Topr=25° C			10		µA
			Topr=25° C (while clock is stopped)			0.8	5	µA
			Topr=85° C (while clock is stopped)				50	µA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=5V$

Table 5.4 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}=4.2$ to 5.5V, $V_{SS}=AV_{SS}=0V$ at Topr=–20 to 85°C, $f(X_{IN})$ = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8.00		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2.00		V_{CC1}	V
V_{IA}	Analog Input Voltage			0.00		V_{REF}	V

NOTES:
1. Divide $f(X_{IN})$, if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. Sample and hold function available.

Table 5.5 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}=4.2$ to 5.5V, $V_{SS}=AV_{SS}=0V$ at Topr=–20 to 85°C, $f(X_{IN})$ = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Table 5.6 Flash Memory Version Electrical Characteristics(1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and Erase Endurance(3)		100			cycles
-	Word Program Time (V_{CC1}=5.0V, Topr=25° C)			25	200	µs
-	Lock Bit Program Time			25	200	µs
-	Block Erase Time (V_{CC1}=5.0V, Topr=25° C)	4-Kbyte Block		0.3	4	s
		8-Kbyte Block		0.3	4	s
		32-Kbyte Block		0.5	4	s
		64-Kbyte Block		0.8	4	s
-	All-Unlocked-Block Erase Time(2)				4 x *n*	s
t_{PS}	Flash Memory Circuit Stabilization Wait Time				15	µs
-	Data Hold Time(4)		10			years

NOTES:
1. Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at Topr = 0 to 60 ° C unless otherwise specified.
2. n denotes the number of block to be erased.
3. Number of program-erase cycles per block.
   If Program and Erase Endurance is *n* cycle (*n*=100), each block can be erased and programmed *n* cycles.
   For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (Rewrite prohibited).
4. Topr = -40 to 85 ° C

$V_{CC1}=V_{CC2}=5V$

Table 5.7 Low Voltage Detect Circuit Electrical Characteristics ($V_{CC1}=V_{CC2}=3.0$ to 5.5V, Vss= AVss=0V at Topr=–20 to 85°C unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Voltage Down Detect Voltage(1)	V_{CC1}=3.0 to 5.5V		3.8		V
Vdet3	Reset Space Detect Voltage(1)			3.0		V
Vdet3s	Low Voltage Reset Hold Voltage		2.0			V
Vdet3r	Low Voltage Reset Release Voltage(2)			3.1		V

NOTES:
1. Vdet4 >Vdet3
2. Vdet3r >Vdet3 is not guaranteed.

Table 5.8 Power Supply Timing

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time for Stable Internal Supply Voltage when Power-on	V_{CC1}=3.0 to 5.5V			2	ms
td(S-R)	Wait Time to Release Voltage Voltage Down Detect Reset	V_{CC1}=Vdet3r to 5.5V		6(1)	20	ms
td(E-A)	Start-up Time for Low Voltage Detect Circuit Operation	V_{CC1}=3.0 to 5.5V			20	µs

NOTES:
1. V_{CC1}=5V

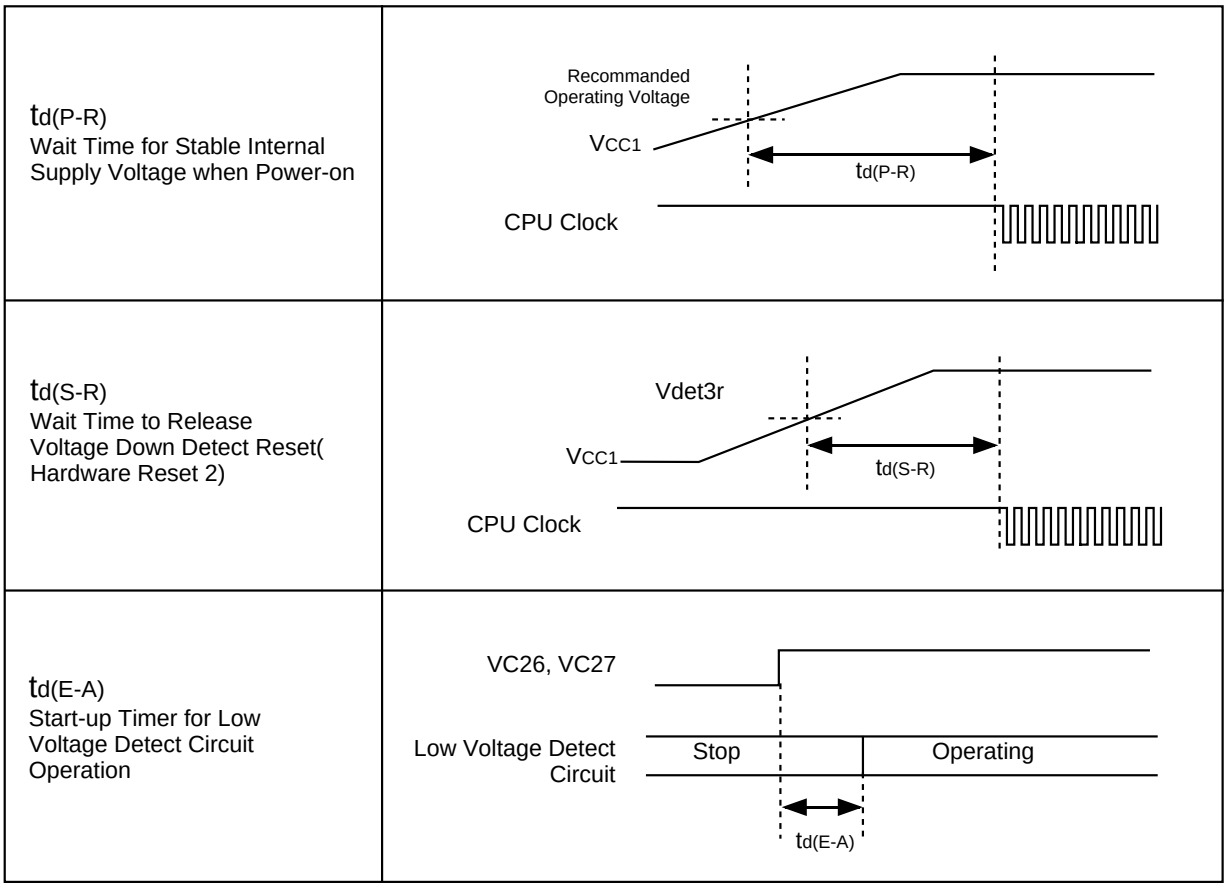


Figure 5.1 Power Supply Timing Diagram

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr=–20 to 85°C unless otherwise specified)

Table 5.9 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$t_{w(H)}$	External Clock Input High ("H") Width	13.75		ns
$t_{w(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.10 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	26		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	26		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	30		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:
1. Values can be obtained from the following equations, according to BCLK frequecncy and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)+1)

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, n=a+b)

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, p={(a+b-1)x2}+1)

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr=–20 to 85°C unless otherwise specified)

Table 5.11 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	40		ns

Table 5.12 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	200		ns

Table 5.13 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.14 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.15 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

(V_{CC1} = V_{CC2} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.16 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on both edges)	80		ns

Table 5.17 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.18 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.19 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for re-trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Width	125		ns

Table 5.20 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.21 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.22 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-5		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{W(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{W(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n=(bx2)-1)

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, m= b)

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics

(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.23 Memory Expansion Mode and Microprocessor Mode (when accessing an external memory space with the multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		(Note 1)		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-5		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(DB-WR)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time (BCLK standard)		-2		ns
$t_{d(AD-ALE)}$	ALE Signal Output Delay Time (address standard)		(Note 3)		ns
$t_{h(ALE-AD)}$	ALE Signal Output Hold Time (address standard)		(Note 4)		ns
$t_{dz(RD-AD)}$	Address Output Float Start Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(RD-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(RD-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, m= (bx2)-1)

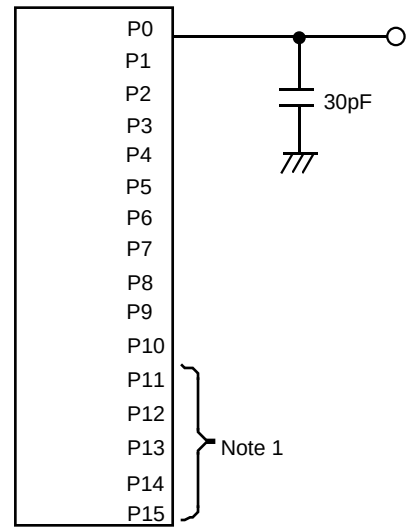
3. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$t_{d(AD-ALE)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n= a)

4. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$t_{h(ALE-AD)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n= a)

$V_{CC1}=V_{CC2}=5V$



NOTES:
1. P11 to P15 are provided in the 144-pin package only.

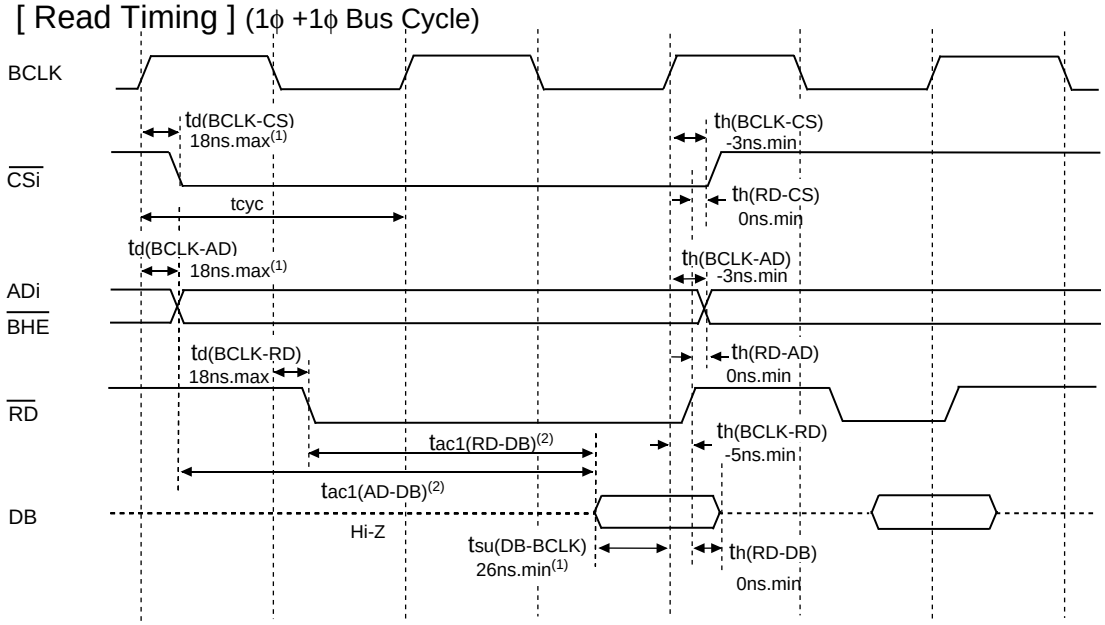
Figure 5.2 P0 to P15 Measurement Circuit

Vcc1=Vcc2=5V

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space)

[Read Timing] (1ϕ +1ϕ Bus Cycle)



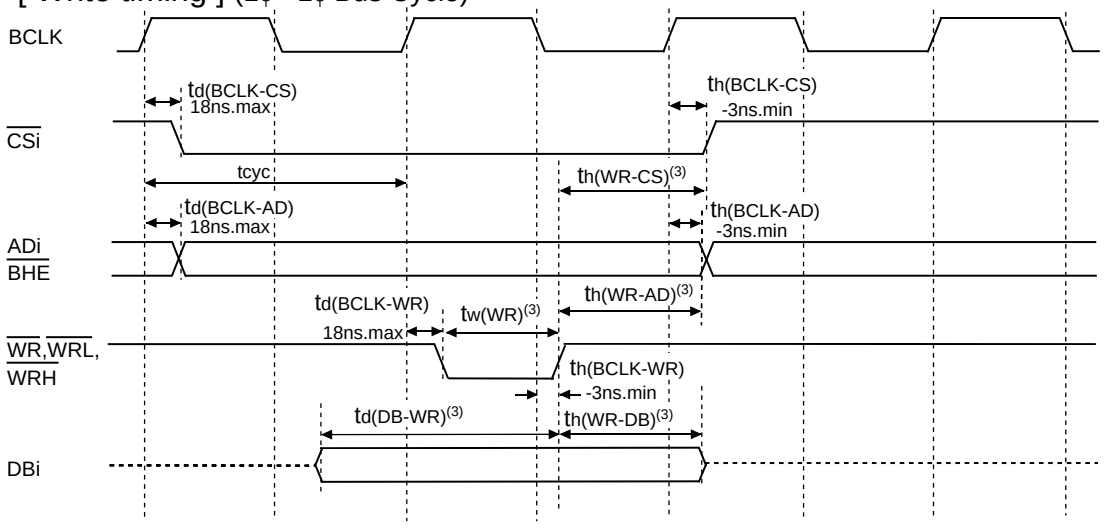
NOTES:

1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency:

   $t_{ac1(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aϕ + bϕ, m=(b x 2)+1)

   $t_{ac1(AD-DB)}$=(tcyc x n-35)ns.max (if external bus cycle is aϕ + bϕ, n=a+b)

[Write timing] (1ϕ +1ϕ Bus Cycle)



NOTES:

3. Varies with operation frequency:
   $t_{d(DB-WR)}$=(tcyc x m-20)ns.min
   (if external bus cycle is aϕ+bϕ, m=b)
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2 x n-15)ns.min
   (if external bus cycle is aϕ+bϕ , n=(bx2)+1)

Measurement Conditions:

- V_{CC1}=V_{CC2}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

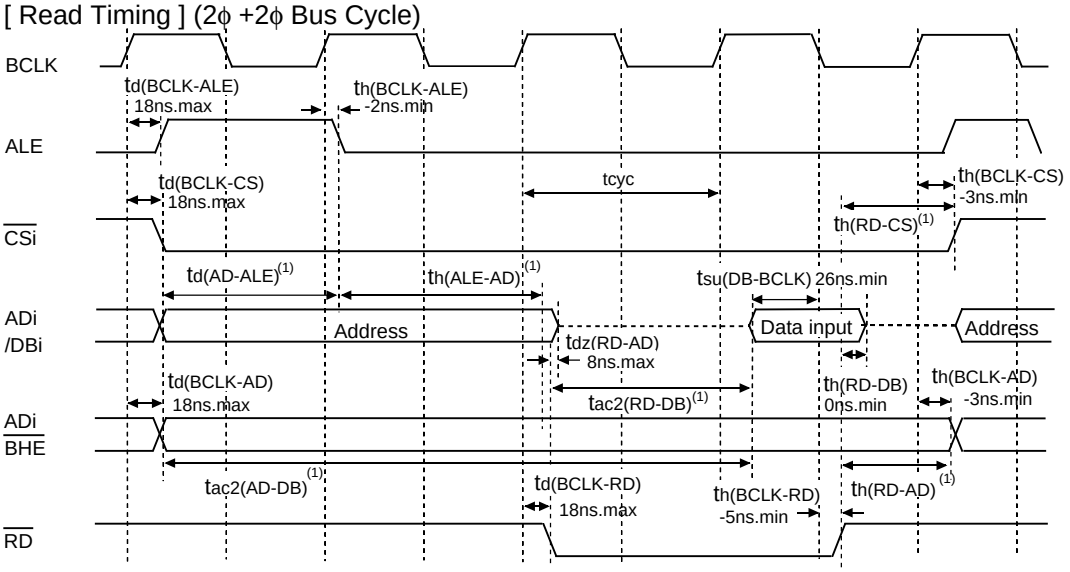
Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (1)

Vcc1=Vcc2=5V

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space with the multiplexed bus)

[Read Timing] (2ϕ +2ϕ Bus Cycle)



NOTES:

1. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n-20)ns.min (if external bus cycle is aϕ + bϕ, n=a)

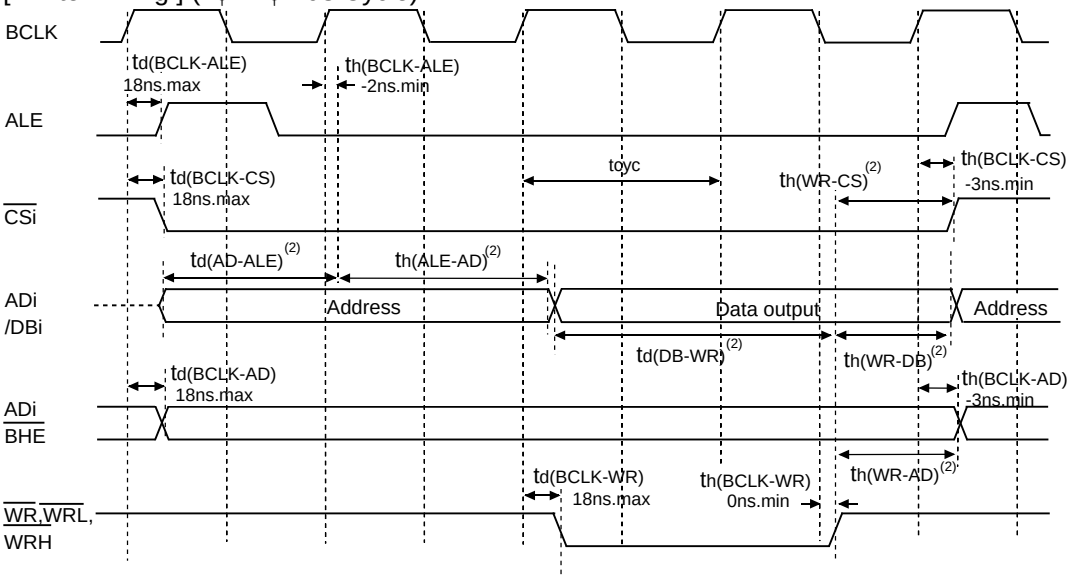
$t_{h(ALE-AD)}$=(tcyc x n-10)ns.min (if external bus cycle is aϕ + bϕ, n=a)

$t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min

$t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aϕ + bϕ, m=(b x 2)+1)

$t_{ac2(AD-DB)}$=(tcyc/2 x p-35)ns.max (if external bus cycle is aϕ + bϕ, p={(a+b-1) x 2}-1)

[Write Timing] (2ϕ +2ϕ Bus Cycle)



NOTES:

2. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n - 20)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

$t_{h(ALE-AD)}$=(tcyc x n -10)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

$t_{h(WR-AD)}$=(tcyc/2-10)ns.min,

$t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-10)ns.min

$t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min

(if external bus cycle is aϕ + bϕ, m=(b x 2)+1)

Measurement Conditions:

- V_{CC1}=V_{CC2}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 5.4 V_{CC1}=V_{CC2}=5V Timing Diagram (2)

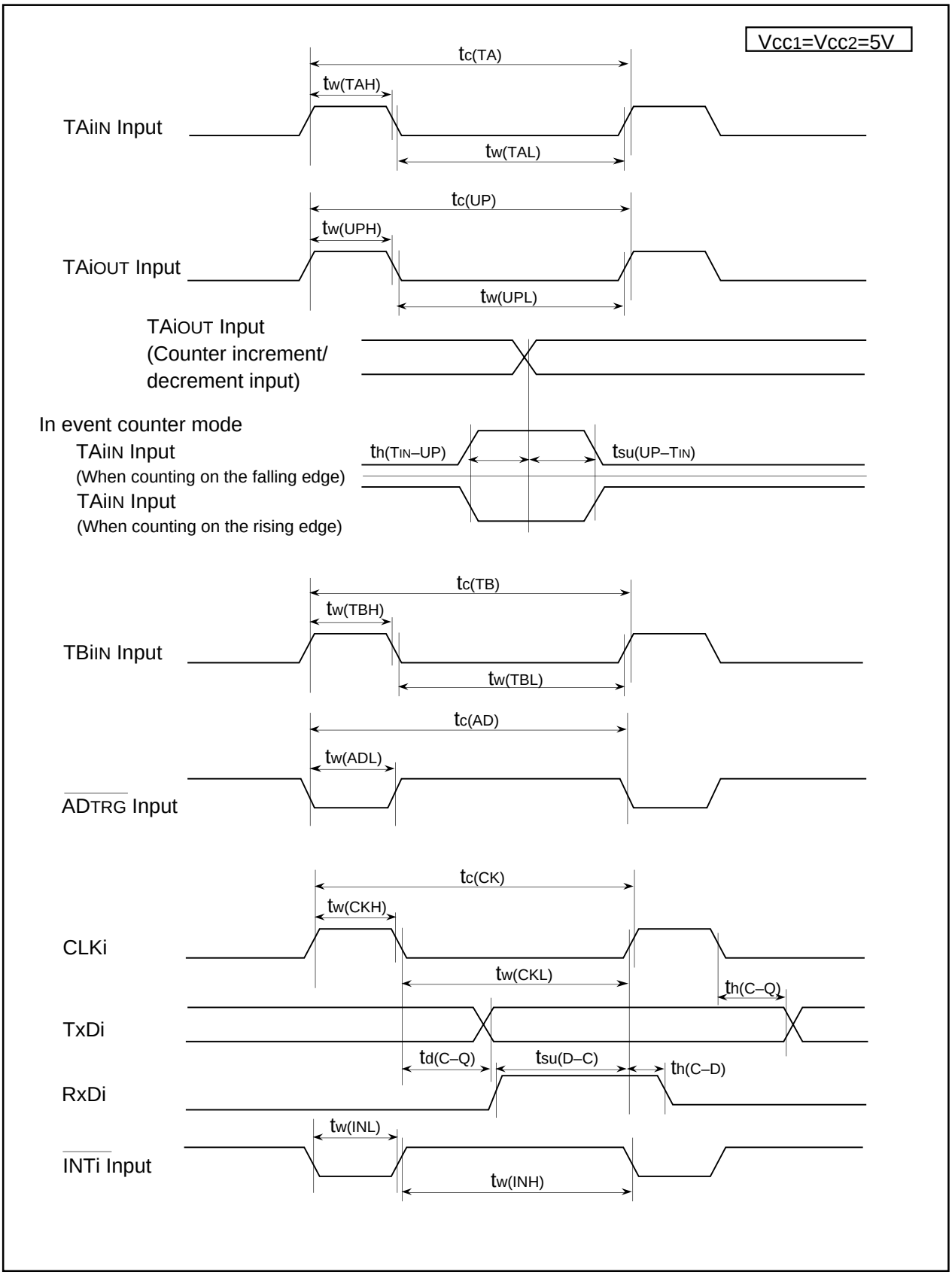


Figure 5.5 Vcc1=Vcc2=5V Timing Diagram (3)

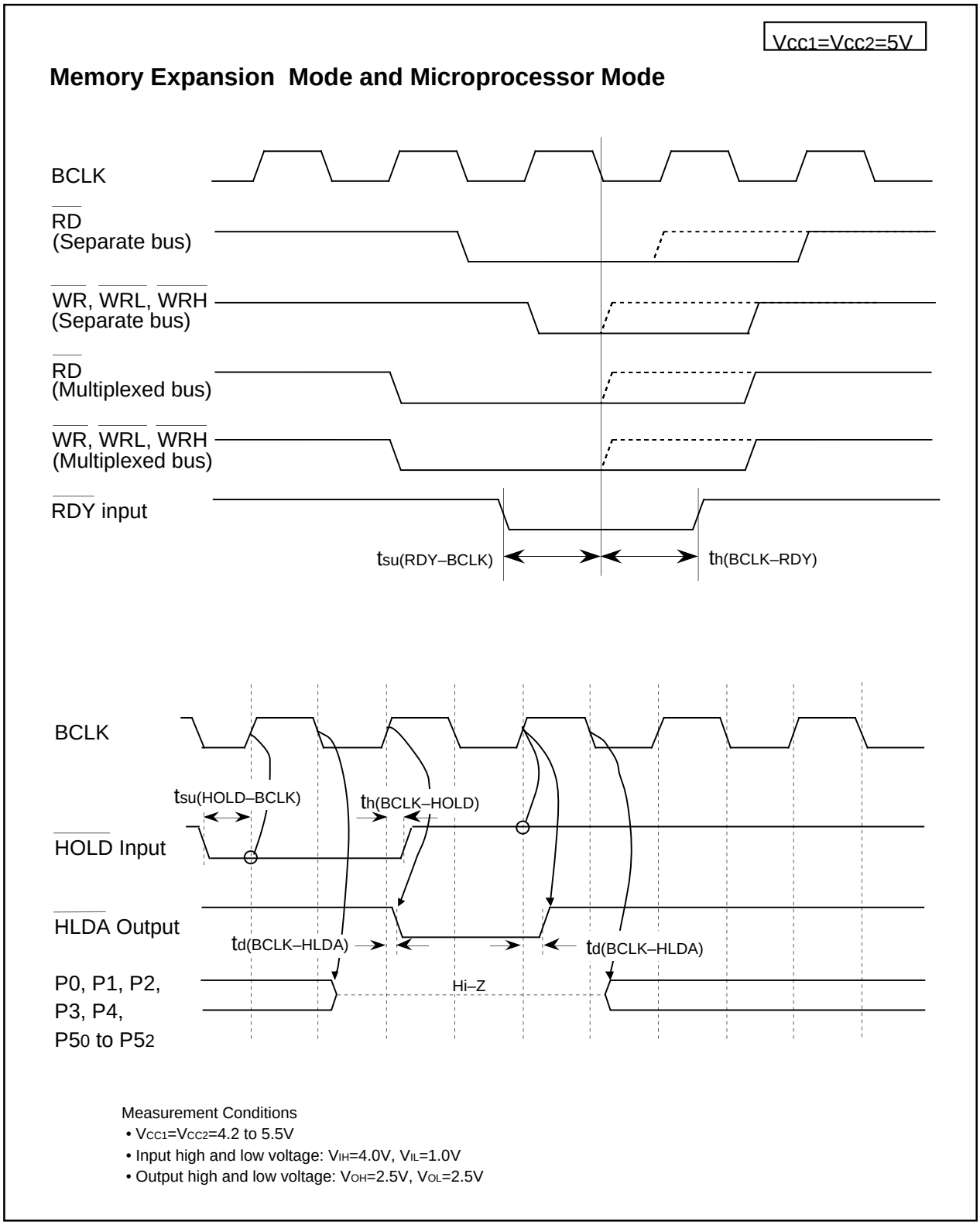


Figure 5.6 Vcc1=Vcc2=5V Timing Diagram (4)

$V_{CC1}=V_{CC2}=3.3V$

Table 5.24 Electrical Characteristics

($V_{CC1}=V_{CC2}$=3.0 to 3.6V, V_{SS}=0V at Topr = –20 to 85°C, f(X_{IN})=24MHz unless otherwise specified)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$	I_{OH}=-1mA		2.7		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)			2.7		V_{CC1}	V
		X_{OUT}	I_{OH}=-0.1mA		2.7		V_{CC1}	V
		X_{COUT} High Power	No load applied			2.5		V
		X_{COUT} Low Power	No load applied			1.6		V
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=1mA				0.5	V
		X_{OUT}	I_{OL}=0.1mA				0.5	V
		X_{COUT} High Power	No load applied			0		V
		X_{COUT} Low Power	No load applied			0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0$_{IN}$-TA4$_{IN}$, TB0$_{IN}$-TB5$_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, TA0$_{OUT}$-TA4$_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4			0.2		1.0	V
		$\overline{RESET}$			0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=3V				4.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V				-4.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_I=0V	Flash Memory	66	120	500	kΩ
				Masked ROM	40	70	500	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}				3.0		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}				20.0		MΩ
V_{RAM}	RAM Standby Voltage	in stop mode			2.0			V
I_{CC}	Power Supply Current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(X_{IN})=24 MHz, square wave, no division			22	35	mA
			f(X_{CIN})=32 kHz, in wait mode, Topr=25° C			10		µA
			Topr=25° C when the clock stops			0.8	5	µA
			Topr=85° C when the clock stops				50	µA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=3.3V$

Table 5.25 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}$= 3.0 to 3.6V, $V_{SS}=AV_{SS}$=0V at Topr = –20 to 85°C, f(X_{IN}) = 24MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
-	Resolution		$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	No S&H function (8-bit)	$V_{CC1}=V_{CC2}=V_{REF}$=3.3V			±2	LSB
DNL	Differential Nonlinearity Error	No S&H function (8-bit)				±1	LSB
-	Offset Error	No S&H function (8-bit)				±2	LSB
-	Gain Error	No S&H function (8-bit)				±2	LSB
R_{LADDER}	Resistor Ladder		$V_{REF}=V_{CC1}$	8		40	kΩ
t_{CONV}	8-bit Conversion Time(1, 2)			6.1			µs
V_{REF}	Reference Voltage			3.0		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

S&H: Sample and Hold

NOTES:
1. Divide f(X_{IN}), if exceeding 10 MHz, to keep ϕAD frequency at 10 MHz or less.
2. S&H function not available.

Table 5.26 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}$=3.0 to 3.6V, $V_{SS}=AV_{SS}$=0V at Topr = –20 to 85°C, f(X_{IN}) = 24MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.0	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.27 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	41		ns
$t_{w(H)}$	External Clock Input High ("H") Width	18		ns
$t_{w(L)}$	External Clock Input Low ("L") Width	18		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.28 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	30		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	40		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	60		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequecncy and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m= (b x 2)+1)

$$t_{ac1(AD-DB)} = \frac{10^9}{f_{(BCLK)}} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, n= a+b)

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)}} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, p={(a+b-1) x 2})

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS}= 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.29 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	40		ns

Table 5.30 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	200		ns

Table 5.31 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.32 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.33 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.34 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on both edges)	80		ns

Table 5.35 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Wdth	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.36 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.37 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for re-trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Width	125		ns

Table 5.38 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.39 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

$V_{CC1}=V_{CC2}=3.3V$

Switching Characteristics

($V_{CC1}=V_{CC2}$=3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.40 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi, \text{ m=b)}$$

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi, \text{ n=(b x 2)-1)}$$

$V_{CC1}=V_{CC2}=3.3V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.41 Memory Expansion Mode and Microprocessor Mode (when accessing an external memory space with the multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		(Note 1)		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-AD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time (BCLK standard)		-2		ns
$t_{d(AD-ALE)}$	ALE Signal Output Delay Time (address standard)		(Note 3)		ns
$t_{h(ALE-AD)}$	ALE Signal Output Hold Time (address standard)		(Note 4)		ns
$t_{dz(RD-AD)}$	Address Output Float Start Time			8	ns

NOTES:

1. Values can be obtained by the following equations, according to BLCK frequency.

$$t_{h(RD-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(RD-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

2. Values can be obtained by the following equations, according to BLCK frequency and external bus cycles.

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [ns] \text{ (if external bus cycle is } a\phi + b\phi, \text{ m=(b+2)-1)}$$

3. Values can be obtained by the following equations, according to BLCK frequency and external bus cycles.

$$t_{d(AD-ALE)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 20 \quad [ns] \text{ (if external bus cycle is } a\phi + b\phi, \text{ n=a)}$$

4. Values can be obtained by the following equations, according to BLCK frequency and external bus cycles.

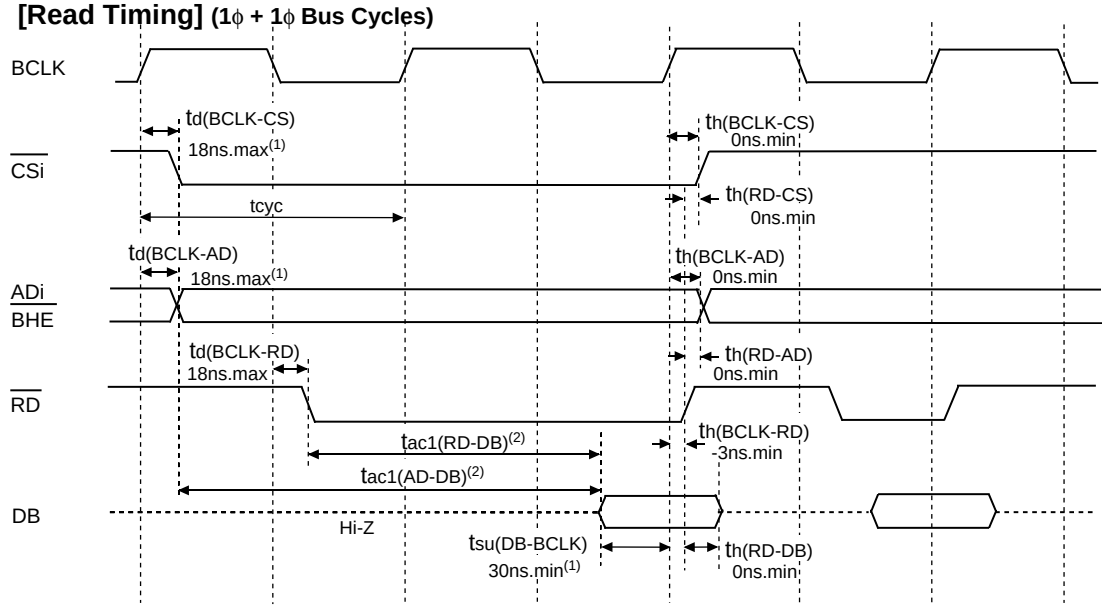
$$t_{h(ALE-AD)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 10 \quad [ns] \text{ (if external bus cycle is } a\phi + b\phi, \text{ n=a)}$$

Vcc1=Vcc2=3.3V

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space)

[Read Timing] (1φ + 1φ Bus Cycles)



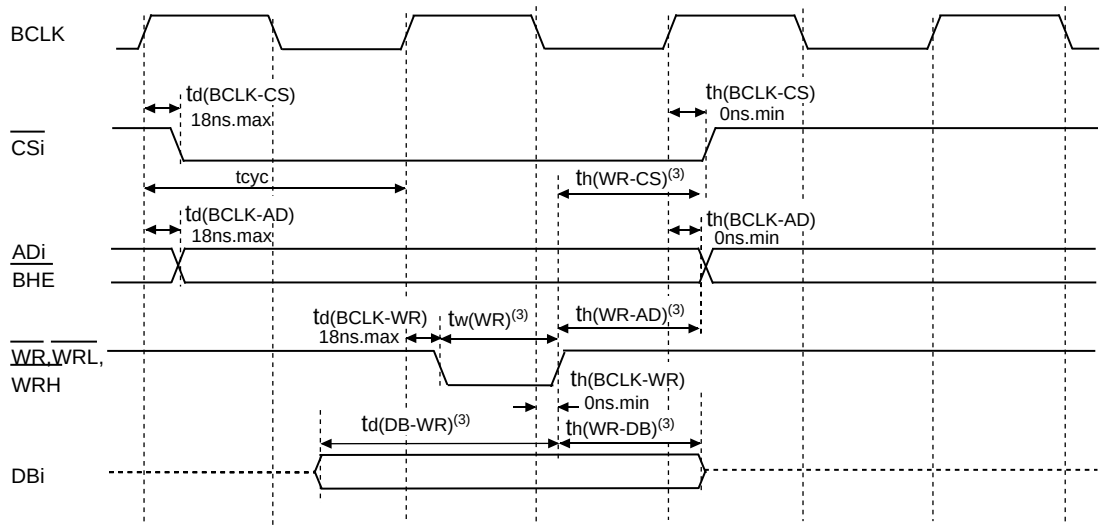
NOTES:

1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency.

   $t_{ac1(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aφ + bφ, m=(b x 2) + 1)

   $t_{ac1(AD-DB)}$=(tcyc x n-35)ns.max (if external bus cycle is aφ + bφ, n = a + b)

[Write Timing] (1φ + 1φ Bus Cycles)



NOTES:

3. Varies with operation frequency.

   $t_{d(DB-WR)}$=(tcyc x m-20)ns.min

   (if external bus cycle is aφ + bφ, m=b)

   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min

   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min

   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min

   $t_{w(WR)}$=(tcyc/2 x n-15)ns.min

   (if external bus cycle is aφ + bφ, n=(bx2)+1)

Measurement Conditions

- V_{CC1}=V_{CC2}=3.0 to 3.6V
- Input high and low voltage: V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

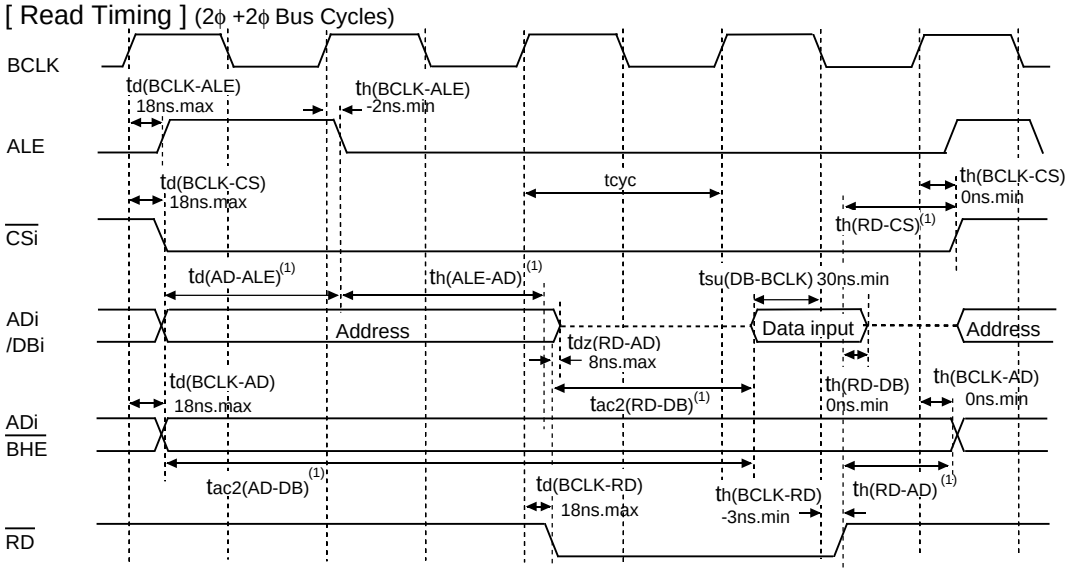
Figure 5.7 V_{CC1}=V_{CC2}=3.3V Timing Diagram (1)

Vcc1=Vcc2=3.3V

Memory Expansion Mode and Microprocessor Mode

(when accessing external memory space and using the multiplexed bus)

[Read Timing] (2ϕ +2ϕ Bus Cycles)



NOTES:

1. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n-20)ns.min (if external bus cycle is aϕ + bϕ, n=a)

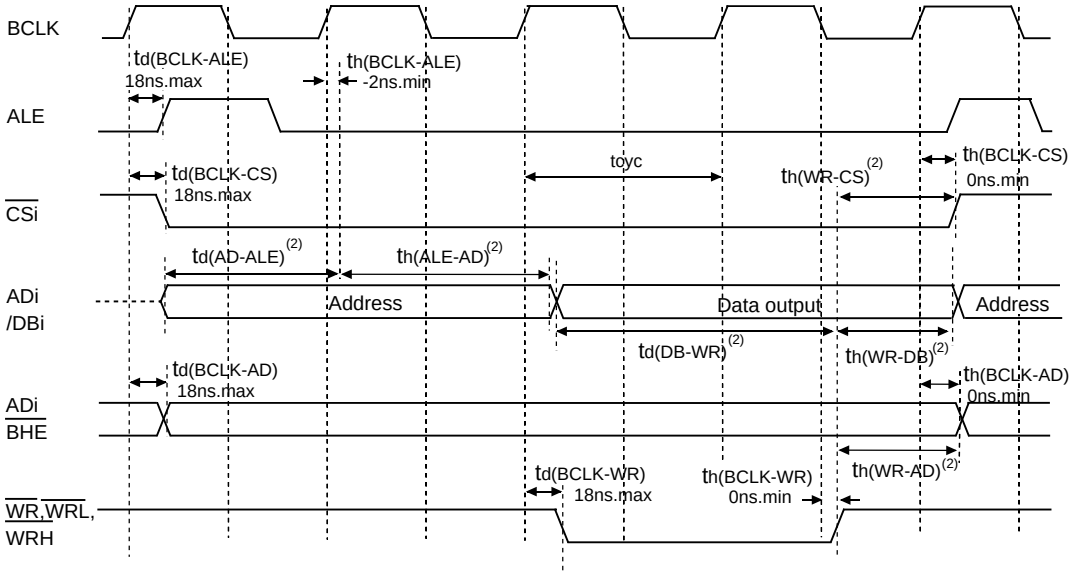
$t_{h(ALE-AD)}$=(tcyc x n-10)ns.min (if external bus cycle is aϕ + bϕ, n=a)

$t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min

$t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aϕ + bϕ, m=(b x 2)+1)

$t_{ac2(AD-DB)}$=(tcyc/2 x p-35)ns.max (if external bus cycle is aϕ + bϕ, p={(a+b-1) x 2}-1)

[Write Timing] (2ϕ +2ϕ Bus Cycles)



NOTES:

2. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n - 20)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

$t_{h(ALE-AD)}$=(tcyc x n -10)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

$t_{h(WR-AD)}$=(tcyc/2-10)ns.min,

$t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-10)ns.min

$t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min

(if external bus cycle is aϕ + bϕ, m=(b x 2)+1)

Measurement Conditions:

- V_{CC1}=V_{CC2}=3.0 to 3.6V
- Input high and low voltage:
  V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
  V_{OH}=1.5V, V_{OL}=1.5V

Figure 5.8 V_{CC1}=V_{CC2}=3.3V Timing Diagram (2)

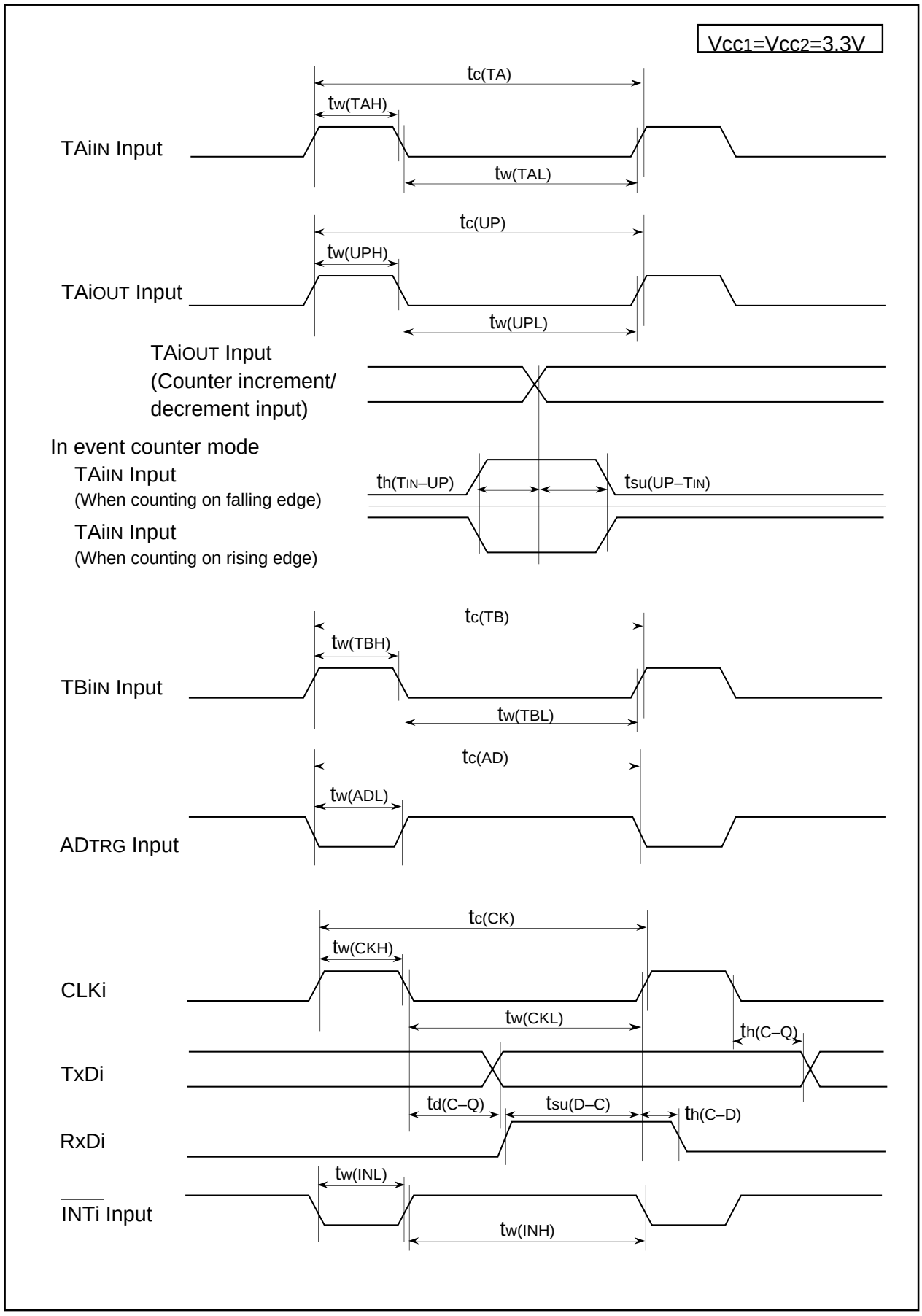


Figure 5.9 Vcc1=Vcc2=3.3V Timing Diagram (3)

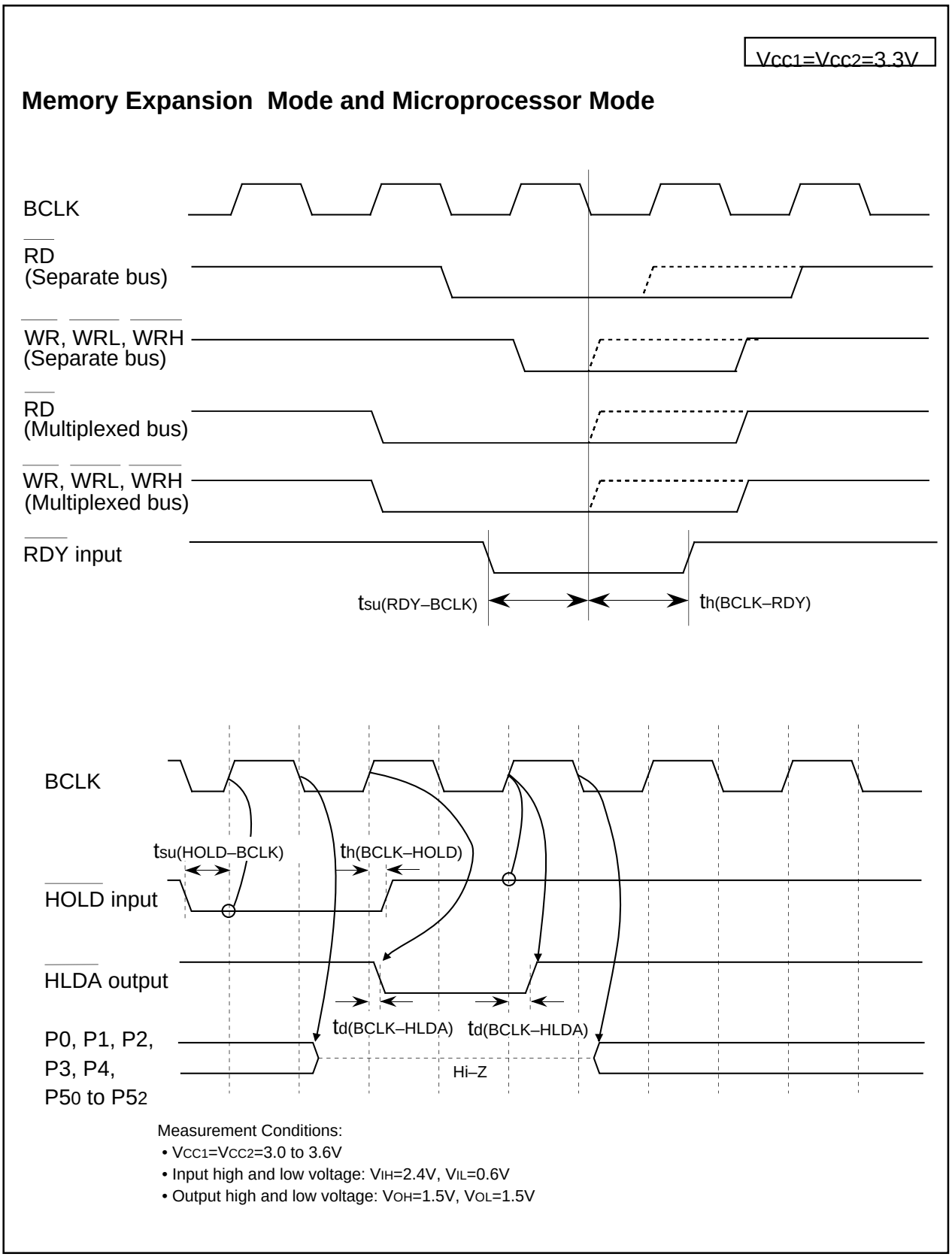


Figure 5.10 Vcc1=Vcc2=3.3V Timing Diagram (4)

5.2 Electrical Characteristics (M32C/85T)

Table 5.42 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V_{CC1}, V_{CC2}	Supply Voltage		V_{CC1}=V_{CC2}=AVcc	-0.3 to 6.0	V
AVcc	Analog Supply Voltage		V_{CC1}=V_{CC2}=AVcc	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNVss, BYTE, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), V_{REF}, X_{IN}		-0.3 to V_{CC1}+0.3	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(1)		-0.3 to V_{CC2}+0.3	
		$P7_0$, $P7_1$		-0.3 to 6.0	
V_O	Output Voltage	$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{OUT}		-0.3 to V_{CC1}+0.3	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(1)		-0.3 to V_{CC2}+0.3	
Pd	Power Dissipation		Topr=25° C	500	mW
Topr	Operating Ambient Temperature	during CPU operation	T version	-40 to 85	° C
		during flash memory program and erase operation		0 to 60	
Tstg	Storage Temperature			-65 to 150	° C

NOTES:
1. P11 to P15 are provided in the 144-pin package only.

Table 5.43 Recommended Operating Conditions

(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr= -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply Voltage (V_{CC1}=V_{CC2})	4.2	5.0	5.5	V
AV_{CC}	Analog Supply Voltage		V_{CC1}		V
V_{SS}	Supply Voltage		0		V
AV_{SS}	Analog Supply Voltage		0		V

Table 5.43 Recommended Operating Conditions (Continued)

(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter	Accommodating Pins	Standard			Unit
			Min.	Typ.	Max.	
V_{IH}	Input High ("H") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0.8V_{CC2}		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0.8V_{CC1}		V_{CC1}	
		$P7_0$, $P7_1$	0.8V_{CC1}		6.0	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$	0.8V_{CC2}		V_{CC2}	V
V_{IL}	Input Low ("L") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0		0.2V_{CC2}	V
		$P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE			0.2V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$	0		0.2V_{CC2}	V
$I_{OH(peak)}$	Peak Output High ("H") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			5.0	mA

NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, and P11 must be -40mA or less.
   Total $I_{OH(peak)}$ for $P8_6$, $P8_7$, P9, P10, P14 and P15 must be -40mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P12 and P13 must be -40mA or less.
   Total $I_{OH(peak)}$ for P6, P7, and $P8_0$ to $P8_4$ must be -40mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply when $P8_7$ is used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

Table 5.43 Recommended Operating Conditions (Continued)

(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f(X_{IN})$	Main Clock Input Frequency	V_{CC1}=4.2 to 5.5V	0		32	MHz
$f(X_{CIN})$	Sub Clock Frequency			32.768	50	kHz
$f(_{Ring})$	On-chip Oscillator Frequency			1		MHz
$f(_{PLL})$	PLL Clock Frequency	V_{CC1}=4.2 to 5.5V	10		32	MHz
$t_{SU(PLL)}$	PLL Lock Time	V_{CC1}=5.0V			5	ms

$V_{CC1}=V_{CC2}=5V$

Table 5.44 Electrical Characteristics

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr = -40 to 85°C (T version), $f(X_{IN})=32MHz$ unless otherwise specified)

Symbol	Parameter			Measurement Condition		Standard			Unit
						Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$		I_{OH}=-5mA		3.0		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OH}=-5mA		3.0		V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$		I_{OH}=-200µA		4.7		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$,$P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OH}=-200µA		4.7		V_{CC1}	
		X_{OUT}		I_{OH}=-1mA		3.0			V
		X_{COUT}	High Power	No load applied			2.5		V
			Low Power	No load applied			1.6		
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OL}=5mA				2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		I_{OL}=200µA				0.45	V
		X_{OUT}		I_{OL}=1mA				2.0	V
		X_{COUT}	High Power	No load applied			0		V
			Low Power	No load applied			0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{AD_{TRG}}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4				0.2		1.0	V
		$\overline{RESET}$				0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		V_I=5V				5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		V_I=0V				-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)		V_I=0V	Flash Memory	30	50	167	kΩ
					Masked ROM	20	40	167	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}					1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}					10		MΩ
V_{RAM}	RAM Standby Voltage	in stop mode				2.0			V
I_{CC}	Power Supply Current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	$f(X_{IN})$=32 MHz, square wave, no division				28	50	mA
			$f(X_{CIN})$=32 kHz, in wait mode, Topr=25° C				10		µA
			Topr=25° C (while clock is stopped)				0.8	5	µA
			Topr=85° C (while clock is stopped)					50	µA

NOTES:
1. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=5V$

Table 5.45 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at Topr= -40 to 85°C (T version), $f(X_{IN})=32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, AN_{EX0}, AN_{EX1}			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8.00		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2.00		V_{CC1}	V
V_{IA}	Analog Input Voltage			0.00		V_{REF}	V

NOTES:
1. Divide $f(X_{IN})$, if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. Sample and Hold function is available.

Table 5.46 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at Topr= -40 to 85°C (T version), $f(X_{IN})=32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Table 5.47 Flash Memory Version Electrical Characteristics(1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and Erase Endurance(3)		100			cycles
-	Word Program Time (V_{CC1}=5.0V,Topr=25° C)			25	200	µs
-	Lock Bit Program Time			25	200	µs
-	Block Erase Time (V_{CC1}=5.0V,Topr=25° C)	4-Kbyte Block		0.3	4	s
		8-Kbyte Block		0.3	4	s
		32-Kbyte Block		0.5	4	s
		64-Kbyte Block		0.8	4	s
-	All-Unlocked-Block Erase Time(2)				4 x *n*	s
t_{PS}	Flash Memory Circuit Stabilization Wait Time				15	µs
-	Data Hold Time(4)		10			years

NOTES:
1. Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at Topr = 0 to 60 ° C unless otherwise specified.
2. n denotes the number of block to be erased.
3. Number of program-erase cycles per block.
   If Program and Erase Endurance is *n* cycle (*n*=100), each block can be erased and programmed *n* cycles.
   For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (Rewrite prohibited).
4. Topr = -40 to 85 ° C

$V_{CC1}=V_{CC2}=5V$

Table 5.48 Power Supply Timing

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time for Stable Internal Supply Voltage when Power-on	V_{CC1}=3.0 to 5.5V			2	ms

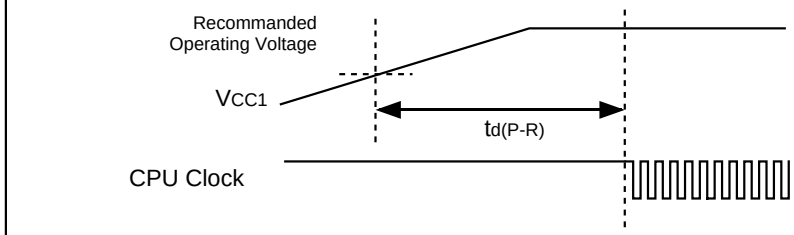
td(P-R) Wait Time for Stable Internal Supply Voltage when Power-on	

Figure 5.11 Power Supply Timing Diagram

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version) unless otherwise specified)

Table 5.49 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$tw_{(H)}$	External Clock Input High ("H") Width	13.75		ns
$tw_{(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version) unless otherwise specified)

Table 5.50 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	40		ns

Table 5.51 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	200		ns

Table 5.52 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.53 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.54 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version) unless otherwise specified)

Table 5.55 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on both edges)	80		ns

Table 5.56 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.57 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.58 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for re-trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Pulse Width	125		ns

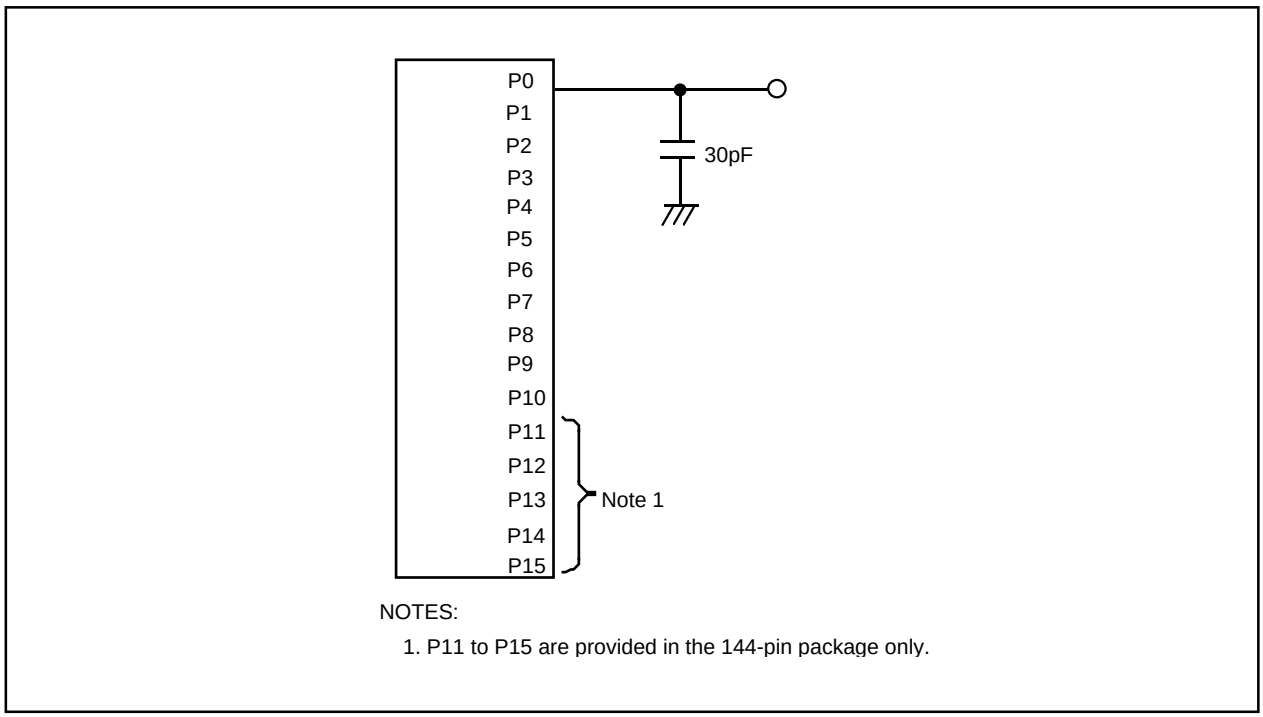
Table 5.59 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.60 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

$V_{CC1}=V_{CC2}=5V$



NOTES:
1. P11 to P15 are provided in the 144-pin package only.

Figure 5.12 P0 to P15 Measurement Circuit

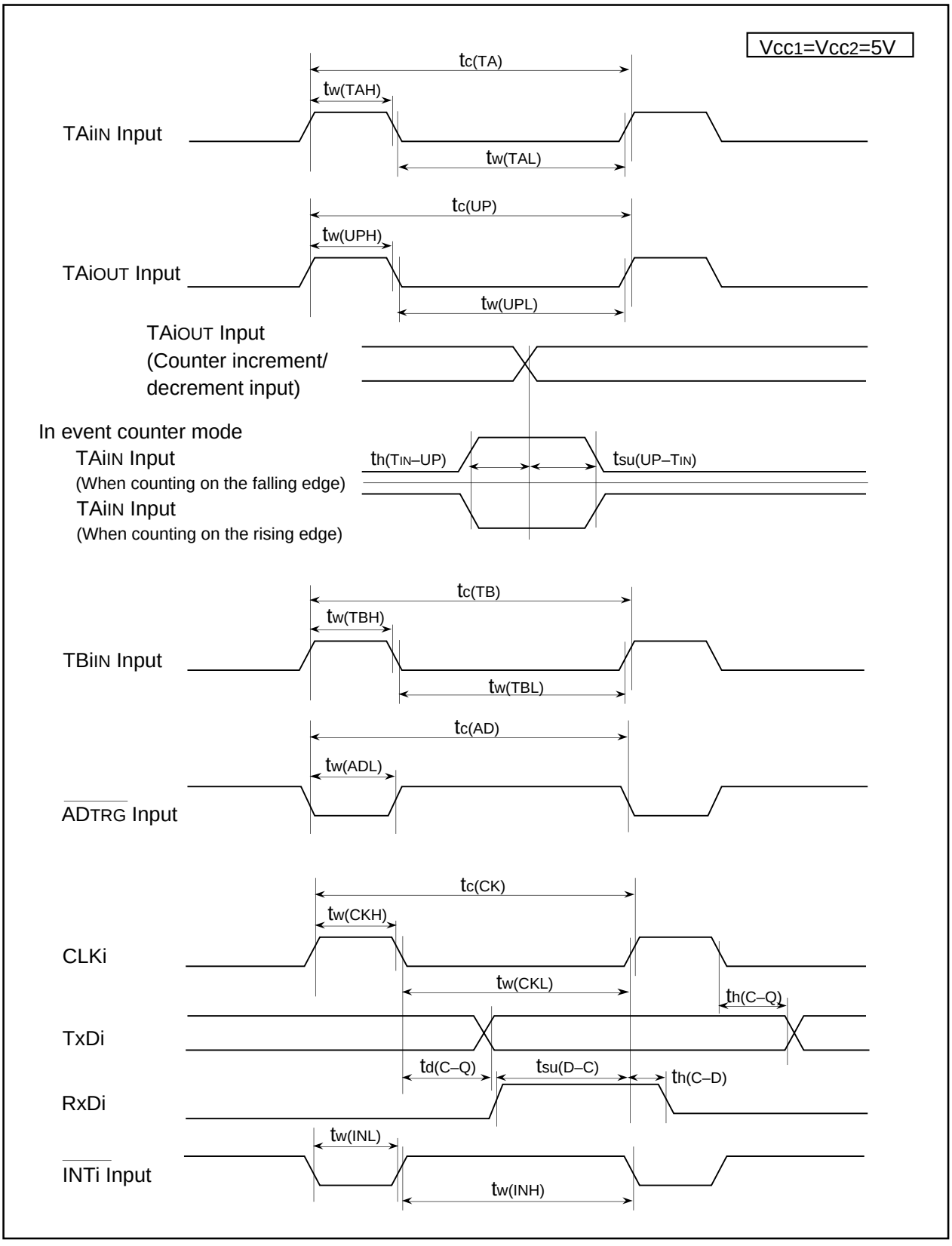


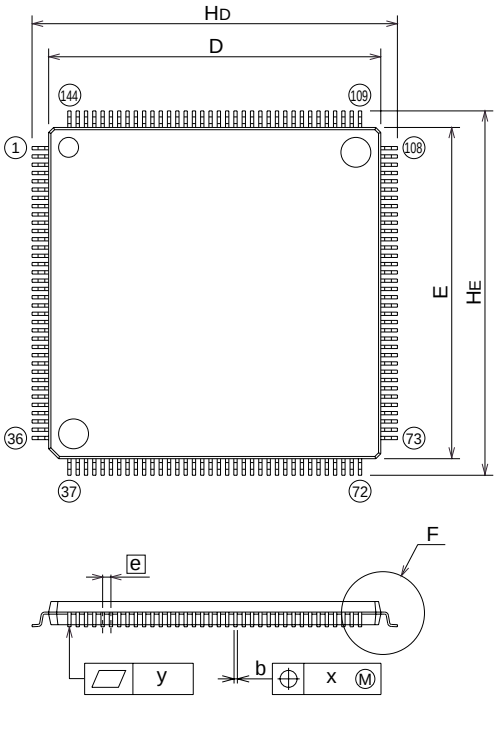
Figure 5.13 Vcc1=Vcc2=5V Timing Diagram

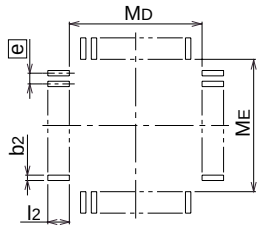
Package Dimensions

144P6Q-A Recommended

Plastic 144pin 20×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP144-P-2020-0.50	–	1.23	Cu Alloy





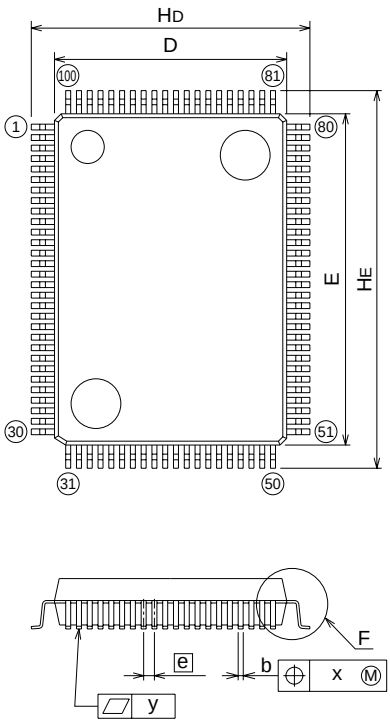
Recommended Mount Pad

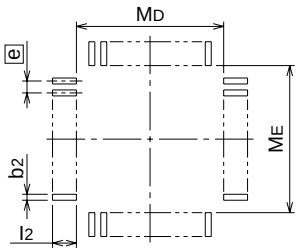
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0.05	0.125	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	–	0.5	–
HD	21.8	22.0	22.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
l2	0.95	–	–
MD	–	20.4	–
ME	–	20.4	–

100P6S-A Recommended

Plastic 100pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	–	1.58	Alloy 42





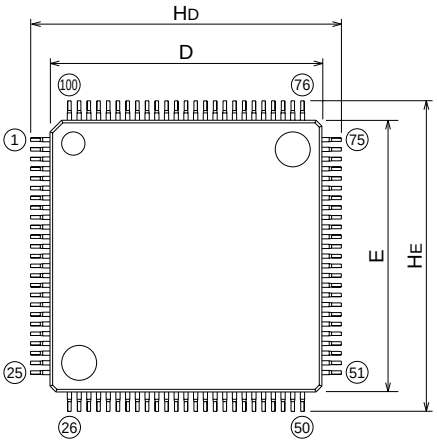
Recommended Mount Pad

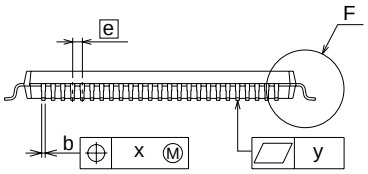
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	–	1.4	–
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b2	–	0.35	–
l2	1.3	–	–
MD	–	14.6	–
ME	–	20.6	–

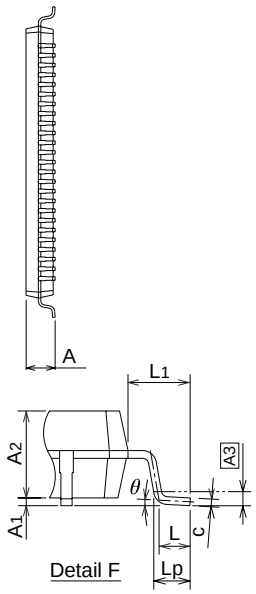
100P6Q-A Recommended

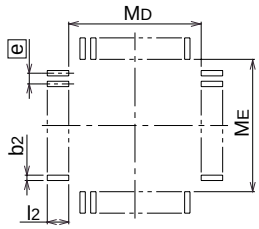
Plastic 100pin 14×14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	–	0.63	Cu Alloy









Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	14.4	–
ME	–	14.4	–

REVISION HISTORY	M32C/85 Group (M32C/85, M32C/85T) Data Sheet

Rev.	Date	Description	
		Page	Summary
0.30	Jul. 18, 2003	–	New Document
0.40	Sep. 30, 2003		**Overview**
		2 to 3	• **Tables 1.1 and 1.2 M32C/85 Performance** "Oscillator Stop Detect Function" added
		5	• **Figure 1.2 ROM/RAM Capacity** and **Table 1.3. M32C/85 Group** M30852ME-XXXGP and M30850ME-XXXGP/FP deleted
		6	• ROM capacity "192 Kbytes" deleted
		7, 11, 12	• **Figures 1.4** to **1.6 Pin Assignments** Note 2 added
		10,14	- V_{REF} pin changed from analog input pins to control pins.
		16 to 18	- SDA0 to SDA4 pins changed from output pins to I/O pins.
		17	- $TA4_{OUT}$ changed from input pin to I/O pin.
			- $TA4_{IN}$ pin changed from output pin to input pin.
			- ISRxD1 pin modified to ISRxD0 pin in port P8.
		18	- DA0 and DA1 pins changed from input pins to output pins.
		19	- Symbol "$P11_7$" modified to "$P11_4$" and description from "8-bit" to "5-bit".
			- Descriptions of ISTxD1 and $BE1_{IN}$ modified from "received data" to "transmit data".
			SFR
		44,45	- Notes written directly in the Tables.
0.50	Feb. 05, 2004		**Overview**
		2, 3	• **Tables 1.1 and 1.2 M32C/85 Performance** "Shortest Instruction Execution Time" and "Power Comsumption" values modified
			Memory
		23	• **Figure 3.1 Memory Map** Diagram modified
			SFR
		24	• "After RESET" values of PM 1, PM 2, D4INT, G0IRF, G1IRF, IDB0 to IDB1, TA0MR to TA4MR, TCSPR, DM0SL to DM3SL registers corrected
			• NOTES added to PM0 and TCSPR registers
			Electrical Characteristics
			• Newly added
0.51	Feb. 09, 2004		**Electrical Characteristics**
		52	• **Table 5.6 Flash Memory Version Electrical Characteristics** Note 4 changed
		59	• **Figure 5.2 Vcc1=Vcc2=5V Timing Diagram (1)** Notes 1 and 2 changed
		60	• **Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (2)** Notes 1, 2, and 3 changed
		70	• **Figure 5.6 Vcc1=Vcc2=3.3V Timing Diagram (1)** Notes 1, 2, and 3 changed
		71	• **Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (2)** Notes 1 and 2 changed
0.52	Mar. 12, 2004		**Overview**
		2, 3	• **Table 1.1 and 1.2 M32C/85 Group Performance** Value of Power Consumption modified

Rev.	Date	Description	
		Page	Summary
			Electrical Characteristics
		50	• **Table 5.3 Electrical Characteristics** Maximum values for Power Supply Current modified
		52	• **Table 5.6 Flash Memory Version Electrical Characteristics** Note 1. 100-cycle Products (D3, D5, U3, U5) deleted; Note 4 modified
			• **Table 5.7 Flash Memory Version Program and Erase Voltage and Read Operation Voltage Characteristics (at Topr=0 to 60°C)** deleted
		63	• **Table 5.22 Electrical Characteristics** Maximum values for Power Supply Consumption modified and standard values when "Topr=85°C while clock is stopped" deleted
1.00	Jun. 01, 2004	-	**M32C/85T (High-reliability version)** added
		All Pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
			Overview
		1	• **1.1 Applications** Automobiles added
		2, 3	• **Table 1.1** and **Table 1.2 M32C/85 Group (M32C/85, M32C/85T) Performance** M32C/85T added; note 3 added
		4	• **Figure 1.1 M32C/85 Group (M32C/85, M32C/85T) Block Diagram** Note 3 added
		5	• **1.4 Product Information** Description modified
			• **Figure 1.2 ROM/RAM Capacity** figure modified
		5, 6	• **Table 1.3 M32C/85 Group** M32C/85T added
		6	• **Figure 1.3 Product Numbering System** M32C/85T added
		7	• **Figure 1.4 Pin Assignment for 144-Pin Package** Note 3 added
		12	• **Figure 1.6 Pin Assignment for 100-Pin Pacakage** Note 5 added
		8 to 10	• **Table 1.5 Pin Characteristics for 144-Pin Package** Note 1 added
		13, 14	• **Table 1.6 Pin Characteristics for 100-Pin Package** Note 1 added
		15 to 18	• **Table 1.7 Pin Description** Notes added
			Memory
		22	• **Figure 3.1 Memory Map** Tables of internal ROM/internal RAM modified; note 2 modified; notes 4 and 5 added
			SFR
		23	• Note 2 added
		24	• PWCR0 and PWCR1 registers deleted
			• "Values after RESET" of the masked ROM version added to the FMR0 register
			• Note 1 added
			Electrical Characteristics
		46	• **Table 5.2 Recommended Operating Conditions** $f_{(ripple)}$, $V_{p-p(ripple)}$, V_{CC}, SV_{CC} and note 1 deleted
		47	• **Table 5.3 Electrical Characteristics** R_{PULLUP} value for the masked ROM version added

Rev.	Date	Description	
		Page	Summary
		49	• **Table 5.3 Electrical Characteristics** Maximum ICC value modified
		50	• **Table 5.4 A/D Conversion Characteristics** tSMP value modified; note 1 added
		52	• **Table 5.7 Low Voltage Detect Circuit Electrical Characteristics** added
			• **Table 5.8 Power Supply Timing** added
			• **Figure 5.1 Power Supply Timing Diagram** added
		57	• **Table 5.23 Memory Expassion Mode and Microprocessor Mode** th(BCLK-ALE) value modified
		63	• **Table 5.24 Electrical Characteristics** Maximum ICC value modified
		61	• **Table 5.24 Electrical Characteristics** RPULLUP value for the masked ROM version added
		64	• **Table 5.25 A/D Conversion Characteristics** tCONV value modified
		65	• **Table 5.28 Memory Expassion Mode and Microprocessor Mode** tsu(DB-BCLK), tsu(RDY-BCLK) and tsu(HOLD-BCLK) value modified
		68	• **Table 5.40 Memory Expassion Mode and Microprocessor Mode** equetion of th(WR-DB) modified
		69	• **Table 5.41 Memory Expassion Mode and Microprocessor Mode** th(BCLK-ALE) value modified; equetion of th(WR-DB) modified
		74	• **5.2 Electrical Characteristics (M32C/85T)** added
1.10	Jun.28, 2004	-	**High-reliability version (U version)** deleted
			Overview
		5	• **Table 1.3 M32C/85 Group (1) (2)** development status modified
		6	• **Figure 1.2 Product Numbering System** figure modified

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