# LM5117/Q1 Wide Input Range Synchronous Buck Controller with Analog Current Monitor

## 1 Features

- LM5117-Q1 is Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Emulated Peak Current Mode Control
- Wide Operating Range from 5.5 V to 65 V
- Robust 3.3-A Peak Gate Drives
- Adaptive Dead-Time Output Driver Control
- Free-Run or Synchronizable Clock up to 750 kHz
- Optional Diode Emulation Mode
- Programmable Output from 0.8 V
- Precision 1.5% Voltage Reference
- Analog Current Monitor
- Programmable Current Limit
- Hiccup Mode Overcurrent Protection
- Programmable Soft-Start and Tracking
- Programmable Line Undervoltage Lockout
- Programmable Switchover to External Bias Supply
- Thermal Shutdown

## 2 Applications

- Automotive Infotainment
- Industrial DC-DC Motor Drivers
- Automotive USB Power
- Telecom Server

## 3 Description

The LM5117 is a synchronous buck controller intended for step-down regulator applications from a high voltage or widely varying input supply. The control method is based upon current mode control utilizing an emulated current ramp. Current mode control provides inherent line feed-forward, cycle-by-cycle current limiting and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable control of very small duty cycles necessary in high input voltage applications.

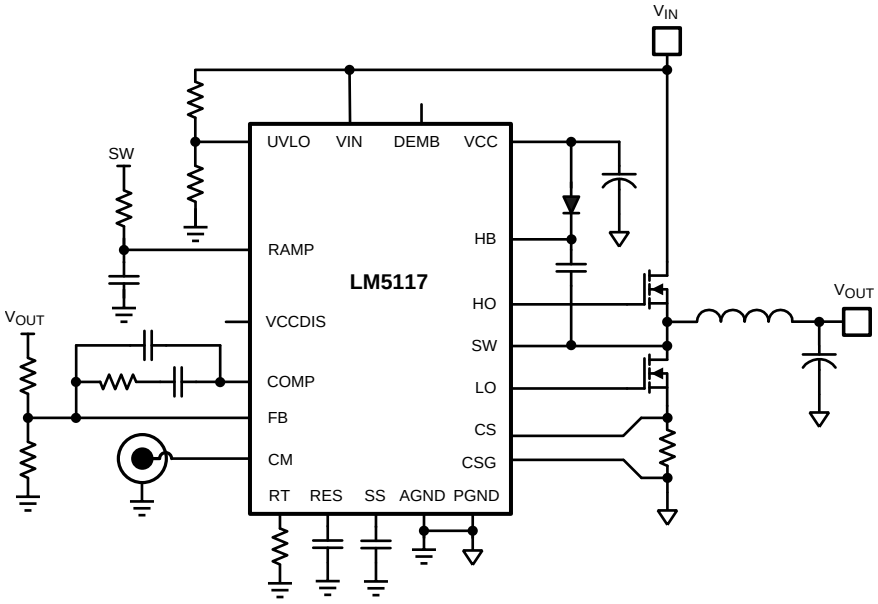
The operating frequency is programmable from 50 kHz to 750 kHz. The LM5117 drives external high-side and low-side NMOS power switches with adaptive dead-time control. A user-selectable diode emulation mode enables discontinuous mode operation for improved efficiency at light load conditions. A high voltage bias regulator that allows external bias supply further improves efficiency. The LM5117's unique analog telemetry feature provides average output current information. Additional features include thermal shutdown, frequency synchronization, hiccup mode current limit, and adjustable line undervoltage lockout.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LM5117 | HTSSOP (20) PWP | 6.50 mm × 4.40 mm |
| LM5117-Q1 | WQFN (24) RTW | 4.00 mm × 4.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Typical Application**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision E (March 2013) to Revision F** — **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, ESD Rating table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support* , and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Changed µH into µF ... 29

**Changes from Revision D (March 2013) to Revision E** — **Page**

- Changed layout of National Data Sheet to TI format ... 34


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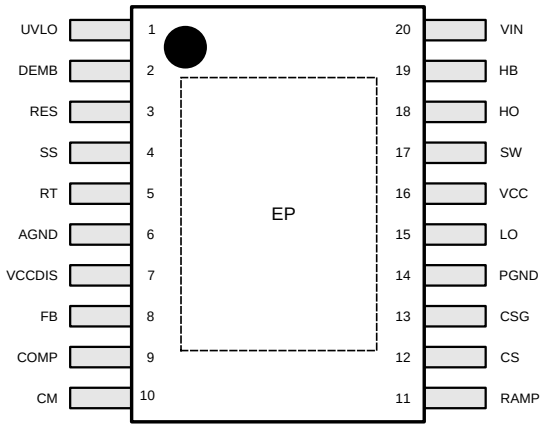
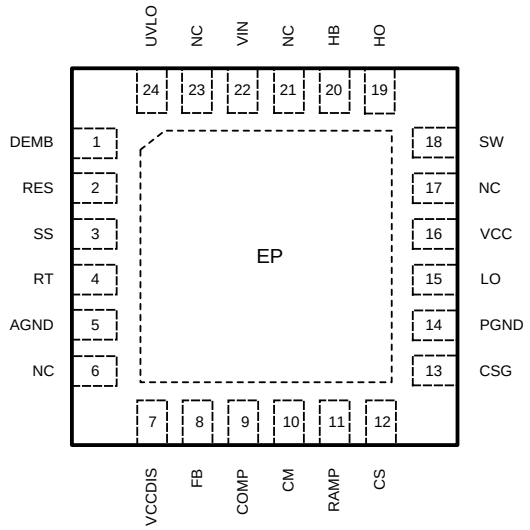
# 5 Pin Configuration and Functions

**PWP Package**
**20-Pin HTSSOP**
**Top View**




**RTW Package**
**24-Pin WQFN**
**Top View**



## Pin Functions

| PIN | | | TYPE (1) | DESCRIPTION |
|---|---|---|---|---|
| HTSSOP | WQFN | NAME | | |
| 1 | 24 | UVLO | I | Undervoltage lockout programming pin. If the UVLO pin voltage is below 0.4 V, the regulator is in the shutdown mode with all functions disabled. If the UVLO pin voltage is greater than 0.4 V and less than 1.25 V, the regulator is in standby mode with the VCC regulator operational, the SS pin grounded, and no switching at the HO and LO outputs. If the UVLO pin voltage is above 1.25 V, the SS pin is allowed to ramp and pulse width modulated gate drive signals are delivered to the HO and LO pins. A 20µA current source is enabled when UVLO exceeds 1.25 V and flows through the external UVLO resistors to provide hysteresis. |
| 2 | 1 | DEMB | I | Optional logic input that enables diode emulation when in the low state. In diode emulation mode, the low-side NMOS is latched off for the remainder of the PWM cycle after detecting reverse current flow (current flow from output to ground through the low-side NMOS). When DEMB is high, diode emulation is disabled allowing current to flow in either direction through the low-side NMOS. A 50-kΩ pull-down resistor internal to the LM5117 holds DEMB pin low and enables diode emulation if the pin is left floating. |
| 3 | 2 | RES | O | The restart timer pin that configures the hiccup mode current limiting. A capacitor on the RES pin determines the time the controller remains off before automatically restarting. The hiccup mode commences when the controller experiences 256 consecutive PWM cycles of cycle-by-cycle current limiting. After this occurs, a 10-µA current source charges the RES pin capacitor to the 1.25 V threshold and restarts LM5117. |
| 4 | 3 | SS | I | An external capacitor and an internal 10-µA current source set the ramp rate of the error amplifier reference during soft-start. The SS pin is held low when VCC< 5 V, UVLO < 1.25 V or during thermal shutdown. |
| 5 | 4 | RT | I | The internal oscillator is programmed with a single resistor between RT and the AGND. The recommended maximum oscillator frequency is 750kHz. The internal oscillator can be synchronized to an external clock by coupling a positive pulse into the RT pin through a small coupling capacitor. |
| 6 | 5 | AGND | G | Analog ground. Return for the internal 0.8 V voltage reference and analog circuits. |
| 7 | 7 | VCCDIS | I | Optional input that disables the internal VCC regulator. If VCCDIS>1.25 V, the internal VCC regulator is disabled. VCCDIS has an internal 500-kΩ pulldown resistor to enable the VCC regulator when the pin is left floating. The internal 500-kΩ pull-down resistor can be overridden by pulling VCCDIS above 1.25 V with a resistor divider connected to an external bias supply. |
| 8 | 8 | FB | I | Feedback. Inverting input of the internal error amplifier. A resistor divider from the output to this pin sets the output voltage level. The regulation threshold at the FB pin is 0.8 V. |
| 9 | 9 | COMP | O | Output of the internal error amplifier. The loop compensation network should be connected between this pin and the FB pin. |
| 10 | 10 | CM | O | Current monitor output. Average of the sensed inductor current is provided. Monitor directly between CM and AGND. CM should be left floating when the pin is not used. |
| 11 | 11 | RAMP | I | PWM ramp signal. An external resistor and capacitor connected between the SW pin, the RAMP pin and the AGND pin sets the PWM ramp slope. Proper selection of component values produces a RAMP signal that emulates the AC component of the inductor with a slope proportional to input supply voltage. |
| 12 | 12 | CS | I | Current sense amplifier input. Connect to the high-side of the current sense resistor. |
| 13 | 13 | CSG | G | Kelvin ground connection to the current sense resistor. Connect directly to the low-side of the current sense resistor. |
| 14 | 14 | PGND | O | Power ground return pin for low-side NMOS gate driver. Connect directly to the low-side of the current sense resistor. |
| 15 | 15 | LO | P/O/I | Low-side NMOS gate drive output. Connect to the gate of the low-side synchronous NMOS transistor through a short, low inductance path. |
| 16 | 16 | VCC | I/O | Bias supply pin. Locally decouple to PGND using a low ESR/ESL capacitor located as close to controller as possible. |
| 17 | 18 | SW | O | Switching node of the buck regulator. Connect to the bootstrap capacitor, the source terminal of the high-side NMOS transistor and the drain terminal of the low-side NMOS through a short, low inductance path. |
| 18 | 19 | HO | P | High-side NMOS gate drive output. Connect to the gate of the high-side NMOS transistor through a short, low inductance path. |

(1) I = Input, O = Output, G = Ground, P = Power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**Pin Functions (continued)**

| PIN | | | TYPE (1) | DESCRIPTION |
|---|---|---|---|---|
| HTSSOP | WQFN | NAME | | |
| 19 | 20 | HB | P/I | High-side driver supply for the bootstrap gate drive. Connect to the cathode of the external bootstrap diode and to the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high-side NMOS gate and should be placed as close to controller as possible. |
| 20 | 22 | VIN | P/I | Supply voltage input source for the VCC regulator. |
| EP | EP | EP | - | Exposed pad of the package. Electrically isolated. Should be soldered to the ground plane to reduce thermal resistance. |
| | 6 | NC | - | No electrical contact. |
| | 17 | NC | - | No electrical contact. |
| | 21 | NC | - | No electrical contact. |
| | 23 | NC | - | No electrical contact. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| VIN to AGND | –0.3 | 75 | V |
| SW to AGND | –3.0 | 75 | V |
| HB to SW | –0.3 | 15 | V |
| VCC to AGND (2) | –0.3 | 15 | V |
| HO to SW | –0.3 | HB + 0.3 | V |
| LO to AGND | –0.3 | VCC + 0.3 | V |
| FB, DEMB, RES, VCCDIS, UVLO to AGND | –0.3 | 15 | V |
| CM, COMP to AGND(3) | –0.3 | 7 | V |
| SS, RAMP, RT to AGND | –0.3 | 7 | V |
| CS, CSG, PGND, to AGND | –0.3 | 0.3 | V |
| Storage Temperature, $T_{stg}$ | –55 | 150 | °C |
| Junction temperature | –40 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See *Application and Implementation* when input supply voltage is less than the VCC voltage.
(3) These pins are output pins. As such they are not specified to have an external voltage applied.

## 6.2 ESD Ratings (LM5117)

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22- V C101(2) | ±750 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 ESD Ratings (LM5117-Q1)

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | Charged-device model (CDM), per AEC Q100-011 | ±750 | V |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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## 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| VIN(2) | 5.5 | 65 | V |
| VCC | 5.5 | 14 | V |
| HB to SW | 5.5 | 14 | V |
| Junction temperature | -40 | 125 | °C |

(1) *Recommended Operating Conditions* are conditions under which operation of the device is intended to be functional, but does not ensure specific performance limits. For specifications and test conditions see *Electrical Characteristics*.
(2) Minimum VIN operating voltage is defined with VCC supplied by the internal HV startup regulator and no external load on VCC. When VCC is supplied by an external source, minimum VIN operating voltage is 4.5 V.

## 6.5 Thermal Information

| THERMAL METRIC(1) | | LM5117, LM5117-Q1 | | UNIT |
|---|---|---|---|---|
| | | PWP (HTSSOP) | RTW (WQFN) | |
| | | 20 PINS | 24 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 40 | 40 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 4 | 6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.


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## 6.6 Electrical Characteristics

Typical limits are for $T_J$ = 25°C only, represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only; minimum and maximum limits apply over the junction temperature range of –40°C to +125°C. Unless otherwise specified, the following conditions apply: $V_{VIN}$ = 48 V, $V_{VCCDIS}$ = 0 V, $R_T$ = 25 kΩ, no load on LO and HO.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VIN SUPPLY** | | | | | | |
| $I_{BIAS}$ | $V_{IN}$ operating current (1) | $V_{SS}$ = 0 V | | 4.8 | 6.2 | mA |
| | | $V_{SS}$ = 0 V, $V_{VCCDIS}$ = 2 V | | 0.4 | 0.55 | mA |
| $I_{SHUTDOWN}$ | $V_{IN}$ shutdown current | $V_{SS}$ = 0 V, $V_{UVLO}$ = 0 V | | 16 | 40 | µA |
| **VCC REGULATOR** | | | | | | |
| $V_{CC(REG)}$ | VCC regulation | No load | 6.85 | 7.6 | 8.2 | V |
| | VCC dropout (VIN to VCC) | $V_{VIN}$ = 5.5 V, No external load | | 0.05 | 0.14 | V |
| | | $V_{VIN}$ = 6 V, $I_{CC}$ = 20 mA | | 0.4 | 0.5 | V |
| | VCC sourcing current limit | $V_{VCC}$ = 0 V | 30 | 42 | | mA |
| $I_{VCC}$ | VCC operating current (1) | $V_{SS}$ = 0 V, $V_{VCCDIS}$ = 2 V | | 4 | 5 | mA |
| | | $V_{SS}$ = 0 V, $V_{VCCDIS}$ = 2 V, $V_{VCC}$ = 14 V | | 5.8 | 7.3 | mA |
| | VCC undervoltage threshold | VCC rising | 4.7 | 4.9 | 5.15 | V |
| | VCC undervoltage hysteresis | | | 0.2 | | V |
| **VCC DISABLE** | | | | | | |
| | VCCDIS threshold | VCCDIS rising | 1.22 | 1.25 | 1.29 | V |
| | VCCDIS hysteresis | | | 0.06 | | V |
| | VCCDIS input current | $V_{VCCDIS}$ = 0 V | | -20 | | nA |
| | VCCDIS pulldown resistance | | | 500 | | kΩ |
| **UVLO** | | | | | | |
| | UVLO threshold | UVLO rising | 1.22 | 1.25 | 1.29 | V |
| | UVLO hysteresis current | $V_{UVLO}$ = 1.4 V | 15 | 20 | 25 | µA |
| | UVLO shutdown threshold | UVLO falling | 0.23 | 0.3 | | V |
| | UVLO shutdown hysteresis | | | 0.1 | | V |
| **SOFT START** | | | | | | |
| $I_{SS}$ | SS current source | $V_{SS}$ = 0 V | 7 | 10 | 12 | µA |
| | SS pulldown resistance | | | 13 | 24 | Ω |
| **ERROR AMPLIFIER** | | | | | | |
| $V_{REF}$ | FB reference voltage | Measured at FB, FB = COMP | 788 | 800 | 812 | mV |
| | FB input bias current | $V_{FB}$ = 0.8 V | | 1 | | nA |
| $V_{OH}$ | COMP output high voltage | $I_{SOURCE}$ = 3 mA | 2.8 | | | V |
| $V_{OL}$ | COMP output low voltage | $I_{SINK}$ = 3 mA | | | 0.26 | V |
| $A_{OL}$ | DC gain | | | 80 | | dB |
| $f_{BW}$ | Unity gain bandwidth | | | 3 | | MHz |
| **PWM COMPARATOR** | | | | | | |
| $t_{HO(OFF)}$ | Forced HO Off-time | | 260 | 320 | 440 | ns |
| $t_{ON(MIN)}$ | Minimum HO On-time | $V_{VIN}$ = 65 V | | 100 | | ns |
| | COMP to PWM comparator offset | | | 1.2 | | V |
| **OSCILLATOR** | | | | | | |
| $f_{SW1}$ | Frequency 1 | $R_T$ = 25 kΩ | 180 | 200 | 220 | kHz |
| $f_{SW2}$ | Frequency 2 | $R_T$ = 10 kΩ | 430 | 480 | 530 | kHz |
| | RT output voltage | | | 1.25 | | V |
| | RT sync positive threshold | | 2.6 | 3.2 | 3.95 | V |
| | Sync pulse width | | 100 | | | ns |

(1) Operating current does not include the current into the $R_T$ resistor.

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## Electrical Characteristics (continued)

Typical limits are for $T_J$ = 25°C only, represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only; minimum and maximum limits apply over the junction temperature range of –40°C to +125°C. Unless otherwise specified, the following conditions apply: $V_{VIN}$ = 48 V, $V_{VCCDIS}$ = 0 V, $R_T$ = 25 kΩ, no load on LO and HO.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CURRENT LIMIT** | | | | | | |
| $V_{CS(TH)}$ | Cycle-by-cycle sense voltage threshold | $V_{RAMP}$ = 0 V, CSG to CS | 106 | 120 | 135 | mV |
| | CS input bias current | $V_{CS}$ = 0 V | –100 | -66 | | µA |
| | CSG input bias current | $V_{CSG}$ = 0 V | –100 | -66 | | µA |
| | Current sense amplifier gain | | | 10 | | V/V |
| | Hiccup mode fault timer | | | 256 | | Cycles |
| **RES** | | | | | | |
| $I_{RES}$ | RES Current Source | | | 10 | | µA |
| $V_{RES}$ | RES Threshold | RES Rising | 1.22 | 1.25 | 1.285 | V |
| **DIODE EMULATION** | | | | | | |
| $V_{IL}$ | DEMB input low threshold | | | 2 | 1.65 | V |
| $V_{IH}$ | DEMB input high threshold | | 2.95 | 2.5 | | V |
| | SW zero cross threshold | | | –5 | | mV |
| | DEMB input pulldown resistance | | | 50 | | kΩ |
| **CURRENT MONITOR** | | | | | | |
| | Current monitor amplifier gain | CS to CM | 17.5 | 20.5 | 23.5 | V/V |
| | Current monitor amplifier gain | Drift over Temperature | –2 | 0 | 2 | % |
| | Zero input offset | | | 25 | 120 | mV |
| **HO GATE DRIVER** | | | | | | |
| $V_{OHH}$ | HO High-state voltage drop | $I_{HO}$ = –100 mA, $V_{OHH} = V_{HB} – V_{HO}$ | | 0.17 | 0.3 | V |
| $V_{OLH}$ | HO Low-state voltage drop | $I_{HO}$ = 100 mA, $V_{OLH} = V_{HO} – V_{SW}$ | | 0.1 | 0.2 | V |
| | HO rise time | C-load = 1000 pF(2) | | 6 | | ns |
| | HO fall time | C-load = 1000pF(2) | | 5 | | ns |
| $I_{OHH}$ | Peak HO source current | $V_{HO}$ = 0 V, SW = 0 V, HB = 7.6 V | | 2.2 | | A |
| $I_{OLH}$ | Peak HO sink current | $V_{HO} = V_{HB}$ = 7.6 V | | 3.3 | | A |
| | HB to SW undervoltage | | 2.56 | 2.9 | 3.32 | V |
| | HB DC bias current | HB – SW = 7.6 V | | 65 | 100 | µA |
| **LO GATE DRIVER** | | | | | | |
| $V_{OHL}$ | LO High-state Voltage Drop | $I_{LO}$ = –100 mA, $V_{OHL} = V_{CC}$-$V_{LO}$ | | 0.17 | 0.27 | V |
| $V_{OLL}$ | LO Low-state Voltage Drop | $I_{LO}$ = 100 mA, $V_{OLL} = V_{LO}$ | | 0.1 | 0.2 | V |
| | LO rise time | C-load = 1000 pF(2) | | 6 | | ns |
| | LO fall time | C-load = 1000 pF(2) | | 5 | | ns |
| $I_{OHL}$ | Peak LO source current | $V_{LO}$ = 0 V | | 2.5 | | A |
| $I_{OLL}$ | Peak LO sink current | $V_{LO}$ = 7.6 V | | 3.3 | | A |
| **THERMAL** | | | | | | |
| $T_{SD}$ | Thermal shutdown | Temperature rising | | 165 | | °C |
| | Thermal shutdown hysteresis | | | 25 | | °C |

(2) High and low reference are 80% and 20% of the pulse amplitude, respectively.

## 6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_{DLH}$ | LO fall to HO rise delay | No load | | 72 | | ns |
| $T_{DHL}$ | HO fall to LO rise delay | | | 71 | | ns |


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## 6.8 Typical Characteristics

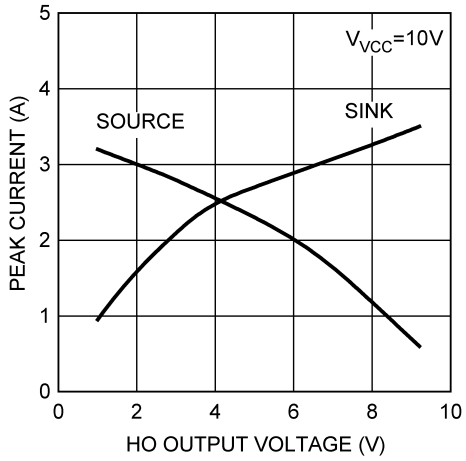


**Figure 1. HO Peak Driver Current vs Output Voltage**

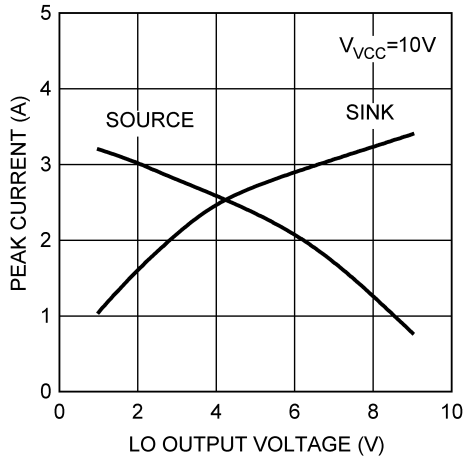


**Figure 2. LO Peak Driver Current vs Output Voltage**

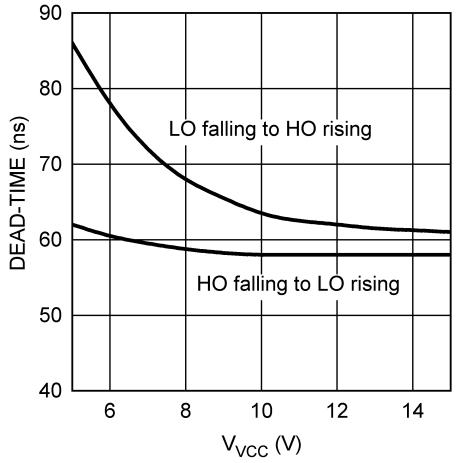


**Figure 3. Driver Dead Time vs $V_{VCC}$**

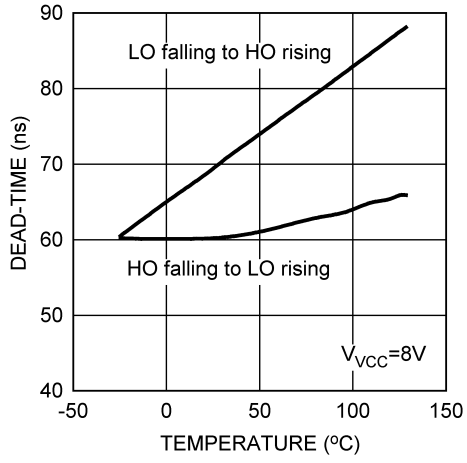


**Figure 4. Driver Dead Time vs Temperature**

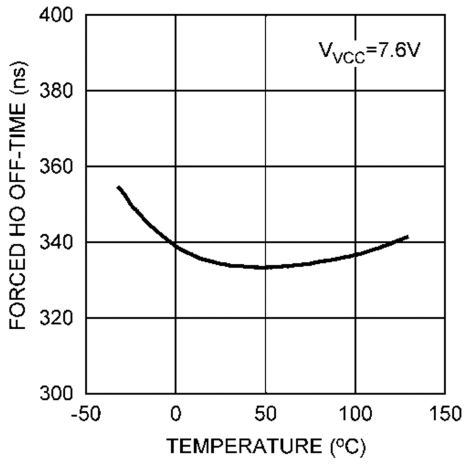


**Figure 5. Forced HO Off-time vs Temperature**

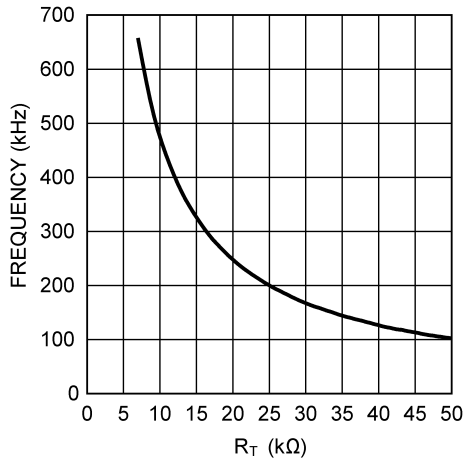


**Figure 6. Switching Frequency vs $R_T$**

## Typical Characteristics (continued)

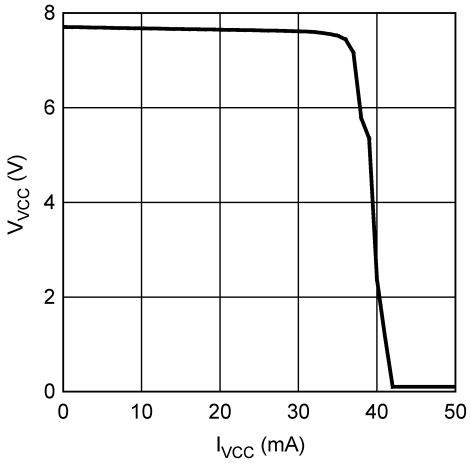


**Figure 7. $V_{VCC}$ vs $I_{VCC}$**

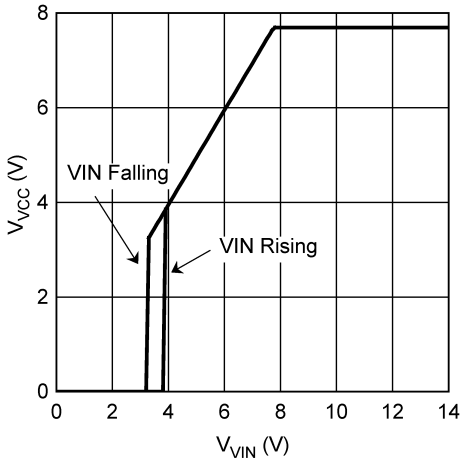


**Figure 8. $V_{VCC}$ vs $V_{VIN}$**

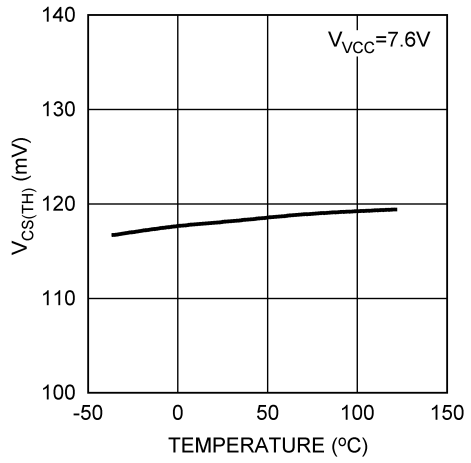


**Figure 9. $V_{CS(TH)}$ vs Temperature**

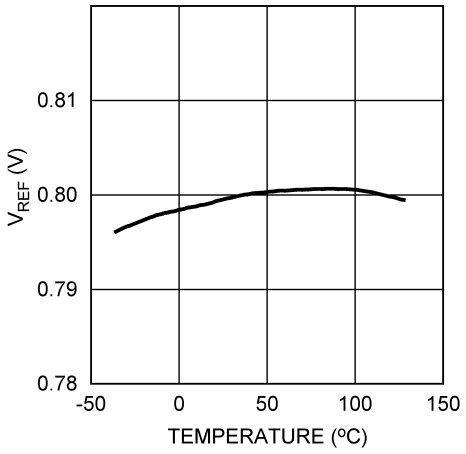


**Figure 10. $V_{REF}$ vs Temperature**

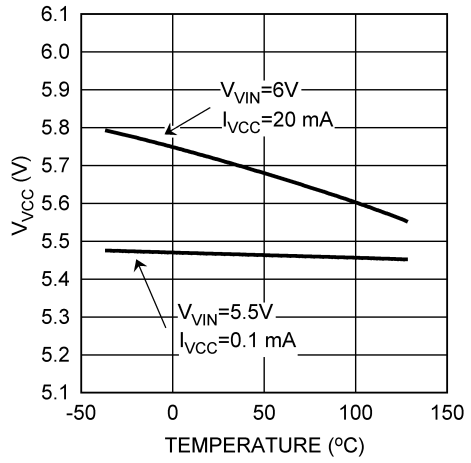


**Figure 11. $V_{VCC}$ vs Temperature**

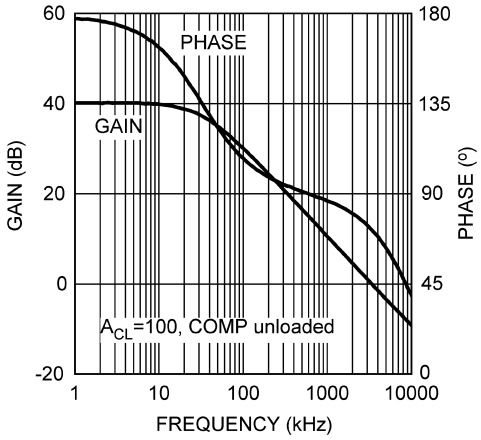


**Figure 12. Error Amp Gain and Phase vs Frequency**


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## Typical Characteristics (continued)

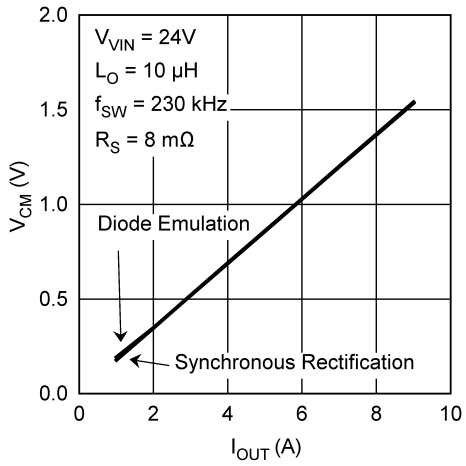


**Figure 13. $V_{CM}$ vs $I_{OUT}$**

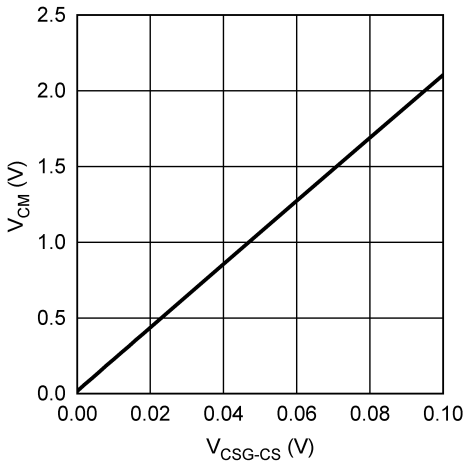


**Figure 14. $V_{CM}$ vs $V_{CSG-CS}$**

# 7 Detailed Description

## 7.1 Overview

The LM5117 high voltage switching controller features all of the functions necessary to implement an efficient high voltage buck regulator that operates over a very wide input voltage range. This easy to use controller integrates high-side and low-side NMOS drivers. The regulator control method is based upon peak current mode control utilizing an emulated current ramp. Peak current mode control provides inherent line feed-forward, cycle-by-cycle current limiting and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the PWM circuit, allowing reliable processing of the very small duty cycles necessary in high input voltage applications.

The switching frequency is user programmable up to 750 kHz. The RT pin allows the switching frequency to be programmed by a single resistor or synchronized to an external clock. Fault protection features include cycle-by-cycle and hiccup mode current limiting, thermal shutdown and remote shutdown capability by pulling down UVLO pin. The UVLO input enables the regulator when the input voltage reaches a user selected threshold and provides a very low quiescent shutdown current when pulled low. A unique analog telemetry feature provides averaged output current information, allowing various applications that need either a current monitor or current control. The functional block diagram and typical application circuit of the LM5117 are shown in *Functional Block Diagram*.

The device is available in a HTSSOP-20 (6.5 mm x 4.4 mm) package, as well as a WQFN-24 (4 mm × 4 mm) package which features an exposed pad to aid in thermal dissipation.

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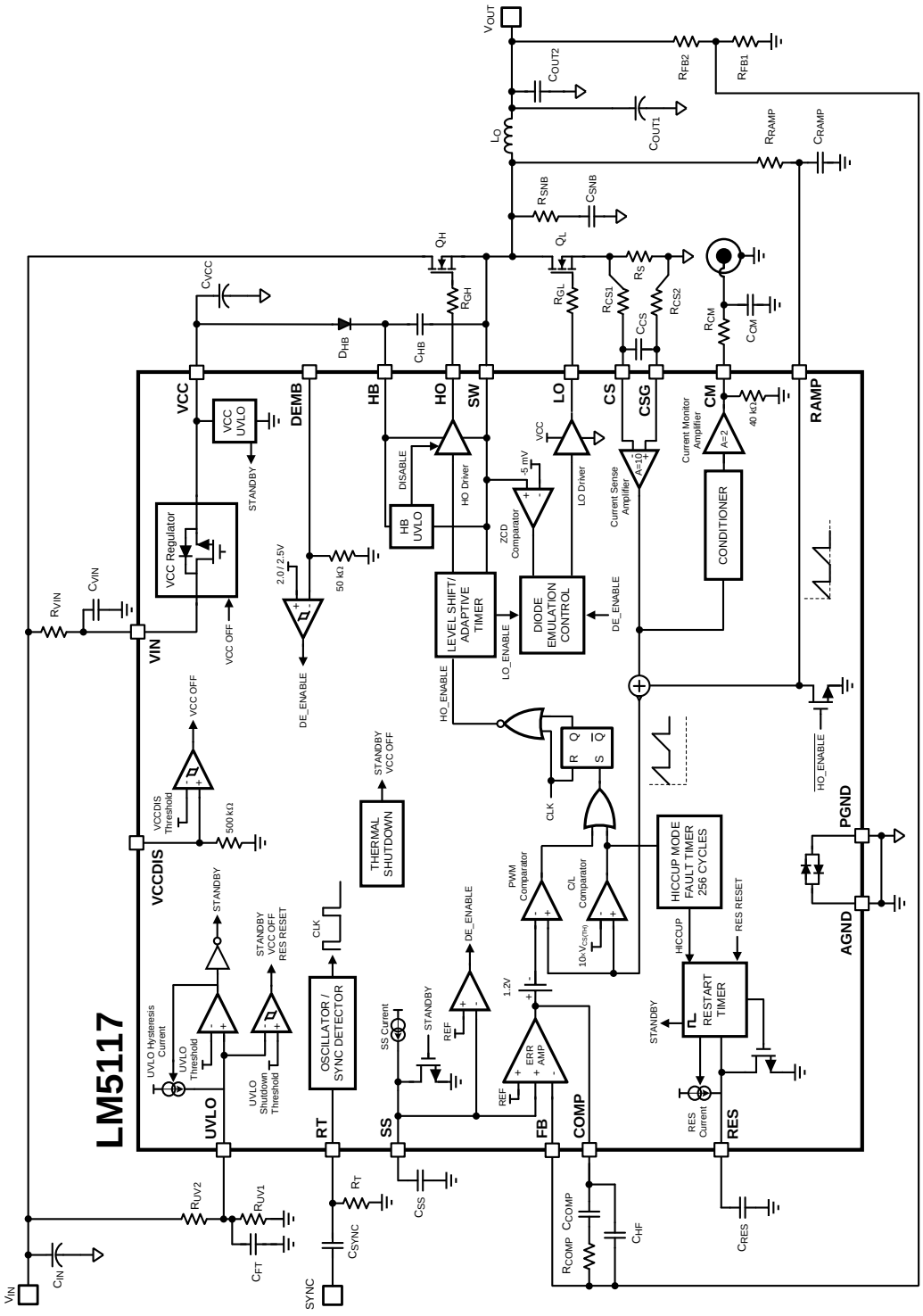
## 7.2 Functional Block Diagram





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## 7.3 Feature Description

### 7.3.1 High Voltage Start-up Regulator and VCC Disable

The LM5117 contains an internal high voltage bias regulator that provides the VCC bias supply for the PWM controller and NMOS gate drivers. The VIN pin can be connected to an input voltage source as high as 65 V. The output of the VCC regulator is set to 7.6V. When the input voltage is below the VCC set-point level, the VCC output tracks the VIN with a small dropout voltage. The output of the VCC regulator is current limited at 30mA minimum.

Upon power-up, the regulator sources current into the capacitor connected to the VCC pin. The recommended capacitance range for the pin VCC is 0.47 µF to 10 µF. When the VCC pin voltage exceeds the VCC UV threshold and the UVLO pin is greater than UVLO threshold, the HO and LO drivers are enabled and a soft-start sequence begins. The HO and LO drivers remain enabled until either the VCC pin voltage falls below VCC UV threshold, the UVLO pin voltage falls below UVLO threshold, hiccup mode is activated or the die temperature exceeds the thermal shutdown threshold. Enabling/Disabling the IC by controlling UVLO is recommended in most of cases.

An output voltage derived bias supply can be applied to the VCC pin to reduce the controller power dissipation at higher input voltage. The VCCDIS input can be used to disable the internal VCC regulator when external biasing is supplied. The externally supplied bias should be coupled to the VCC pin through a diode, preferably a Schottky diode. If the VCCDIS pin voltage exceeds the VCCDIS threshold, the internal VCC regulator is disabled. VCCDIS has a 500-kΩ internal pull-down resistor to ground for normal operation with no external bias.

The VCC regulator series pass transistor includes a diode between VCC (Anode) and VIN (Cathode) that should not be forward biased in normal operation. If the voltage of the external bias supply is greater than the VIN pin voltage, an external blocking diode is required from the input power supply to the VIN pin to prevent the external bias supply from passing current to the input supply through VCC.

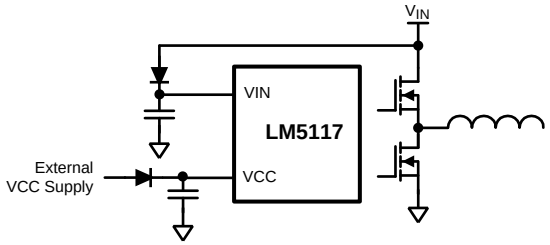


**Figure 15. VIN Configuration for $V_{VIN} < V_{VCC}$**

For $V_{OUT}$ between 6 V and 14.5 V, the output can be connected directly to VCC through a diode.

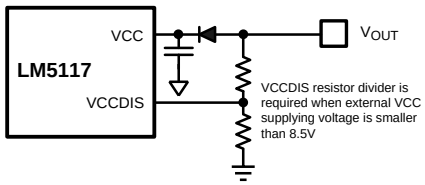


**Figure 16. External VCC Supply for 6 V < $V_{OUT}$< 14.5 V**

For $V_{OUT}$ < 6 V, a bias winding on the output inductor can be added to generate the external VCC supply voltage.

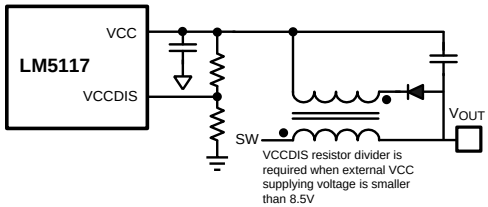


**Figure 17. External VCC Supply for $V_{OUT}$ < 6 V**

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## Feature Description (continued)

For 14.5 V <$V_{OUT}$, the external supply voltage can be regulated by using a series Zener diode from the output to VCC.

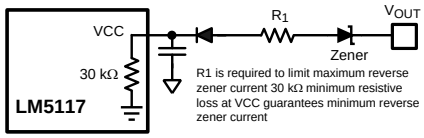


**Figure 18. External VCC Supply for 14.5 V < $V_{OUT}$**

In high input voltage applications, extra care should be taken to ensure the VIN pin does not exceed the absolute maximum voltage rating of 75V. During line or load transients, voltage ringing on the VIN that exceeds the Absolute Maximum Rating can damage the IC. Both careful PC board layout and the use of quality bypass capacitors located close to the VIN and AGND pin are essential. Adding an R-C filter ($R_{VIN}$, $C_{VIN}$) on VIN is optional and helps to prevent faulty operation caused by poor PC board layout and high frequency switching noise injection. The recommended capacitance and resistance range are 0.1 µF to 10 µF and 1 Ω to 10 Ω.

### 7.3.2 UVLO

The LM5117 contains a dual level UVLO (under-voltage lockout) circuit. When the UVLO is less than 0.4 V, the LM5117 is in shutdown mode. The shutdown comparator provides 100 mV of hysteresis to avoid chatter during transitions. When the UVLO pin voltage is greater than 0.4 V but less than 1.25 V, the controller is in standby mode. In the standby mode, the VCC bias regulator is active but the HO and LO drivers are disabled and the SS pin is held low. This feature allows the UVLO pin to be used as a remote shutdown function by pulling the UVLO pin down below 0.4 V with an external open collector or open drain device. When the VCC pin exceeds its under-voltage lockout threshold and the UVLO pin voltage is greater than 1.25 V, the HO and LO drivers are enabled and normal operation begins.

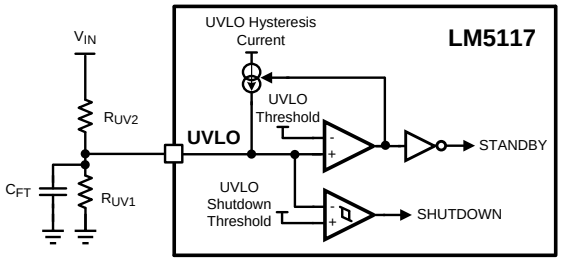


**Figure 19. UVLO Configuration**

The UVLO pin should not be left floating. An external UVLO set-point voltage divider from the VIN to AGND is used to set the minimum input operating voltage of the regulator. The divider must be designed such that the voltage at the UVLO pin is greater than 1.25 V and never exceeds 15 V when the input voltage is in the desired operating range. If necessary, the UVLO pin can be clamped with a Zener diode.

UVLO hysteresis is accomplished with an internal 20µA current source that is switched on or off into the impedance of the UVLO set-point divider. When the UVLO pin voltage exceeds the 1.25 V threshold, the current source is enabled to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25 V threshold, the current source is disabled causing the voltage at the UVLO pin to quickly fall. The use of a $C_{FT}$ capacitor in parallel with $R_{UV1}$ helps to minimize switching noise injection into UVLO pin, but it may slow down the falling speed of the UVLO pin when the 20 µA current source is disabled. The recommended range for $C_{FT}$ is 10 pF to 220 pF.


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## Feature Description (continued)

The values of $R_{UV1}$ and $R_{UV2}$ can be determined from the following equations:

$$R_{UV2} = \frac{V_{HYS}}{20\ \mu A}\ [\Omega] \quad (1)$$

$$R_{UV1} = \frac{1.25V \times R_{UV2}}{V_{IN(STARTUP)} - 1.25V}\ [\Omega] \quad (2)$$

where

- $V_{HYS}$ is the desired UVLO hysteresis and $V_{IN(STARTUP)}$ is the desired start-up voltage of the regulator during turn-on

### 7.3.3 Oscillator and Sync Capability

The LM5117 switching frequency is programmed by a single external resistor connected between the RT pin and the AGND pin. The resistor should be located very close to the device and connected directly to the RT and AGND pins. To set a desired switching frequency ($f_{SW}$), the resistor value can be calculated from the following equation:

$$R_T = \frac{5.2 \times 10^9}{f_{SW}} - 948\ [\Omega] \quad (3)$$

The RT pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by AC coupling a positive edge into the RT pin. The voltage at the RT pin is nominally 1.25 V and the voltage at the RT pin must exceed the RT Sync Positive Threshold to trip the internal synchronization pulse detector. A 5 V amplitude pulse signal coupled through a 100-pF capacitor is a good starting point. The frequency of the external synchronization pulse is recommended to be within ±10% of the frequency programmed by the RT resistor but will operate to +100/-40% of the programmed frequency. Care should be taken to guarantee that the RT pin voltage does not go below –0.3 V at the falling edge of the external pulse. This may limit the duty cycle of external synchronization pulse.

The $R_T$ resistor is always required, whether the oscillator is free running or externally synchronized.

### 7.3.4 Ramp Generator and Emulated Current Sense

The ramp signal used in the pulse width modulator for traditional current mode control is typically derived directly from the high-side switch current. This switch current corresponds to the positive slope portion of the inductor current. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feed-forward compensation.

The disadvantage of using the high-side switch current signal for PWM control is the large leading edge spike due to circuit parasitics that must be filtered or blanked. Minimum achievable pulse width is limited by the filtering, blanking time and propagation delay with a high-side current sensing scheme.

In the applications where the input voltage may be relatively large in comparison to the output voltage, controlling small pulse widths and duty cycles are necessary for regulation. The LM5117 utilizes a unique ramp generator which does not actually measure the high-side switch current but rather reconstructs the signal. Representing or emulating the inductor current provides a ramp signal to the PWM comparator that is free of leading edge spikes and measurement or filtering delays, while maintaining the advantages of traditional peak current mode control.

The current reconstruction is comprised of two elements: a sample-and-hold DC level and the emulated inductor current ramp as shown in Figure 20. The sample-and-hold DC level is derived from a measurement of the recirculating current flowing through the current sense resistor. The voltage across the sense resistor is sampled and held just prior to the onset of the next conduction interval of the high-side switch. The current sense amplifier with a gain of 10 and sample-and-hold circuit provide the DC level of the reconstructed current signal as shown in Figure 21.

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## Feature Description (continued)

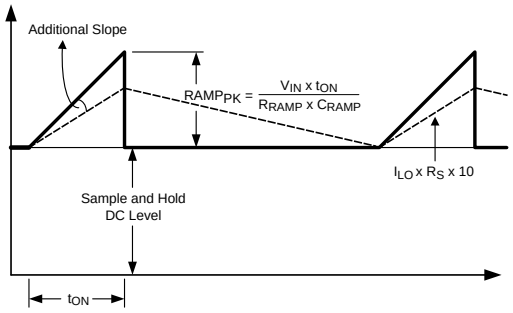


**Figure 20. Composition of Emulated Current Sense Signal**

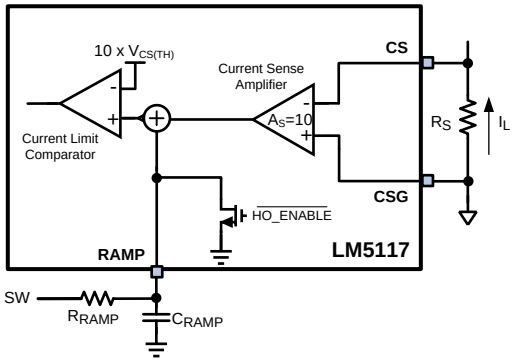


**Figure 21. RAMP Generator and Current Limit Circuit**

The positive slope inductor current ramp is emulated by $C_{RAMP}$ connected between RAMP and AGND and $R_{RAMP}$ connected between SW and RAMP. $R_{RAMP}$ should not be connected to VIN directly because the RAMP pin absolute maximum voltage rating could be exceeded under high input voltage conditions. $C_{RAMP}$ is discharged by an internal switch during the off-time and must be fully discharged during the minimum off-time. This limits the ramp capacitor to be less than 2 nF. A good quality, thermally stable ceramic capacitor is recommended for $C_{RAMP}$.

The selection of $R_{RAMP}$ and $C_{RAMP}$ can be simplified by adopting a K factor, which is defined as:

$$K = \frac{L_O}{R_{RAMP} \times C_{RAMP} \times R_S \times A_S} \quad (4)$$

where

- $A_S$ is the current sense amplifier gain which is normally 10

By choosing 1 as the K factor, the regulator removes any error after one switching cycle and the design procedure is simplified. See *Application and Implementation* for detailed information.

### 7.3.5 Error Amplifier and PWM Comparator

The internal high-gain error amplifier generates an error signal proportional to the difference between the FB pin voltage and the internal precision 0.8-V reference. The output of error amplifier is connected to the COMP pin allowing the user to provide Type 2 loop compensation components, $R_{COMP}$, $C_{COMP}$ and optional $C_{HF}$.


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## Feature Description (continued)

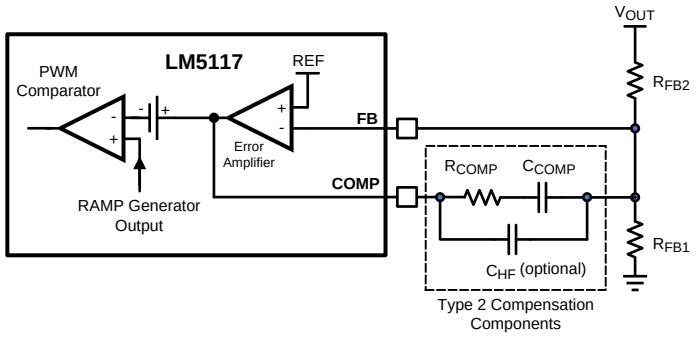


**Figure 22. Feedback Configuration and PWM Comparator**

$R_{COMP}$, $C_{COMP}$ and $C_{HF}$ configure the error amplifier gain and phase characteristics to achieve a stable voltage loop gain. This network creates a pole at DC ($F_{P1}$), a mid-band zero ($F_Z$) for phase boost, and a high frequency pole ($F_{P2}$). The recommended range of $R_{COMP}$ is 2 kΩ to 40 kΩ. See *Application and Implementation* for detailed information.

$$F_{P1} = 0 \quad [Hz] \tag{5}$$

$$F_Z = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \quad [Hz] \tag{6}$$

$$F_{P2} = \frac{1}{2\pi \times R_{COMP} \times \left(\frac{C_{COMP} \times C_{HF}}{C_{COMP} + C_{HF}}\right)} \quad [Hz] \tag{7}$$

The PWM comparator compares the emulated current sense signal from Ramp Generator to the voltage at the COMP pin through a 1.2-V internal voltage drop and terminates the present cycle when the emulated current sense signal is greater than $V_{COMP}$ – 1.2 V.

### 7.3.6 Soft-Start

The soft-start feature allows the regulator to gradually reach the steady state operating point, thus reducing startup stresses and surges. The LM5117 regulates the FB pin to the SS pin voltage or the internal 0.8-V reference, whichever is lower. The internal 10-µA soft-start current source gradually increases the voltage on an external soft-start capacitor connected to the SS pin. This results in a gradual rise of the output voltage. Soft-start time ($t_{ss}$) can be calculated from the following equation:

$$t_{SS} = \frac{C_{SS} \times 0.8V}{10\ \mu A} \ [sec] \tag{8}$$

The LM5117 can track the output of a master power supply during soft-start by connecting a voltage divider from the output of master power supply to the SS pin. At the beginning of the soft-start sequence, $V_{SS}$ should be allowed to go below 25 mV by the internal SS pull-down switch. During soft-start period, when SS pin voltage is less than 0.8V, the LM5117 forces diode emulation for startup into a pre-biased load. If the tracking feature is desired, connect the DEMB pin to GND or leave the pin floating.

### 7.3.7 Cycle-by-Cycle Current Limit

The LM5117 contains a current limit monitoring scheme to protect the regulator from possible over-current conditions as shown in Figure 21. If the emulated ramp signal exceeds 1.2 V, the present cycle is terminated. For the case where the switch current overshoots when the inductor is saturated or the output is shorted to ground, the sample-and-hold circuit detects the excess recirculating current before the high-side NMOS driver is turned on again. The high-side NMOS driver is disabled and will skip pulses until the current has decayed below the current limit threshold. This approach prevents current runaway conditions since the inductor current is forced to decay to a controlled level following any current overshoot.

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## Feature Description (continued)

Maximum peak inductor current can be calculated as:

$$I_{L(MAX)_PK} = \frac{V_{CS(TH)}}{R_S} + I_{PP} - \frac{V_{OUT}}{f_{SW} \times A_S \times R_S \times R_{RAMP} \times C_{RAMP}} \text{ [A]} \quad (9)$$

$$I_{L(MAX)_AVE} = I_{L(MAX)_PK} - \frac{I_{PP}}{2} \text{ [A]}$$

where

- $I_{PP}$ represents inductor peak to peak ripple current in Figure 23, and is defined as: (10)

$$I_{PP} = \frac{V_{OUT}}{L_O \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \text{ [A]} \quad (11)$$

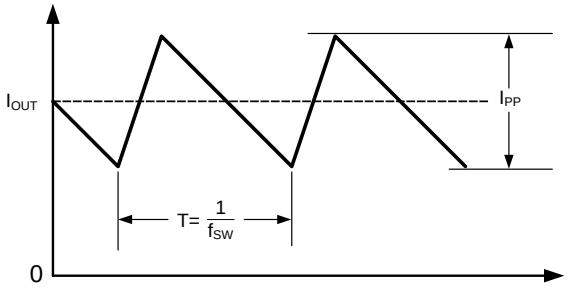


**Figure 23. Inductor Current**

During an output short condition, the worst case peak inductor current is limited to:

$$I_{LIM_PK} = \frac{V_{CS(TH)}}{R_S} + \frac{V_{IN(MAX)} \times t_{ON(MIN)}}{L_O} \text{ [A]}$$

where

- $t_{ON(MIN)}$ is the minimum HO on-time (12)

In most cases, especially if the output voltage is relatively high, it is recommended that a soft-saturating inductor such as a powder core device is used. If a sharp-saturating inductor is used, the inductor saturation level must be above $I_{LIM_PK}$. The temperatures of the NMOS devices, $R_S$ and inductor should be checked under this output short condition.

### 7.3.8 Hiccup Mode Current Limiting

To further protect the regulator during prolonged current limit conditions, LM5117 provides a hiccup mode current limit. An internal hiccup mode fault timer counts the PWM clock cycles during which cycle-by-cycle current limiting occurs. When the hiccup mode fault timer detects 256 consecutive cycles of current limiting, an internal restart timer forces the controller to enter a low power dissipation standby mode and starts sourcing 10 µA of current into the RES pin capacitor $C_{RES}$. In this standby mode, HO and LO outputs are disabled and the soft-start capacitor $C_{SS}$ is discharged.


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## Feature Description (continued)

$C_{RES}$ is connected from RES pin to AGND and determines the time ($t_{RES}$) in which the LM5117 remains in the standby before automatically restarting. When the RES pin voltage exceeds the 1.25-V RES threshold, RES capacitor is discharged and a soft-start sequence begins. $t_{RES}$ can be calculated from the following equation:

$$t_{RES} = \frac{C_{RES} \times 1.25V}{10\ \mu A}\ [sec] \quad (13)$$

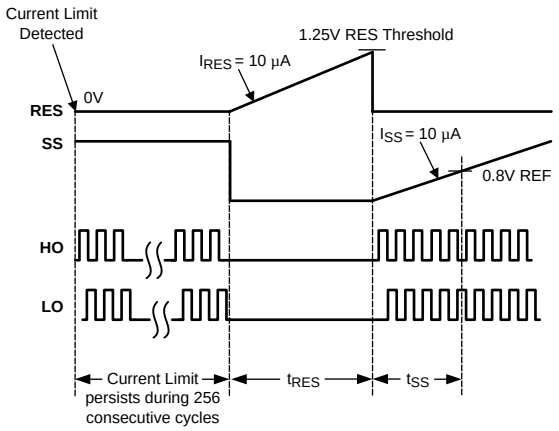



**Figure 24. Hiccup Mode Current Limit Timing Diagram**

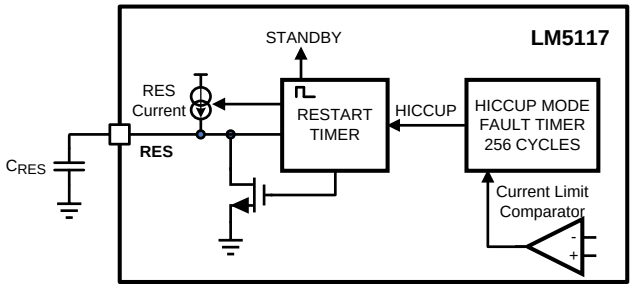
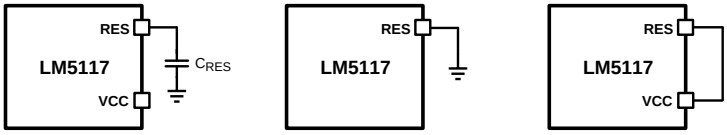



**Figure 25. Hiccup Mode Current Limit Circuit**

The RES pin can also be configured for latch-off mode current limiting or non-hiccup mode cycle-by-cycle current limiting. If the RES pin is tied to VCC or a voltage greater than the RES threshold at initial power-on, the restart timer is disabled and the regulator operates with non-hiccup mode cycle-by-cycle current limit. If the RES pin is tied to GND, the regulator enters into the standby mode after 256 consecutive cycles of current limiting and then never restarts until UVLO shutdown is cycled. The restart timer is configured during initial power-on when UVLO is above the UVLO threshold and VCC is above the VCC UV threshold.




(a) Hiccup Mode Current Limit (b) Latch-off Mode Current Limit (c) Cycle-by-cycle Current Limit

**Figure 26. RES Configurations**

## Feature Description (continued)

### 7.3.9 HO and LO Drivers

The LM5117 contains high current NMOS drivers and an associated high-side level shifter to drive the external high-side NMOS device. This high-side gate driver works in conjunction with an external diode $D_{HB}$, and bootstrap capacitor $C_{HB}$. A 0.1-µF or larger ceramic capacitor, connected with short traces between the HB and SW pin, is recommended. During the off-time of the high-side NMOS driver, the SW pin voltage is approximately 0V and the $C_{HB}$ is charged from VCC through the $D_{HB}$. When operating with a high PWM duty cycle, the high-side NMOS device is forced off each cycle for 320 ns to ensure that $C_{HB}$ is recharged.

The LO and HO outputs are controlled with an adaptive dead-time methodology which insures that both outputs are never enabled at the same time. When the controller commands HO to be enabled, the adaptive dead-time logic first disables LO and waits for the LO voltage to drop. HO is then enabled after a small delay (LO Fall to HO Rise Delay). Similarly, the LO turn-on is delayed until the HO voltage has discharged. LO is then enabled after a small delay (HO Fall to LO Rise Delay). This technique insures adequate dead-time for any size NMOS device, especially when VCC is supplied by a higher external voltage source. The adaptive dead-time circuitry monitors the voltages of HO and LO outputs and insures the dead-time between the HO and LO outputs. Adding a gate resister, $R_{GH}$ or $R_{GL}$, may decrease the effective dead-time.

Care should be exercised in selecting an output NMOS device with the appropriate threshold voltage, especially if VCC is supplied by an external bias supply voltage below the VCC regulation level. During startup at low input voltages, the low-side NMOS device gate plateau voltage should be lower than the VCC under-voltage lockout threshold. Otherwise, there may be insufficient VCC voltage to completely enhance the NMOS device as the VCC under-voltage lockout is released during startup. If the high-side NMOS drive voltage is lower than the high-side NMOS device gate plateau voltage during startup, the regulator may not start or it may hang up momentarily in a high power dissipation state. This condition can be addressed by selecting an NMOS device with a lower threshold voltage. This situation can be avoided if the minimum input voltage programmed by the UVLO resistor is above the VCC regulation level.

### 7.3.10 Current Monitor

The LM5117 provides average output current information, enabling various applications requiring monitoring or control of the output current.

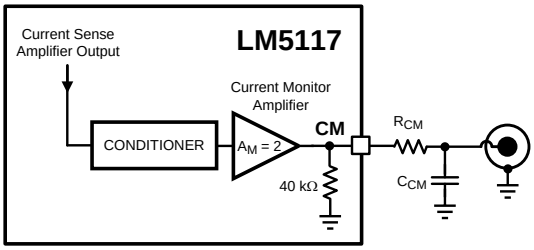



**Figure 27. Current Monitor**

The average of CM output can be calculated by:

$$V_{CM_AVE} = (I_{PEAK} + I_{VALLEY}) \times R_S \times A_S \quad [V] \tag{14}$$

The current monitor output is only valid in continuous conduction operation. The current monitor has a limited bandwidth of approximately one tenth of $f_{SW}$. Adding an R-C filter, $R_{CM}$ and $C_{CM}$, on the output of current monitor with the cut off frequency below one tenth of $f_{SW}$ is recommended to attenuate sampling noise.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## Feature Description (continued)

### 7.3.11 Maximum Duty Cycle

When operating with a high PWM duty cycle, the high-side NMOS device is forced off each cycle for 320ns to ensure that $C_{HB}$ is recharged and to allow time to sample and hold the current in the low-side NMOS FET. This forced off-time limits the maximum duty cycle of the controller. When designing a regulator with high switching frequency and high duty cycle requirements, a check should be made of the required maximum duty cycle against the graph shown in Figure 28. The actual maximum duty cycle varies with the switching frequency as follows:

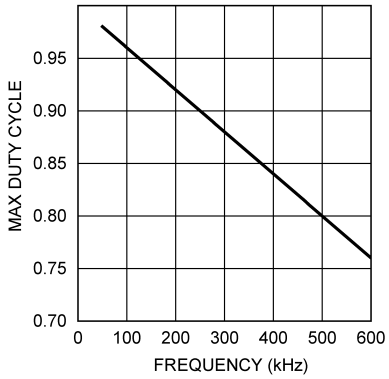


**Figure 28. Maximum Duty Cycle vs Switching Frequency**

### 7.3.12 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the controller in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power shutdown mode, disabling the output drivers and the VCC regulator. This feature is designed to prevent overheating and destroying the device.

## 7.4 Device Functional Modes

### 7.4.1 Diode Emulation

A fully synchronous buck regulator implemented with a freewheeling NMOS rather than a diode has the capability to sink current from the output in certain conditions such as light load, over-voltage or pre-bias startup. The LM5117 provides a diode emulation feature that can be enabled to prevent reverse current flow in the low-side NMOS device. When configured for diode emulation, the low-side NMOS driver is disabled when SW pin voltage is greater than -5mV during the off-time of the high-side NMOS driver, preventing reverse current flow.

A benefit of the diode emulation is lower power loss at no load or light load conditions. The negative effect of diode emulation is degraded light load transient response.

The diode emulation feature is configured with the DEMB pin. To enable diode emulation, connect the DEMB pin to GND or leave the pin floating. If continuous conduction operation is desired, the DEMB pin should be tied to a voltage greater than 3 V and may be connected to VCC. The LM5117 forces the regulator to operate in diode emulation mode when SS pin voltage is less than the internal 0.8-V reference, allowing for startup into a pre-biased load with the continuous conduction configuration.

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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The LM5117 is a step-down dc-dc controller. The device is typically used to convert a higher dc-dc voltage to a lower dc voltage. Use the following design procedure to select component values. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and assesses a comprehensive database of components when generating a design.

## 8.2 Typical Applications

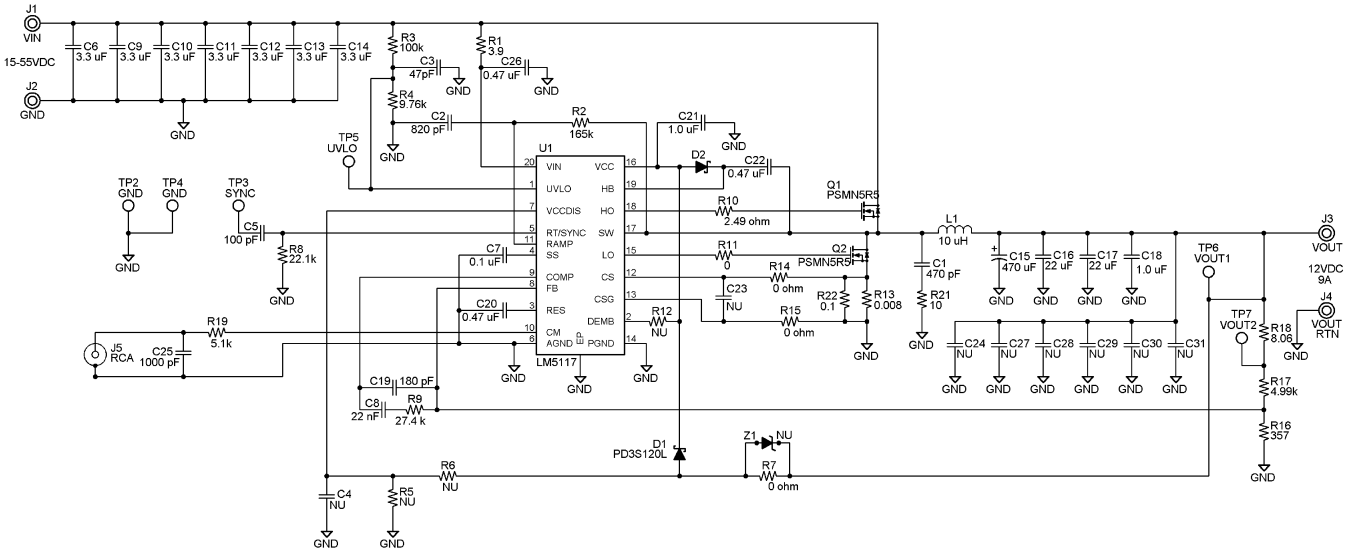


**Figure 29. 12 V, 9 A Typical Application Schematic**

## 8.3 Detailed Design Procedure

### 8.3.1 Feedback Compensation

Open loop response of the regulator is defined as the product of modulator transfer function and feedback transfer function. When plotted on a dB scale, the open loop gain is shown as the sum of modulator gain and feedback gain.


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## Detailed Design Procedure (continued)

The modulator transfer function includes a power stage transfer function with an embedded current loop and can be simplified as one pole and one zero system as shown in Equation 15.

$$\frac{\hat{V}_{OUT}}{\hat{V}_{COMP}} = A_M \times \frac{1 + \frac{s}{\omega_{Z_ESR}}}{\left(1 + \frac{s}{\omega_{P_LF}}\right)} \tag{15}$$

Where $A_M$ (Modulator DC gain) = $\frac{R_{LOAD}}{R_S \times A_S}$,

$\omega_{Z_ESR}$ (ESR zero) = $\frac{1}{R_{ESR} \times C_{OUT}}$,

$\omega_{P_LF}$ (Load pole) = $\frac{1}{R_{LOAD} \times C_{OUT}}$

If the ESR of $C_{OUT}$ ($R_{ESR}$) is very small, the modulator transfer function can be further simplified to a one pole system and the voltage loop can be closed with only two loop compensation components, $R_{COMP}$ and $C_{COMP}$, leaving a single pole response at the crossover frequency. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

The feedback transfer function includes the feedback resistor divider and loop compensation of the error amplifier. $R_{COMP}$, $C_{COMP}$ and optional $C_{HF}$ configure the error amplifier gain and phase characteristics and create a pole at origin, a low frequency zero and a high frequency pole. This is shown mathematically in Equation 16.

$$-\frac{\hat{V}_{COMP}}{\hat{V}_{OUT}} = A_{FB} \times \frac{1 + \frac{s}{\omega_{Z_EA}}}{s \times \left(1 + \frac{s}{\omega_{P_EA}}\right)} \tag{16}$$

Where $A_{FB}$ (Feedback DC gain) = $\frac{1}{R_{FB2} \times (C_{COMP} + C_{HF})}$,

$w_{Z_EA}$ (Low frequency zero) = $\frac{1}{R_{COMP} \times C_{COMP}}$,

$w_{P_EA}$ (High frequency pole) = $\frac{1}{R_{COMP} \times C_{HF}}$

The pole at the origin minimizes output steady state error. The low frequency zero should be placed to cancel the load pole of the modulator. The high frequency pole can be used to cancel the zero created by the output capacitor ESR or to decrease noise susceptibility of the error amplifier. By placing the low frequency zero an order of magnitude less than the crossover frequency, the maximum amount of phase boost can be achieved at the crossover frequency. The high frequency pole should be placed well beyond the crossover frequency since the addition of $C_{HF}$ adds a pole in the feedback transfer function.

The crossover frequency (loop bandwidth) is usually selected between one twentieth and one fifth of the $f_{SW}$. In a simplified formula, the crossover frequency can be defined as:

$$f_{CROSS} = \frac{R_{COMP}}{2 \times \pi \times R_S \times R_{FB2} \times A_S \times C_{OUT}} \text{ [Hz]} \tag{17}$$

For higher crossover frequency, $R_{COMP}$ can be increased, while proportionally decreasing $C_{COMP}$. Conversely, decreasing $R_{COMP}$ while proportionally increasing $C_{COMP}$, results in lower bandwidth while keeping the same zero frequency in the feedback transfer function.

The sampled gain inductor pole is inversely proportional to the K factor, which is defined as:

$$\omega_{p_HF} = \frac{f_{SW}}{K - 0.5} \tag{18}$$

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## Detailed Design Procedure (continued)

The maximum achievable loop bandwidth, in fact, is limited by this sampled gain inductor pole. In traditional current mode control, the maximum achievable loop bandwidth varies with input voltage. With the LM5117's unique slope compensation scheme, the sampled gain inductor pole is independent of changes to the input voltage. This frees the user from additional concerns in wide varying input range applications and is an advantage of the LM5117.

If the sampled gain inductor pole or the ESR zero is close to the crossover frequency, it is recommended that the comprehensive formulas in Table 1 be used and the stability should be checked by a network analyzer. The modulator transfer function can be measured and the feedback transfer function can be configured for the desired open loop transfer function. If a network analyzer is not available, step load transient tests can be performed to verify acceptable performance. The step load goal is minimum overshoot/undershoot with a damped response.

### 8.3.2 Sub-Harmonic Oscillation

Peak current mode regulators can exhibit unstable behavior when operating above 50% duty cycle. This behavior is known as sub-harmonic oscillation and is characterized by alternating wide and narrow pulses at the SW pin. Sub-harmonic oscillation can be prevented by adding an additional voltage ramp (slope compensation) on top of the sensed inductor current shown in Figure 20. By choosing K≥1, the regulator will not be subject to sub-harmonic oscillation caused by a varying input voltage.

In time-domain analysis, the steady-state inductor current starts and ends at the same value during one clock cycle. If the magnitude of the end-of-cycle current error, $dI_1$, caused by an initial perturbation, $dI_0$, is less than the magnitude of $dI_0$ or $dI_1/dI_0 > -1$, the perturbation naturally disappears after a few cycles. When $dI_1/dI_0 < -1$, the initial perturbation does not disappear, resulting in sub-harmonic oscillation in steady-state operation.

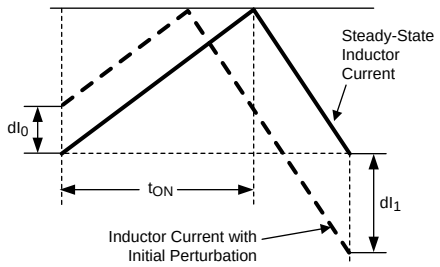


**Figure 30. Effect of Initial Perturbation when $dI_1/dI_0 < -1$**

$dI_1/dI_0$ can be calculated by:

$$\frac{dI_1}{dI_0} = 1 - \frac{1}{K} \tag{19}$$

The relationship between $dI_1/dI_0$ and K factor is illustrated graphically in Figure 31.

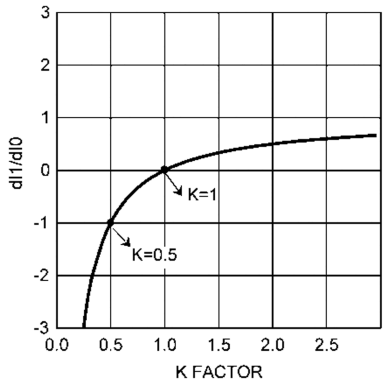


**Figure 31. $dI_1/dI_0$ vs K Factor**


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## Detailed Design Procedure (continued)

The minimum value of K is 0.5. When K<0.5, the amplitude of $dI_1$ is greater than the amplitude of $dI_0$ and any initial perturbation results in sub-harmonic oscillation. If K=1, any initial perturbation will be removed in one switching cycle. This is known as one-cycle damping. When $-1<dI_1/dI_0<0$, any initial perturbation will be under-damped. Any perturbation will be over-damped when $0<dI_1/dI_0<1$.

In the frequency-domain, Q, the quality factor of the sampling gain term in the modulator transfer function, is used to predict the tendency for sub-harmonic oscillation, which is defined as:

$$Q = \frac{1}{\pi(K-0.5)} \tag{20}$$

The relationship between Q and K factor is illustrated graphically in Figure 32.

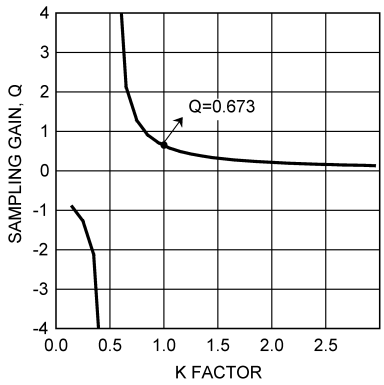


**Figure 32. Sampling gain Q vs K Factor**

The minimum value of K is 0.5 again. This is the same as time domain analysis result. When K<0.5, the regulator is unstable. High gain peaking at 0.5 results in sub-harmonic oscillation at $F_{SW}/2$. When K=1, one-cycle damping is realized. Q is equal to 0.673 at this point. A higher K factor may introduce additional phase shift by moving the sampled gain inductor pole closer to the crossover frequency, but will help reduce noise sensitivity in the current loop. The maximum allowable value of K factor can be calculated by the Maximum Crossover Frequency equation in Table 1.

### 8.3.3 Design Requirements

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Output voltage | 12 V |
| Full load current, $I_{OUT}$ | 9 A |
| Minimum input voltage, $V_{IN(MIN)}$ | 15 V |
| Maximum input voltage, $V_{IN(MAX)}$ | 55 V |
| Switching frequency, $f_{SW}$ | 230 kHz |
| Diode emulation | yes |
| External VCC supply | yes |

### 8.3.4 Timing Resistor $R_T$

Generally, higher frequency applications are smaller but have higher losses. Operation at 230 kHz was selected for this example as a reasonable compromise between small size and high efficiency. The value of $R_T$ for 230 kHz switching frequency can be calculated from Equation 3 as follows:

$$R_T = \frac{5.2 \times 10^9}{230 \times 10^3} - 948 = 21.7\ k\Omega \tag{21}$$

A standard value of 22.1 kΩ was chosen for $R_T$.

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### 8.3.5 Output Inductor $L_O$

The maximum inductor ripple current occurs at the maximum input voltage. Typically, 20% to 40% of the full load current is a good compromise between core loss and copper loss of the inductor. Higher ripple current allows for a smaller inductor size, but places more of a burden on the output capacitor to smooth the ripple voltage on the output. For this example, a ripple current of 40% of 9 A was chosen. Knowing the switching frequency, maximum ripple current, maximum input voltage and the nominal output voltage, the inductor value can be calculated as follows:

$$L_O = \frac{V_{OUT}}{I_{PP(MAX)} \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) = \frac{12\,V}{9\,A \times 0.4 \times 230\,kHz} \times \left(1 - \frac{12\,V}{55\,V}\right) = 11.3\,\mu H \quad (22)$$

The closest standard value of 10 µH was chosen for $L_O$. Using the value of 10 µH for $L_O$, calculate $I_{PP}$ again. This step is necessary if the chosen value of $L_O$ differs significantly from the calculated value.

From Equation 11,

$$I_{PP(MAX)} = \frac{12V}{10\,\mu H \text{ x } 230\text{ kHz}} \text{ x } \left(1 - \frac{12V}{55V}\right) = 4.1A \quad (23)$$

At the minimum input voltage, this value is 1.04 A.

### 8.3.6 Diode Emulation Function

The DEMB pin is left floating since this example uses diode emulation to reduce the power loss under no load or light load conditions.

### 8.3.7 Current Sense Resistor $R_S$

The performance of the converter will vary depending on the K value. For this example, K = 1 was chosen to control sub-harmonic oscillation and achieve one-cycle damping. The maximum output current capability ($I_{OUT(MAX)}$) should be 20~50% higher than the required output current, to account for tolerances and ripple current. For this example, 130% of 9 A was chosen. The current sense resistor value can be calculated from Equation 9 and Equation 10 as follows:

$$R_S = \frac{V_{CS(TH)}}{I_{OUT(MAX)} + \frac{V_{OUT} \text{ x } K}{f_{SW} \text{ x } L_O} - \frac{I_{PP}}{2}} \; [\Omega] \quad (24)$$

$$R_S = \frac{0.12V}{9A \text{ x } 1.3 + \frac{12 \text{ x } 1}{230\text{ kHz x } 10\,\mu H} - \frac{1.04A}{2}} = 7.3\ m\Omega \quad (25)$$

A value of 7.41 mΩ was realized for $R_S$ by placing an additional 0.1-Ω sense resistor in parallel with 8 mΩ. The sense resistor must be rated to handle the power dissipation at maximum input voltage when current flows through the low-side NMOS for the majority of the PWM cycle. The maximum power dissipation of $R_S$ can be calculated as:

$$P_{RS} = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \text{ x } I_{OUT}{}^2 \text{ x } R_S \quad [W] \quad (26)$$

$$P_{RS} = \left(1 - \frac{12V}{55V}\right) \text{ x } 9A^2 \text{ x } 7.41\ m\Omega = 0.47W \quad (27)$$

The worst case peak inductor current under the output short condition can be calculated from Equation 12 as follows:

$$I_{LIM_PK} = \frac{0.12V}{7.41\ m\Omega} + \frac{55V \text{ x } 100\text{ ns}}{10\,\mu H} = 16.7A$$

where

- $t_{ON(MIN)}$ is normally 100ns (28)


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### 8.3.8 Current Sense Filter $R_{CS}$ and $C_{CS}$

The LM5117 itself is not affected by the large leading edge spike because it samples valley current just prior to the onset of the high-side switch. A current sense filter is used to minimize a noise injection from any external noise sources. In general, a current sense filter is not necessary. In this example, a current sense filter is not used

Adding $R_{CS}$ resistor changes the current sense amplifier gain which is defined as $A_S$=10 k / (1 k+$R_{CS}$). A small value of $R_{CS}$ resistor below 100 Ω is recommended to minimize the gain change which is caused by the temperature coefficient difference between internal and external resistors.

### 8.3.9 Ramp Resistor $R_{RAMP}$ and Ramp Capacitor $C_{RAMP}$

The positive slope of the inductor current ramp signal is emulated by $R_{RAMP}$ and $C_{RAMP}$. For this example, the value of $C_{RAMP}$ was set at the standard capacitor value of 820 pF. With the inductor, sense resistor and the K factor selected, the value of $R_{RAMP}$ can be calculated from Equation 4 as follows:

$$R_{RAMP} = \frac{L_O}{K \times C_{RAMP} \times R_S \times A_S} \ [\Omega] \tag{29}$$

$$R_{RAMP} = \frac{10\ \mu H}{1 \times 820\ pF \times 7.41\ m\Omega \times 10} = 165\ k\Omega \tag{30}$$

The standard value of 165 kΩ was selected for $R_{RAMP}$.

### 8.3.10 UVLO Divider $R_{UV2}$, $R_{UV1}$ and $C_{FT}$

The desired startup voltage and the hysteresis are set by the voltage divider $R_{UV1}$ and $R_{UV2}$. Capacitor $C_{FT}$ provides filtering for the divider. For this design, the startup voltage was set to 14 V, 1 V below $V_{IN(MIN)}$. $V_{HYS}$ was set to 2 V. The value of $R_{UV1}$, $R_{UV2}$ can be calculated from Equation 1 and Equation 2 as follows:

$$R_{UV2} = \frac{2V}{20\ \mu A} = 100\ k\Omega \tag{31}$$

$$R_{UV1} = \frac{1.25V \times 100\ k\Omega}{14V - 1.25V} = 9.8\ k\Omega \tag{32}$$

The standard value of 100 kΩ was selected for $R_{UV2}$. $R_{UV1}$ was selected to be 9.76 kΩ. A value of 47 pF was chosen for $C_{FT}$.

### 8.3.11 VCC Disable and External VCC Supply

The 12-V output voltage allows the external VCC supply configuration as shown in Figure 16. In this example, VCCDIS can be left floating since $V_{OUT}$ is higher than VCC regulator set-point level.

### 8.3.12 Power Switches $Q_H$ and $Q_L$

Selection of the power NMOS devices is governed by the same trade-offs as switching frequency. Breaking down the losses in the high-side and low-side NMOS devices is one way to compare the relative efficiencies of different devices. Losses in the power NMOS devices can be broken down into conduction loss, gate charging loss, and switching loss.

Conduction loss $P_{DC}$ is approximately:

$$P_{DC\ (High\text{-}Side)} = D \times (I_{OUT}^2 \times R_{DS(ON)} \times 1.3) \quad [W] \tag{33}$$

$$P_{DC\ (Low\text{-}Side)} = (1 - D) \times (I_{OUT}^2 \times R_{DS(ON)} \times 1.3) \quad [W]$$

where

- D is the duty cycle
- the factor of 1.3 accounts for the increase in the NMOS device on-resistance due to heating (34)

Alternatively, the factor of 1.3 can be eliminated and the high temperature on-resistance of the NMOS device can be estimated using the $R_{DS(ON)}$ vs Temperature curves in the MOSFET datasheet.

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Gate charging loss ($P_{GC}$) results from the current driving the gate capacitance of the power NMOS devices and is approximated as:

$$P_{GC} = n \times V_{VCC} \times Q_g \times f_{SW} \quad [W] \tag{35}$$

Qg refers to the total gate charge of an individual NMOS device, and 'n' is the number of NMOS devices. Gate charge loss differs from conduction and switching losses in that the actual dissipation occurs in the controller IC. Switching loss ($P_{SW}$) occurs during the brief transition period as the high-side NMOS device turns on and off. During the transition period both current and voltage are present in the channel of the NMOS device. The switching loss can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW} \quad [W] \tag{36}$$

$t_R$ and $t_F$ are the rise and fall times of the high-side NMOS device. The rise and fall times are usually mentioned in the MOSFET datasheet or can be empirically observed with an oscilloscope. Switching loss is calculated for the high-side NMOS device only. Switching loss in the low-side NMOS device is negligible because the body diode of the low-side NMOS device turns on before and after the low-side NMOS device switches. For this example, the maximum drain-to-source voltage applied to either NMOS device is 55 V. The selected NMOS devices must be able to withstand 55 V plus any ringing from drain to source and must be able to handle at least the VCC voltage plus any ringing from gate to source.

### 8.3.13 Snubber Components $R_{SNB}$ and $C_{SNB}$

A resistor-capacitor snubber network across the low-side NMOS device reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and can couple noise to the output voltage. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. Start with a resistor value between 5 and 50 Ω. Increasing the value of the snubber capacitor results in more damping, but higher snubber losses. Select a minimum value for the snubber capacitor that provides adequate damping of the spikes on the switch waveform at heavy load. A snubber may not be necessary with an optimized layout.

### 8.3.14 Bootstrap Capacitor $C_{HB}$ and Bootstrap Diode $D_{HB}$

The bootstrap capacitor between the HB and SW pin supplies the gate current to charge the high-side NMOS device gate during each cycle's turn-on and also supplies recovery charge for the bootstrap diode. These current peaks can be several amperes. The recommended value of the bootstrap capacitor is at least 0.1 µF. $C_{HB}$ should be a good quality, low ESR, ceramic capacitor located at the pins of the IC to minimize potentially damaging voltage transients caused by trace inductance. The absolute minimum value for the bootstrap capacitor is calculated as:

$$C_{HB} \geq \frac{Q_g}{\Delta V_{HB}} \quad [F] \tag{37}$$

where

- Qg is the high-side NMOS gate charge
- $\Delta V_{HB}$ is the tolerable voltage droop on $C_{HB}$, which is typically less than 5% of VCC or 0.15 V conservatively

A value of 0.47 µF was selected for this design.

### 8.3.15 VCC Capacitor $C_{VCC}$

The primary purpose of the VCC capacitor ($C_{VCC}$) is to supply the peak transient currents of the LO driver and bootstrap diode as well as provide stability for the VCC regulator. These peak currents can be several amperes. The recommended value of $C_{VCC}$ should be no smaller than 0.47µF, and should be a good quality, low ESR, ceramic capacitor. $C_{VCC}$ should be placed at the pins of the IC to minimize potentially damaging voltage transients caused by trace inductance. A value of 1 µF was selected for this design.


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### 8.3.16 Output Capacitor $C_O$

The output capacitors smooth the output voltage ripple caused by inductor ripple current and provide a source of charge during transient loading conditions. For this design example, a 470-µF electrolytic capacitor with maximum 20mΩ ESR was selected as the main output capacitor. The fundamental component of the output ripple voltage with maximum ESR is approximated as:

$$\Delta V_{OUT} = I_{PP} \times \sqrt{R_{ESR}^2 + \left(\frac{1}{8 \times f_{SW} \times C_{OUT}}\right)^2} \quad [V] \tag{38}$$

$$\Delta V_{OUT} = 4.1 \times \sqrt{0.02\Omega^2 + \left(\frac{1}{8 \times 230\ kHz \times 470\ \mu F}\right)^2} = 82\ mV \tag{39}$$

Additional low ERS / ESL ceramic capacitors can be placed in parallel with the main output capacitor to further reduce the output voltage ripple and spikes. In this example, two 22µF capacitors were added.

### 8.3.17 Input Capacitor $C_{IN}$

The regulator input supply voltage typically has high source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. When the high-side NMOS device turns on, the current into the device steps to the valley of the inductor current waveform, ramps up to the peak value, and then drops to the zero at turnoff. The input capacitor should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating necessary is $I_{RMS} > I_{OUT} / 2$.

In this example, seven 3.3µF ceramic capacitors were used. With ceramic capacitors, the input ripple voltage will be triangular. The input ripple voltage can be approximated as:

$$\Delta V_{IN} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}} \quad [V] \tag{40}$$

$$\Delta V_{IN} = \frac{9\ A}{4 \times 230\ kHz \times 3.3\ \mu F \times 7} = 0.42\ V \tag{41}$$

Capacitors connected in parallel should be evaluated for RMS current rating. The current will split between the input capacitors based on the relative impedance of the capacitors at the switching frequency.

### 8.3.18 VIN Filter $R_{VIN}$, $C_{VIN}$

An R-C filter ($R_{VIN}$, $C_{VIN}$) on VIN is optional. The filter helps to prevent faults caused by high frequency switching noise injection into the VIN pin. A 0.47-µF ceramic capacitor is used for $C_{VIN}$ in the example. $R_{VIN}$ is selected to be 3.9 Ω.

### 8.3.19 Soft-Start Capacitor $C_{SS}$

The capacitor at the SS pin ($C_{SS}$) determines the soft-start time ($t_{SS}$), which is the time for the output voltage to reach the final regulated value. The $t_{SS}$ for a given $C_{SS}$ can be calculated from Equation 8 as follows:

$$t_{SS} = \frac{0.1\ \mu F \times 0.8V}{10\ \mu A} = 8\ ms \tag{42}$$

For this example, a value of 0.1 µF was chosen for a soft-start time of 8 ms.

### 8.3.20 Restart Capacitor $C_{RES}$

The capacitor at the RES pin ($C_{RES}$) determines $t_{RES}$, which is the time the LM5117 remains off before a restart attempt is made in hiccup mode current limiting. $t_{RES}$ for a given $C_{RES}$ can be calculated from Equation 13 as follows:

$$t_{RES} = \frac{0.47\ \mu F \times 1.25V}{10\ \mu A} = 59\ ms \tag{43}$$

For this example, a value of 0.47 µF was chosen for a restart time of 59 ms.

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### 8.3.21 Output Voltage Divider $R_{FB2}$ and $R_{FB1}$

$R_{FB1}$ and $R_{FB2}$ set the output voltage level. The ratio of these resistors is calculated as:

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{0.8V} - 1 \quad (44)$$

The ratio between $R_{COMP}$ and $R_{FB2}$ determines the mid-band gain, $A_{FB_MID}$. A larger value for $R_{FB2}$ may require a corresponding larger value for $R_{COMP}$. $R_{FB2}$ should be large enough to keep the total divider power dissipation small. 4.99 kΩ was chosen for $R_{FB2}$ in this example, which results in a $R_{FB1}$ value of 357 Ω for 12-V output.

### 8.3.22 Loop Compensation Components $C_{COMP}$, $R_{COMP}$ and $C_{HF}$

$R_{COMP}$, $C_{COMP}$ and $C_{HF}$ configure the error amplifier gain and phase characteristics to produce a stable voltage loop. For a quick start, follow the 4 steps listed below.

**STEP1: Select $f_{CROSS}$**

By selecting one tenth of the switching frequency, $f_{CROSS}$ is calculated as follows:

$$f_{CROSS} = \frac{f_{SW}}{10} = 23 \text{ kHz} \quad (45)$$

**STEP2: Determine required $R_{COMP}$**

Knowing $f_{CROSS}$, $R_{COMP}$ is calculated as follows:

$$R_{COMP} = 2\pi \times R_S \times A_S \times C_{OUT} \times R_{FB2} \times f_{CROSS} \quad [\Omega] \quad (46)$$

$$R_{COMP} = 2\pi \times 7.41\ m\Omega \times 10 \times 514\ \mu F \times 4.99\ k\Omega \times 23\ kHz = 27.5\ k\Omega \quad (47)$$

The standard value of 27.4kΩ was selected for $R_{COMP}$

**STEP3: Determine $C_{COMP}$ to cancel load pole**

Knowing $R_{COMP}$, $C_{COMP}$ is calculated as follows:

$$C_{COMP} = \frac{R_{LOAD} \times C_{OUT}}{R_{COMP}} = \frac{\left(\frac{12\,V}{9\,A}\right) \times 514\,\mu F}{27.4\,k\Omega} = 25\,nF \quad (48)$$

The standard value of 22nF was selected for $C_{COMP}$

**STEP4: Determine $C_{HF}$ to cancel ESR zero**

Knowing $R_{COMP}$ and $C_{COMP}$, $C_{HF}$ is calculated as follows:

$$C_{HF} = \frac{R_{ESR} \times C_{OUT} \times C_{COMP}}{R_{COMP} \times C_{COMP} - R_{ESR} \times C_{OUT}} \quad [F] \quad (49)$$

$$C_{HF} = \frac{10\ m\Omega \times 514\ \mu F \times 22\ nF}{27.4k\Omega \times 22\ nF - 10\ m\Omega \times 514\ \mu F} = 189\ pF \quad (50)$$

Half of the maximum ESR is assumed as a typical ESR. The standard value of 180pF was selected for $C_{HF}$.


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**Table 1. LM5117 Frequency Analysis Formulas**

| | SIMPLE FORMULA | COMPREHENSIVE FORMULA (1) |
|---|---|---|
| **MODULATOR TRANSFER FUNCTION** | $\frac{\hat{V}_{OUT}}{\hat{V}_{COMP}} = A_M \times \frac{1 + \frac{s}{\omega_{Z_ESR}}}{\left(1 + \frac{s}{\omega_{P_LF}}\right)}$ | $\frac{\hat{V}_{OUT}}{\hat{V}_{COMP}} = A_M \times \frac{1 + \frac{s}{\omega_{Z_ESR}}}{\left(1 + \frac{s}{\omega_{P_LF}}\right) \times \left(1 + \frac{s}{\omega_{P_ESR}}\right) \times \left(1 + \frac{s}{\omega_{P_HF}} + \frac{s^2}{\omega_n{}^2}\right)}$ |
| Modulator DC Gain | $A_M = \frac{R_{LOAD}}{R_S \times A_S}$ | $A_M = \frac{R_{LOAD}}{R_S \times A_S} \times \frac{1}{1 + \frac{R_{LOAD}}{\omega_{P_HF} \times L_O}}$ |
| ESR Zero | $\omega_{Z_ESR} = \frac{1}{R_{ESR} \times C_{OUT}}$ | $\omega_{Z_ESR} = \frac{1}{R_{ESR1} \times C_{OUT1}}$ |
| ESR Pole | Not considered | $\omega_{P_ESR} = \frac{1}{R_{ESR1} \times (C_{OUT1} // C_{OUT2})}$ |
| Dominant Load Pole | $\omega_{P_LF} = \frac{1}{R_{LOAD} \times C_{OUT}}$ | $\omega_{P_LF} = \frac{1}{(R_{LOAD} + R_{ESR1}) \times (C_{OUT1} + C_{OUT2})} + \frac{1}{L_O \times (C_{OUT1} + C_{OUT2}) \times \omega_{P_HF}}$ |
| Sampled Gain Inductor Pole | Not considered | $\omega_{P_HF} = \frac{f_{SW}}{K - 0.5}$ or $\omega_{P_HF} = Q \times \omega_n$ |
| Quality Factor | Not considered | $Q = \frac{1}{\pi(K - 0.5)}$ |
| Sub-harmonic Double Pole | Not considered | $\omega_n = \frac{\omega_{SW}}{2} = \pi \times f_{SW}$ or $f_n = \frac{f_{SW}}{2}$ |
| K Factor | $K = 1$ | $K = \frac{L_O}{R_{RAMP} \times C_{RAMP} \times R_S \times A_S}$ |
| **FEEDBACK TRANSFER FUNCTION** | $-\frac{\hat{V}_{COMP}}{\hat{V}_{OUT}} = A_{FB} \times \frac{1 + \frac{s}{\omega_{Z_EA}}}{s \times \left(1 + \frac{s}{\omega_{P_EA}}\right)}$ | $-\frac{\hat{V}_{COMP}}{\hat{V}_{OUT}} = A_{FB} \times \frac{1 + \frac{s}{\omega_{Z_EA}}}{s \times \left(1 + \frac{s}{\omega_{P_EA}}\right)}$ |
| Feedback DC Gain | $A_{FB} = \frac{1}{R_{FB2} \times (C_{COMP} + C_{HF})}$ | $A_{FB} = \frac{1}{R_{FB2} \times (C_{COMP} + C_{HF})}$ |
| Mid-band Gain | $A_{FB_MID} = \frac{R_{COMP}}{R_{FB2}}$ | $A_{FB_MID} = \frac{R_{COMP}}{R_{FB2}}$ |
| Low Frequency Zero | $\omega_{Z_EA} = \frac{1}{R_{COMP} \times C_{COMP}}$ | $\omega_{Z_EA} = \frac{1}{R_{COMP} \times C_{COMP}}$ |
| High Frequency Pole | $\omega_{P_EA} = \frac{1}{R_{COMP} \times C_{HF}}$ | $\omega_{P_EA} = \frac{1}{R_{COMP} \times (C_{HF} // C_{COMP})}$ |

(1) Comprehensive Equation includes an inductor pole and a gain peaking at $f_{SW}/2$, which caused by sampling effect of the current mode control. Also it assumes that a ceramic capacitor $C_{OUT2}$ (No ESR) is connected in parallel with $C_{OUT1}$. $R_{ESR1}$ represents ESR of $C_{OUT1}$ .

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**Table 1. LM5117 Frequency Analysis Formulas (continued)**

| | SIMPLE FORMULA | COMPREHENSIVE FORMULA (1) |
|---|---|---|
| **OPEN-LOOP RESPONSE** | $T(s) = A_M \times A_{FB} \times \frac{1 + \frac{s}{\omega_{Z_ESR}}}{\left(1 + \frac{s}{\omega_{P_LF}}\right)} \times \frac{1 + \frac{s}{\omega_{Z_EA}}}{s \times \left(1 + \frac{s}{\omega_{P_EA}}\right)}$ | $T(s) = A_M \times A_{FB} \times \frac{1 + \frac{s}{\omega_{Z_ESR}}}{\left(1 + \frac{s}{\omega_{P_LF}}\right) \times \left(1 + \frac{s}{\omega_{P_ESR}}\right) \times \left(1 + \frac{s}{\omega_{P_HF}} + \frac{s^2}{\omega_n^2}\right)} \times \frac{1 + \frac{s}{\omega_{Z_EA}}}{s \times \left(1 + \frac{s}{\omega_{P_EA}}\right)}$ |
| | $T(s) = \frac{A_M \times A_{FB}}{s}$ when $\omega_{Z_EA} = \omega_{P_LF}$ & $\omega_{P_EA} = \omega_{Z_ESR}$ | $T(s) = \frac{A_M \times A_{FB}}{s} \times \frac{1 + \frac{s}{\omega_{Z_ESR}}}{\left(1 + \frac{s}{\omega_{P_EA}}\right) \times \left(1 + \frac{s}{\omega_{P_ESR}}\right) \times \left(1 + \frac{s}{\omega_{P_HF}} + \frac{s^2}{\omega_n^2}\right)}$ when $\omega_{Z_EA} = \omega_{P_LF}$ |
| Cross Over Frequency (Open Loop Bandwidth) | $f_{CROSS} = \frac{R_{COMP}}{2 \times \pi \times R_S \times R_{FB2} \times A_S \times C_{OUT}}$ when $\omega_{Z_EA} = \omega_{P_LF}$ & $\omega_{P_EA} = \omega_{Z_ESR}$ | $f_{CROSS} = \frac{R_{COMP}}{2 \times \pi \times R_S \times R_{FB2} \times A_S \times (C_{OUT1} + C_{OUT2})}$ when $\omega_{Z_EA} = \omega_{P_LF}$ & $\omega_{P_EA} = \omega_{Z_ESR}$ & $f_{CROSS} < \frac{\omega_{P_HF}}{2 \times \pi \times 10}$ & $f_{CROSS} < \frac{\omega_{P_ESR}}{2 \times \pi \times 10}$ |
| Maximum Cross Over Frequency | $f_{CROSS_MAX} = \frac{f_{SW}}{5}$ | $f_{CROSS_MAX} = \frac{f_{SW}}{4 \times Q} \times \left(\sqrt{1 + 4 \times Q^2} - 1\right)$ The frequency at which 45° phase shift occurs in modulator phase characteristics. |

## 8.4 Application Curves

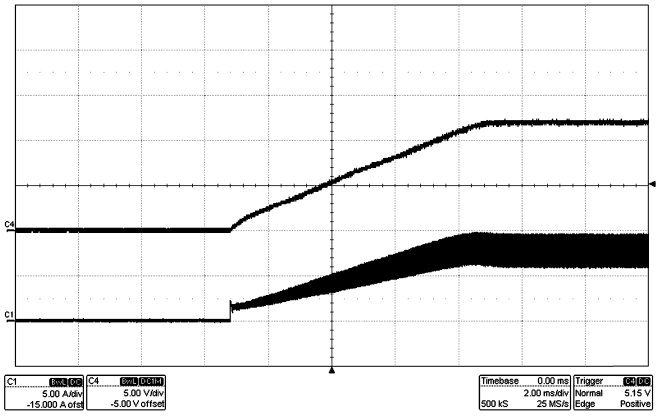


**Figure 33. Start-Up with Resistive Load**

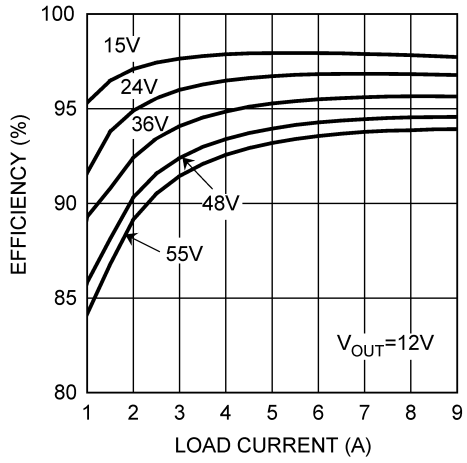


**Figure 34. Typical Efficiency vs Load Current**


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## Application Curves (continued)

### 8.4.1 Constant Current Regulator

The LM5117 can be configured as a constant current regulator by using the current monitor feature (CM) as the feedback input. A voltage divider at the VCCDIS pin from VOUT to AGND can be used to protect against output over-voltage. When the VCCDIS pin voltage is greater than the VCCDIS threshold, the controller disables the VCC regulator and the VCC pin voltage decays. When the VCC pin voltage is less than the VCC UV threshold, both HO and LO outputs stop switching. Due to the time delay required for VCC to decay below the VCC UV threshold, the over-voltage protection operates in hiccup mode. See Figure 35.

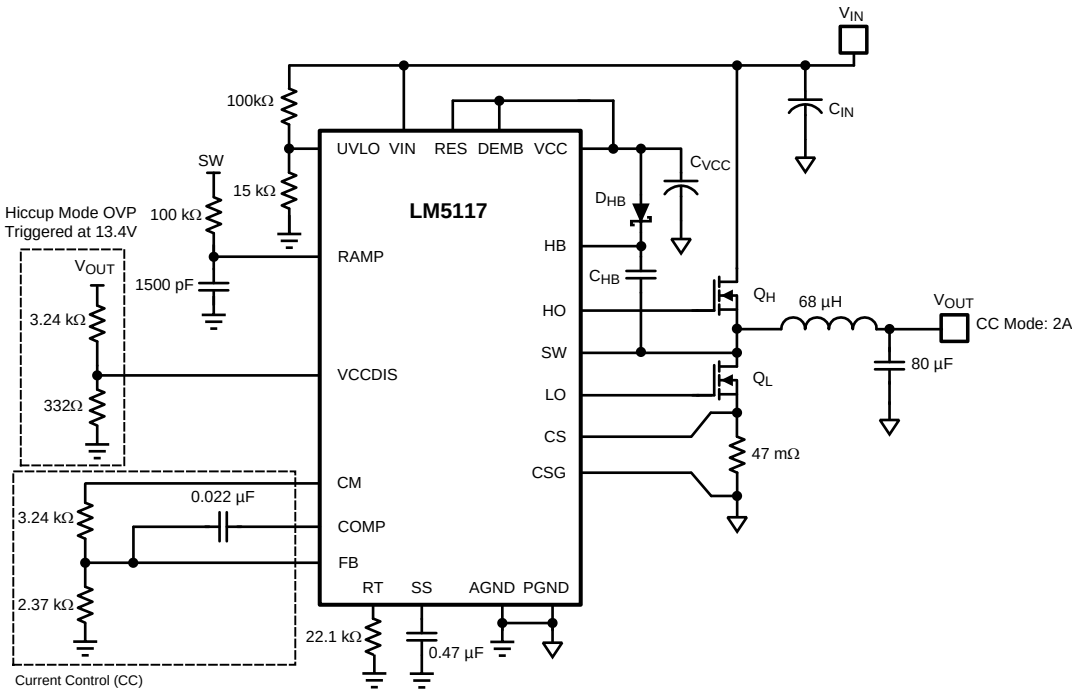


**Figure 35. Constant Current Regulator With Hiccup Mode Output OVP**

### 8.4.2 Constant Voltage and Constant Current Regulator

The LM5117 also can be configured as a constant voltage and constant current regulator, known as CV+CC regulator. In this configuration, there is much less variation in the current limiting as compared to peak cycle-by-cycle current limiting of the inductor current. The LMV431 and the PNP transistor create a voltage-to-current amplifier in the current loop. This amplifier circuitry does not affect the normal operation when the output current is less than the current limit set-point. When the output current is greater than the set-point, the PNP transistor sources a current into $C_{RAMP}$ and increases the positive slope of emulated inductor current ramp until the output current is less than or equal to the current limit set-point. See Figure 36 and Figure 37.

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## Application Curves (continued)

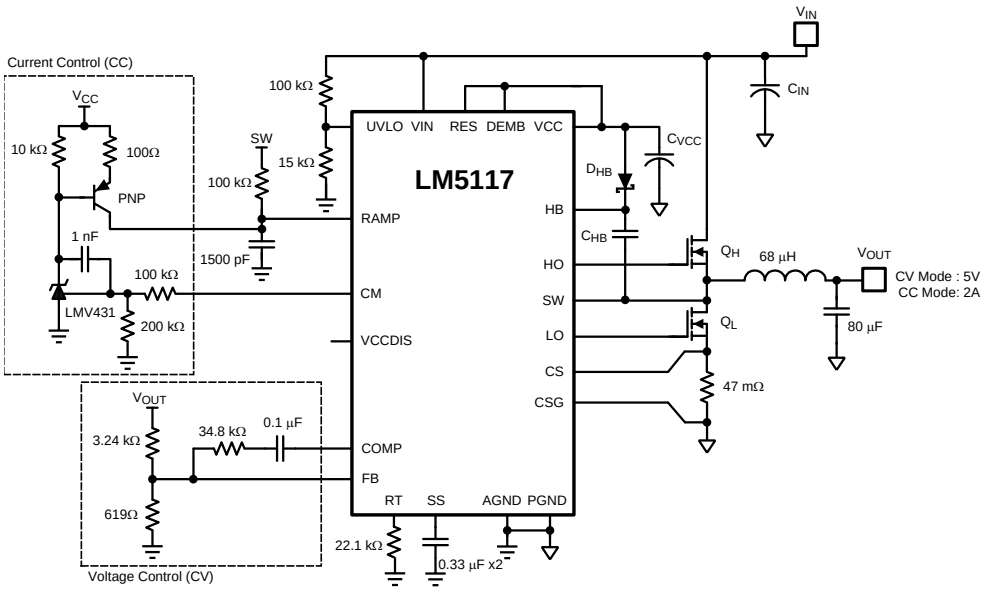


**Figure 36. Constant Voltage Regulator with Accurate Current Limit**

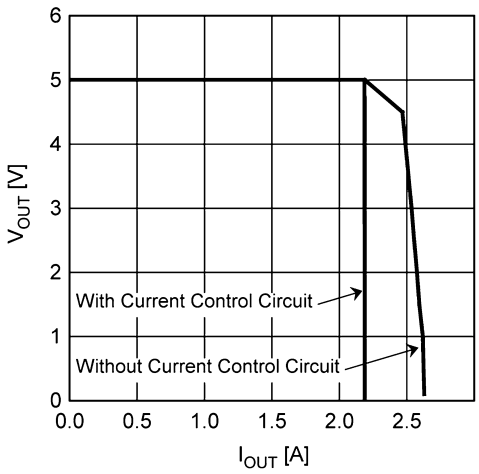


**Figure 37. Current Limit Comparison**


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# 9 Power Supply Recommendations

The LM5117 is a power management device. The power supply for the device is any DC voltage source within the specified input range.

# 10 Layout

## 10.1 Layout Guideline

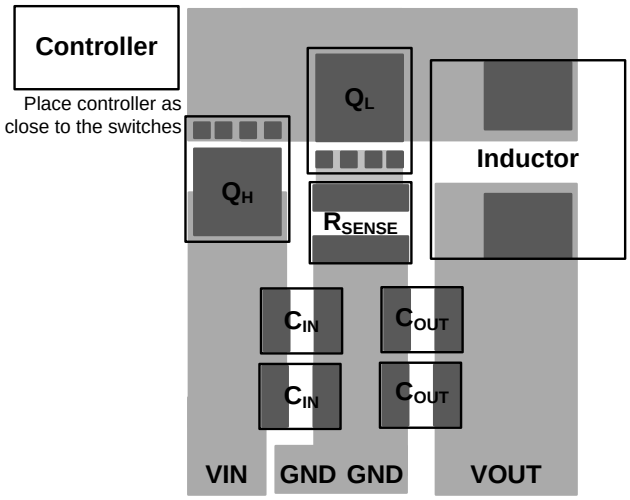


**Figure 38. Layout Example**

### 10.1.1 PC Board Layout Recommendation

In a buck regulator the primary switching loop consists of the input capacitor, NMOS power switches and current sense resistor. Minimizing the area of this loop reduces the stray inductance and minimizes noise and possible erratic operation. High quality input capacitors should be placed as close as possible to the NMOS power switches, with the $V_{IN}$ side of the capacitor connected directly to the high-side NMOS drain and the ground side of the capacitor connected as close as possible to the current sense resistor ground connection.

Connect all of the low power ground connections ($R_{UV1}$, $R_T$, $R_{FB1}$, $C_{SS}$, $C_{RES}$, $C_{CM}$, $C_{VIN}$, $C_{RAMP}$) directly to the regulator AGND pin. Connect $C_{VCC}$ directly to the regulator PGND pin. Note that $C_{VIN}$ and $C_{VCC}$ must be as physically close as possible to the IC. AGND and PGND must be directly connected together through a top-side copper pattern connected to the exposed pad. Ensure no high current flows beneath the underside exposed pad.

The LM5117 has an exposed thermal pad to aid power dissipation. Adding several vias under the exposed pad helps conduct heat away from the IC. The junction to ambient thermal resistance varies with application. The most significant variables are the area of copper in the PC board, the number of vias under the exposed pad and the amount of forced air cooling. The integrity of the solder connection from the IC exposed pad to the PC board is critical. Excessive voids greatly decrease the thermal dissipation capacity.

The highest power dissipating components are the two power switches. Selecting NMOS switches with exposed pads aids the power dissipation of these devices.

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# 11 Device and Documentation Support

## 11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| LM5117 | Click here | Click here | Click here | Click here | Click here |
| LM5117-Q1 | Click here | Click here | Click here | Click here | Click here |

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM5117PMH/NOPB | ACTIVE | HTSSOP | PWP | 20 | 73 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 125 | LM5117 PMH | Samples |
| LM5117PMHE/NOPB | ACTIVE | HTSSOP | PWP | 20 | 250 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 125 | LM5117 PMH | Samples |
| LM5117PMHX/NOPB | ACTIVE | HTSSOP | PWP | 20 | 2500 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 125 | LM5117 PMH | Samples |
| LM5117PSQ/NOPB | ACTIVE | WQFN | RTW | 24 | 1000 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | L5117P | Samples |
| LM5117PSQE/NOPB | ACTIVE | WQFN | RTW | 24 | 250 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | L5117P | Samples |
| LM5117PSQX/NOPB | ACTIVE | WQFN | RTW | 24 | 4500 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | L5117P | Samples |
| LM5117QPMH/NOPB | ACTIVE | HTSSOP | PWP | 20 | 73 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 125 | LM5117 QMH | Samples |
| LM5117QPMHE/NOPB | ACTIVE | HTSSOP | PWP | 20 | 250 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 125 | LM5117 QMH | Samples |
| LM5117QPMHX/NOPB | ACTIVE | HTSSOP | PWP | 20 | 2500 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 125 | LM5117 QMH | Samples |
| LM5117QPSQ/NOPB | ACTIVE | WQFN | RTW | 24 | 1000 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | L5117Q | Samples |
| LM5117QPSQE/NOPB | ACTIVE | WQFN | RTW | 24 | 250 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | L5117Q | Samples |
| LM5117QPSQX/NOPB | ACTIVE | WQFN | RTW | 24 | 4500 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | L5117Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF LM5117, LM5117-Q1 :**

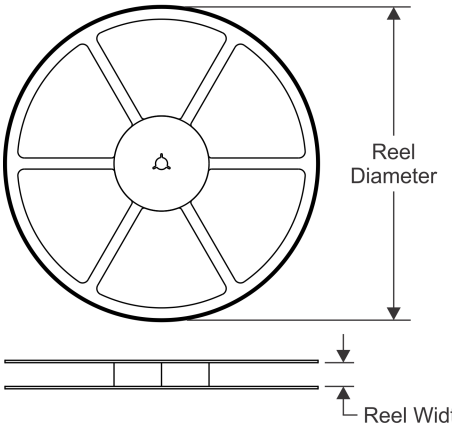
- Catalog: LM5117
- Automotive: LM5117-Q1

NOTE: Qualified Version Definitions:

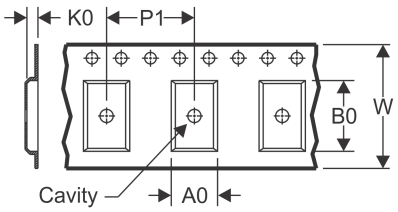
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

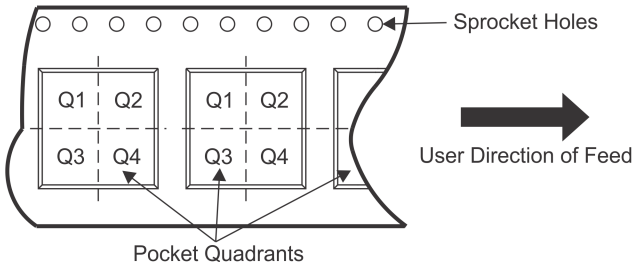



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

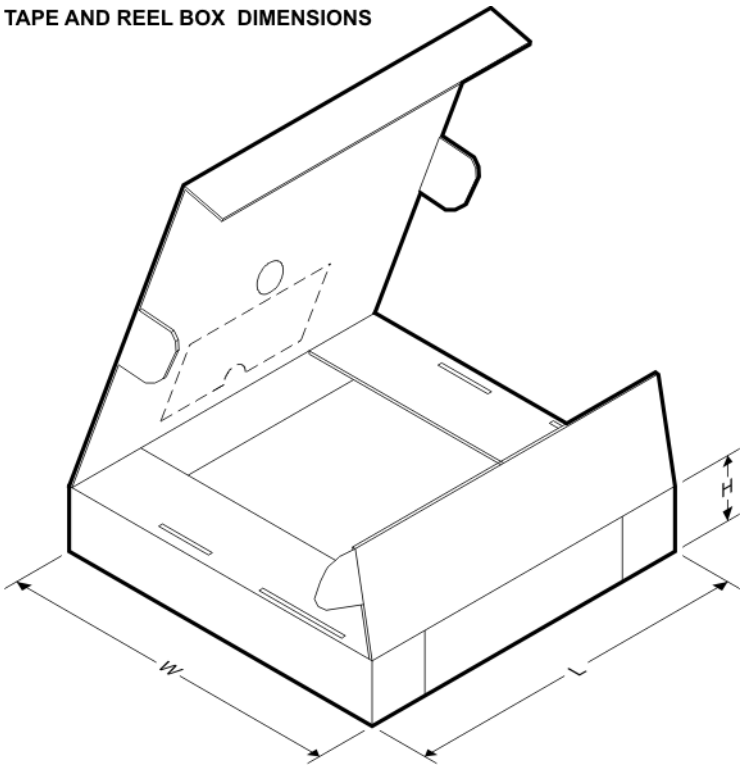
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM5117PMHE/NOPB | HTSSOP | PWP | 20 | 250 | 178.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| LM5117PMHX/NOPB | HTSSOP | PWP | 20 | 2500 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| LM5117PSQ/NOPB | WQFN | RTW | 24 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LM5117PSQE/NOPB | WQFN | RTW | 24 | 250 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LM5117PSQX/NOPB | WQFN | RTW | 24 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LM5117QPMHE/NOPB | HTSSOP | PWP | 20 | 250 | 178.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| LM5117QPMHX/NOPB | HTSSOP | PWP | 20 | 2500 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| LM5117QPSQ/NOPB | WQFN | RTW | 24 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LM5117QPSQE/NOPB | WQFN | RTW | 24 | 250 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LM5117QPSQX/NOPB | WQFN | RTW | 24 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

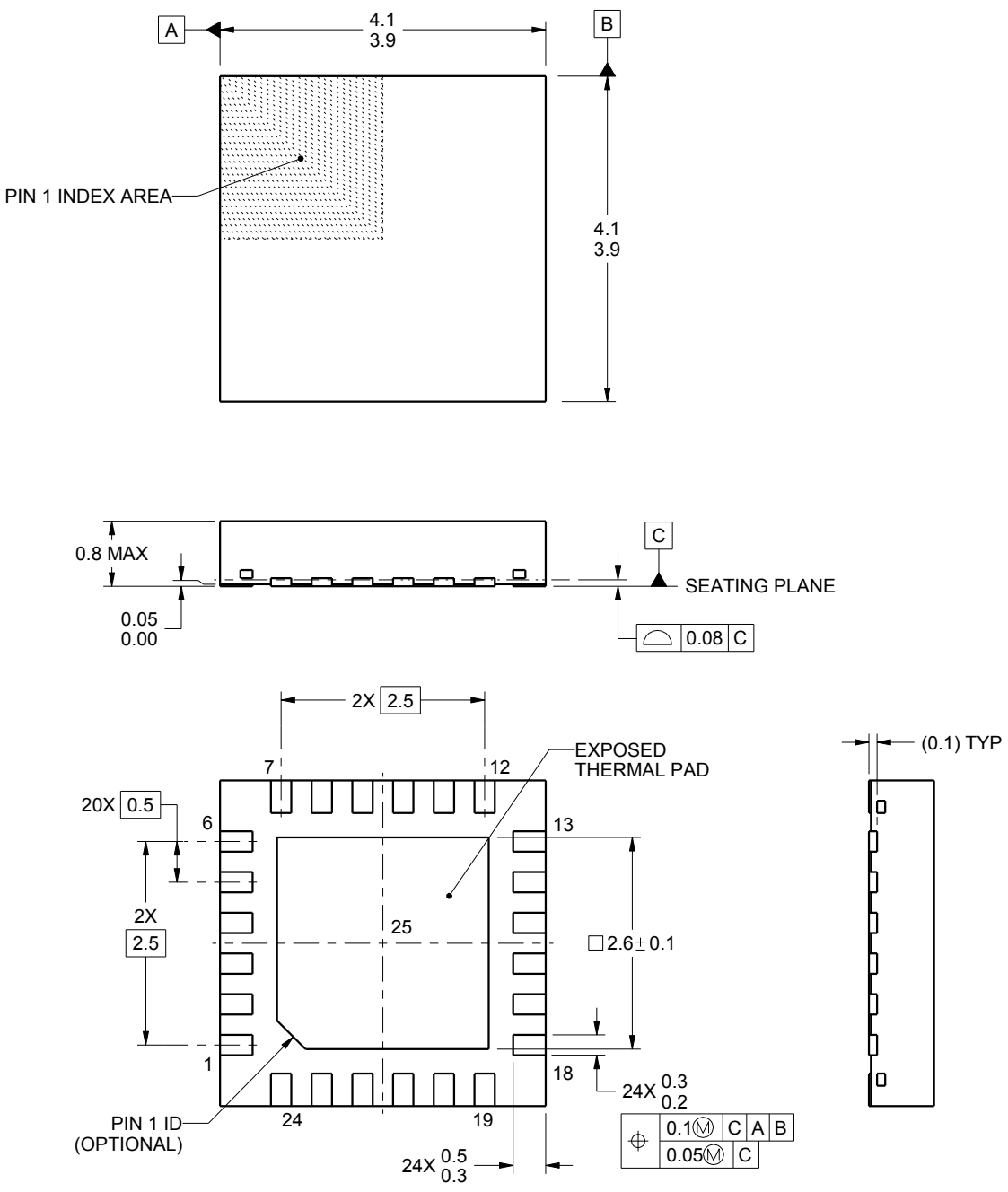
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM5117PMHE/NOPB | HTSSOP | PWP | 20 | 250 | 210.0 | 185.0 | 35.0 |
| LM5117PMHX/NOPB | HTSSOP | PWP | 20 | 2500 | 367.0 | 367.0 | 38.0 |
| LM5117PSQ/NOPB | WQFN | RTW | 24 | 1000 | 210.0 | 185.0 | 35.0 |
| LM5117PSQE/NOPB | WQFN | RTW | 24 | 250 | 210.0 | 185.0 | 35.0 |
| LM5117PSQX/NOPB | WQFN | RTW | 24 | 4500 | 367.0 | 367.0 | 35.0 |
| LM5117QPMHE/NOPB | HTSSOP | PWP | 20 | 250 | 210.0 | 185.0 | 35.0 |
| LM5117QPMHX/NOPB | HTSSOP | PWP | 20 | 2500 | 367.0 | 367.0 | 38.0 |
| LM5117QPSQ/NOPB | WQFN | RTW | 24 | 1000 | 210.0 | 185.0 | 35.0 |
| LM5117QPSQE/NOPB | WQFN | RTW | 24 | 250 | 210.0 | 185.0 | 35.0 |
| LM5117QPSQX/NOPB | WQFN | RTW | 24 | 4500 | 367.0 | 367.0 | 35.0 |

# PACKAGE OUTLINE

## RTW0024A

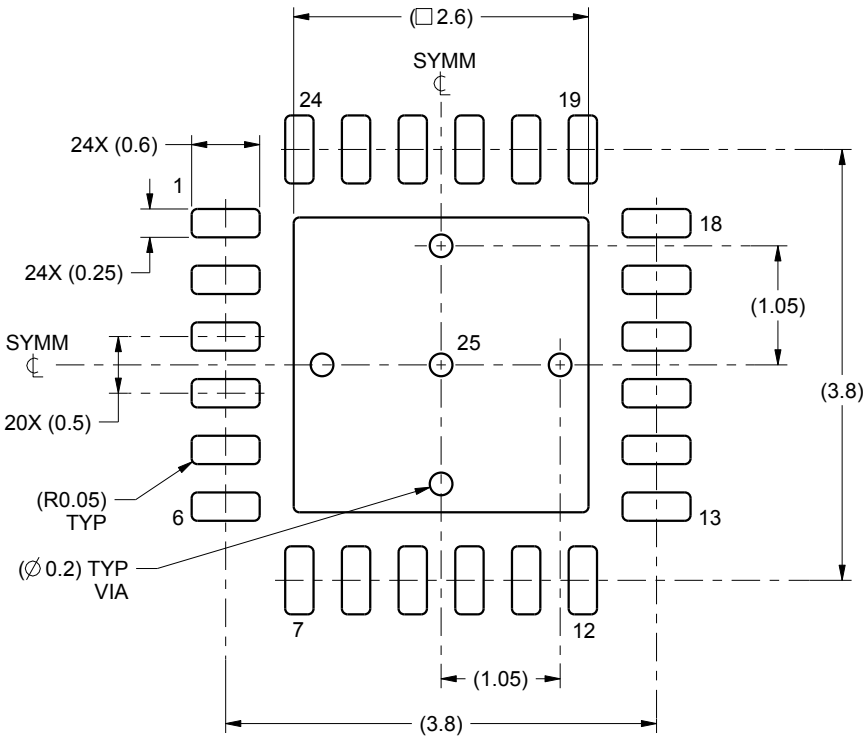
## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

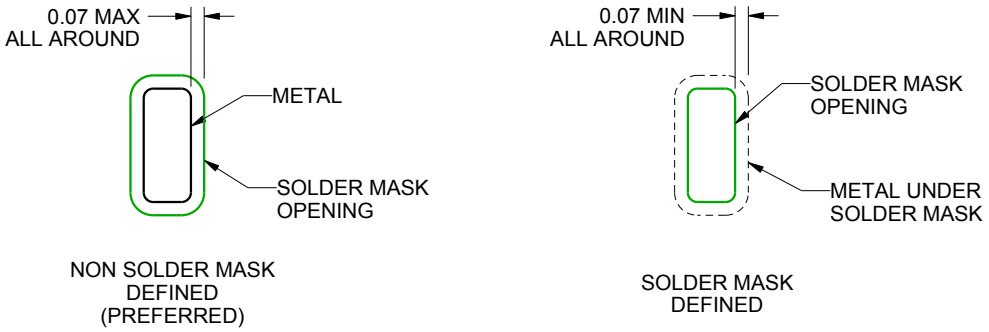



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:15X




SOLDER MASK DETAILS

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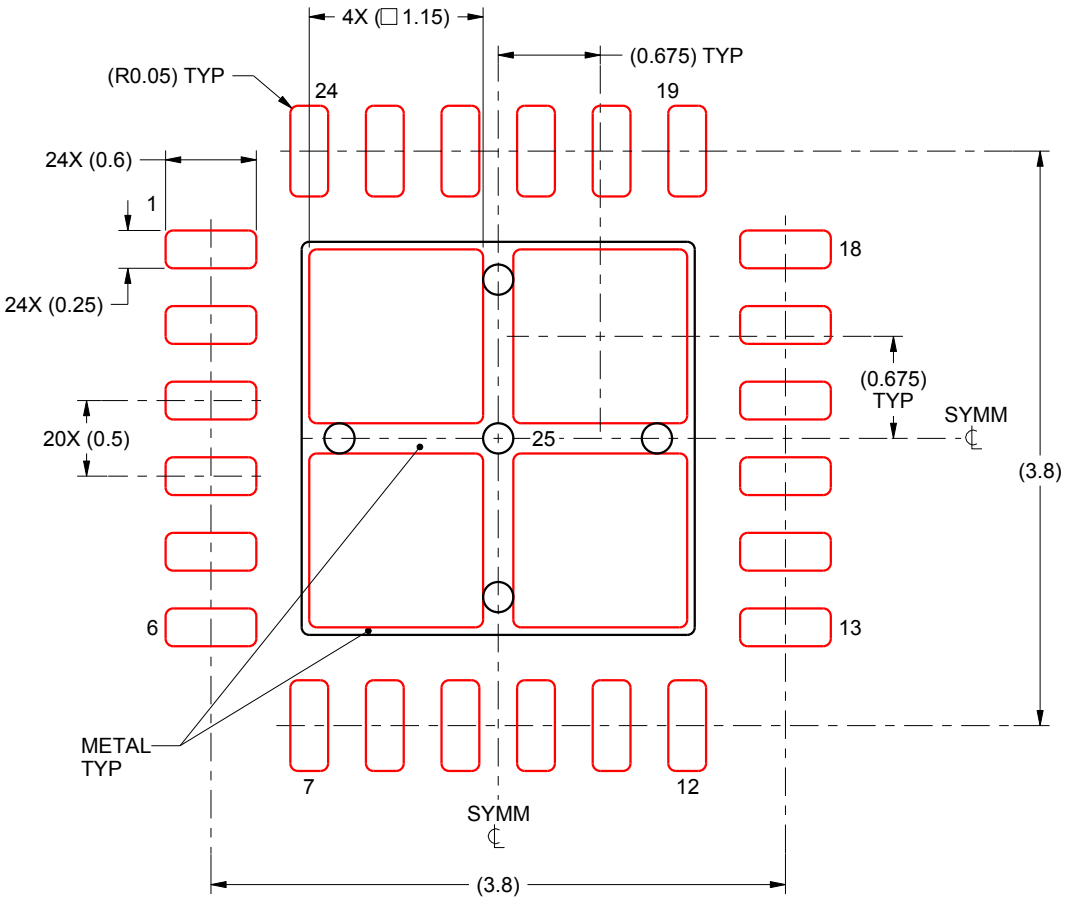
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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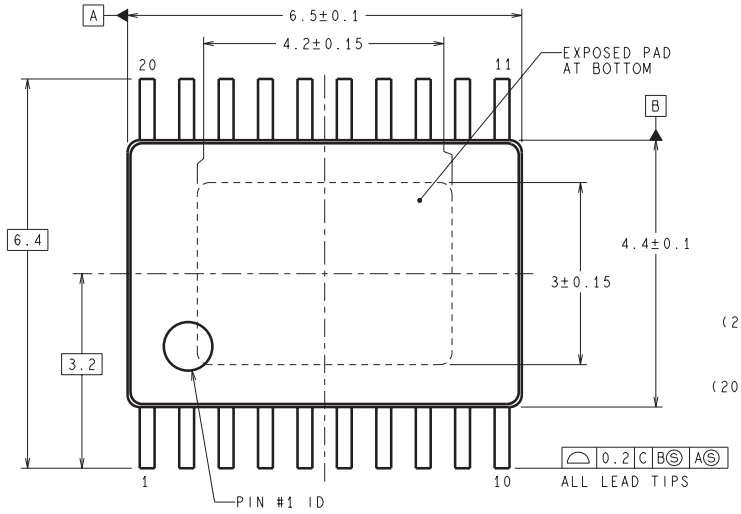
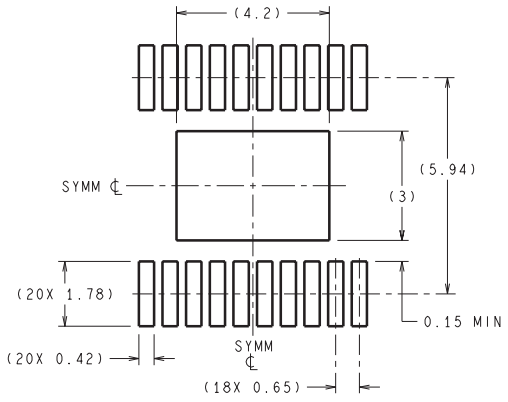
NOTES: (continued)

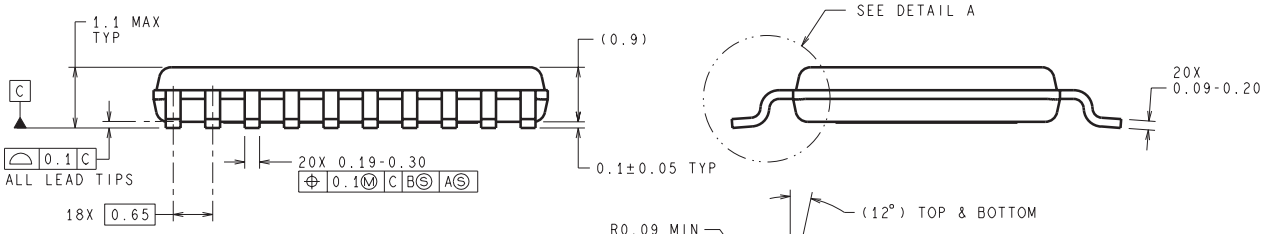
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PWP0020A

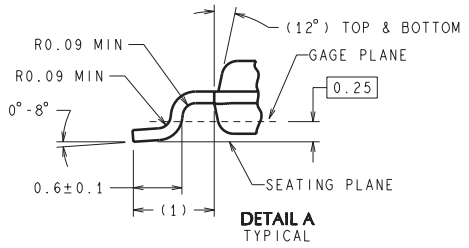



RECOMMENDED LAND PATTERN




DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY




DETAIL A
TYPICAL

MXA20A (Rev C)

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