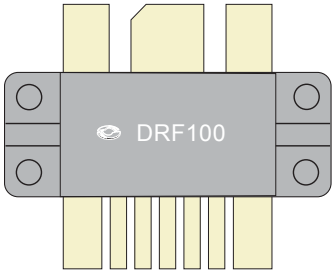
DRF100

15V, 8A, 30MHz

MOSFET Driver Hvbrid

The DRF100 is a High-Speed Power MOSFET driver with a unique anti-ring function. It is intended to drive the gate of a power MOSFET with ≥3nF gate capacitance to 15V at frequencies up to 30MHz. It can produce output currents ≥8A RMS, while dissipating 60W. The Driver output can be configured as Inverting or Non-Inverting.



FEATURES

- **Switching Frequency: DC TO 30MHz**
- **Low Pulse Width Distortion**
- **Single Power Supply**
- **1V CMOS Schmitt Trigger Input 1V Hysteresis**
- **Inverting Non-Inverting Select**
- **RoHS Compliant**
- **Output Capable of ≥ 8A RMS**
- **Power Dissipation Capability 60W**

TYPICAL APPLICATIONS

- **MOSFET Drivers**
- **Switch Mode Power Amplifiers**
- **Digital Output Amplifiers**
- **Pulse Generators**
- **Laser Diode Drivers**
- **Ultrasound Transducer Drivers**
- **Acoustic Optical Modulators**

Driver Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage			15	V
IN	Input Single Voltages			-.7 to +5.5	
$I_{O\,PK}$	Output Current Peak			8	A
T_{JMAX}	Operating Temperature			175	°C

Driver Specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	10		15	V
IN	Input Voltage	3		5.5	
$IN_{(R)}$	Input Voltage Rising Edge		3		ns
$IN_{(F)}$	Input Voltage Falling Edge		3		
I_{DDQ}	Quiescent Current		2		mA
I_O	Output Current		8		A
C_{oss}	Output Capacitance		2500		pF
C_{iss}	Input Capacitance		3		
R_{IN}	Input Parallel Resistance		1		MΩ
$V_{T(ON)}$	Input, Low to High Out (See truth table)	2.0		2.8	V
$V_{T(OFF)}$	Input, High to Low Out (See truth table)	1.0		1.4	
T_{DLY}	Time Delay (throughput)	25		38	ns
t_r	Rise Time	1.5	2.5	3.0	ns
t_f	Fall Time	1.5	2.5	3.0	
T_D	Prop. Delay		35		

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Output Characteristics

DRF100

Symbol	Parameter	Min	Typ	Max	Unit
C_{out}	Output Capacitance		2500		pF
R_{out}	Output Resistance		1		Ω
L_{out}	Output Inductance	2	3	4	nH
F_{MAX}	Operating Frequency CL=3nF + 50Ω			30	MHz
F_{MAX}	Operating Frequency RL=50Ω			50	

Thermal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case		1.5		°C/W
$R_{\theta JHS}$	Thermal Resistance Junction to Heat Sink		2.53		
T_{JSTG}	Storage Temperature		-55 to150		°C
P_{DHS}	Maximum Power Dissipation @ T_{SINK} = 25°C		60		W
P_{DC}	Total Power Dissipation @ T_C = 25°C		100		

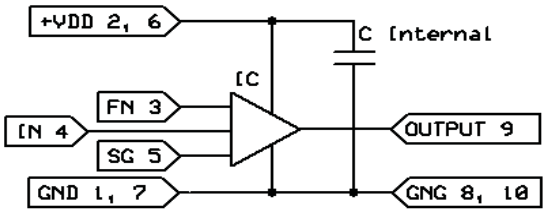

Figure 1, DRF100 Simplified Circuit Diagram

The Simplified DRF100 Circuit Diagram is illustrated above. By including the driver high speed by-pass capacitor (C Internal), the contribution to the internal parasitic loop inductance of the driver output is greatly reduced. This low parasitic approach, coupled with the Schmitt trigger input (pin 4), Kelvin signal ground (pin 5) and the Anti-Ring Function, provide improved stability and control. The IN pin (4) is applied to a Schmitt Trigger. The signal is then applied to the intermediate drivers and level shifters; this section contains proprietary circuitry designed specifically for ring abatement. The P channel and N channel power drivers provide the high current to the OUTPUT (pin 9.)

The Function (FN, pin 3) is the invert or non-invert select Pin, it is Internally held high, Normally Non-inverting.

Truth Table *Referenced to SG			
FN (pin 3)*	**IN (pin 4)***	**Function**	**OUTPUT**
HIGH	HIGH	Non-Invert	HIGH
HIGH	LOW	Non-Invert	LOW
LOW	HIGH	Inverting	LOW
LOW	LOW	Inverting	HIGH

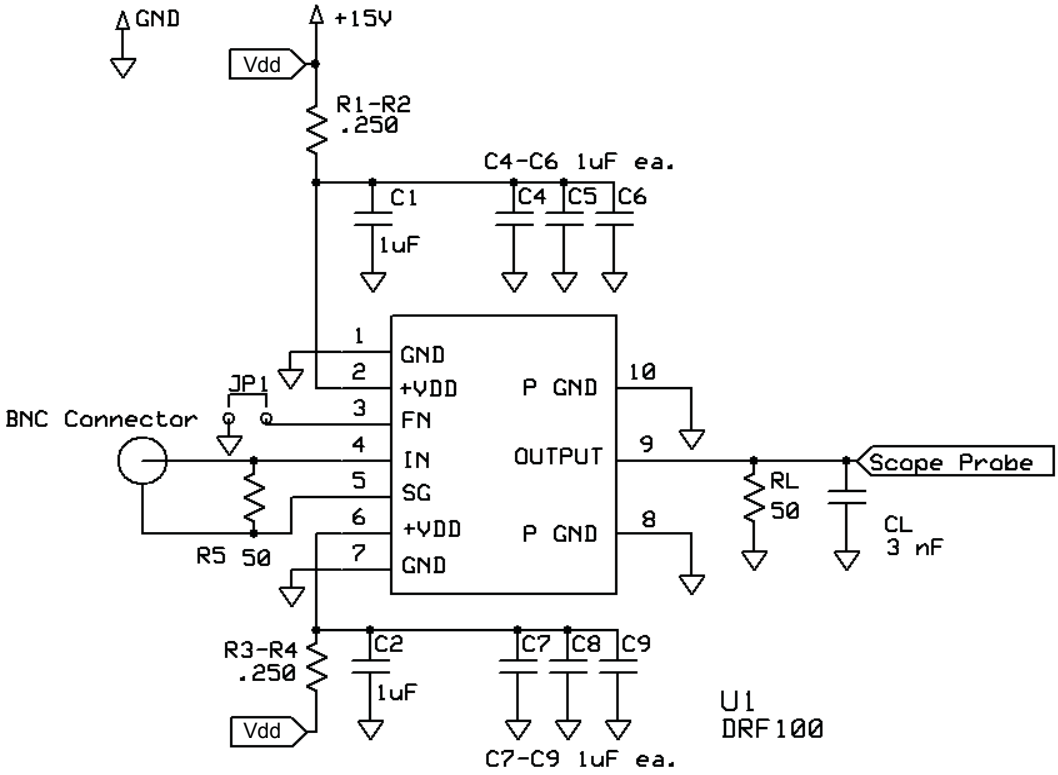

Figure 2, DRF100 Test Circuit

The Test Circuit illustrated above was used to evaluate the DRF100 (available as an evaluation Board DRF100 / EVALSW.) The input control signal is applied to the DRF100 via IN(4) and SG(5) pins using RG188. This provides excellent noise immunity and control of the signal ground currents.

The $+V_{DD}$ inputs (2,6) are by-passed (C1, C2, C4-C9), this is in addition to the internal by-passing mentioned previously. The capacitors used for this function must be capable of supporting the RMS currents and frequency of the gate load.

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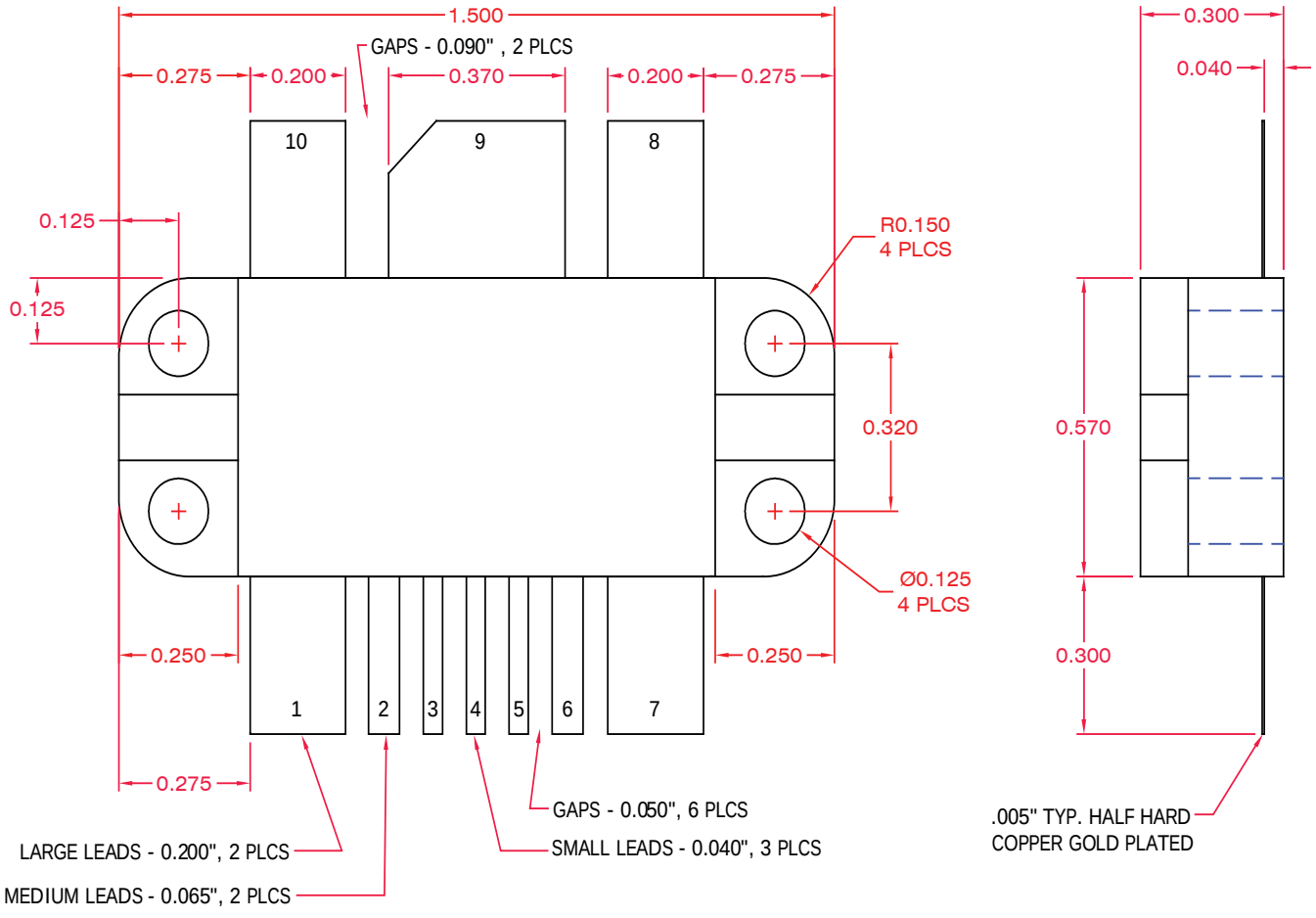
Pin Assignments	
Pin 1	Ground
Pin 2	+Vdd
Pin 3	FN
Pin 4	IN
Pin 5	SG
Pin 6	+Vdd
Pin 7	Ground
Pin 8	Source
Pin 9	Drain
Pin 10	Source



All dimensions are ± .005

Figure 3, DRF100 Mechanical Outline