

# 74HC4040; 74HCT4040

## 12-stage binary ripple counter

Rev. 5 — 3 February 2016

Product data sheet

### 1. General description

The 74HC4040; 74HCT4040 is a 12-stage binary ripple counter with a clock input ( $\overline{CP}$ ), an overriding asynchronous master reset input (MR) and twelve parallel outputs (Q0 to Q11). The counter advances on the HIGH-to-LOW transition of  $\overline{CP}$ . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of  $\overline{CP}$ . Each counter stage is a static toggle flip-flop. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

### 2. Features and benefits

- Complies with JEDEC standard no. 7A
- Input levels:
  - ◆ For 74HC4040: CMOS level
  - ◆ For 74HCT4040: TTL level
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

### 3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

### 4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4040D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4040D				
74HC4040DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT4040DB				

**nexperia**

Table 1. Ordering information ...continued

Type number	Package			
	Temperature range	Name	Description	Version
74HC4040PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT4040PW				
74HC4040BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4040BQ				

## 5. Functional diagram

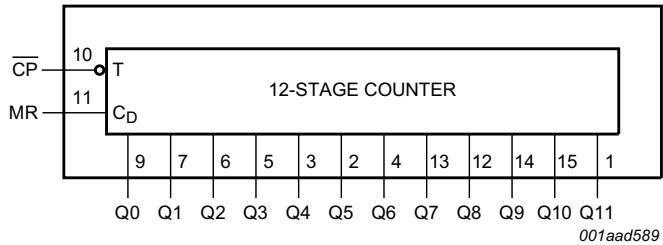


Fig 1. Functional diagram

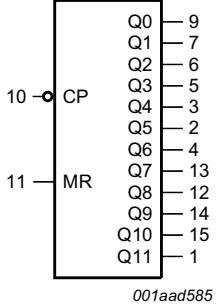


Fig 2. Logic symbol

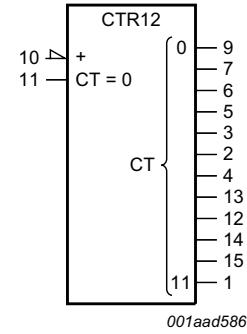


Fig 3. IEC logic symbol

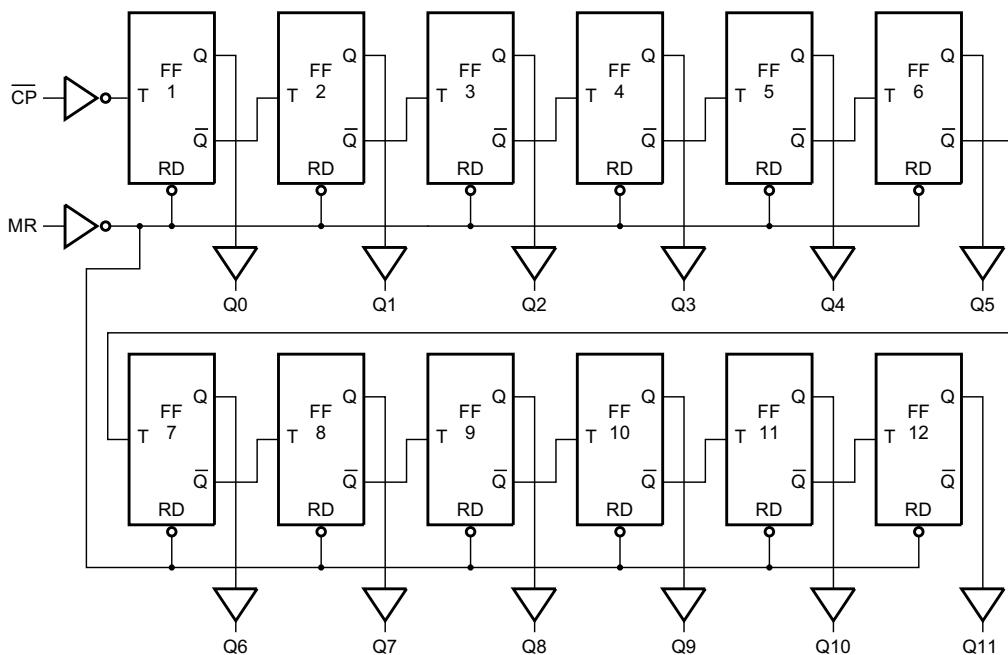


Fig 4. Logic diagram

## 6. Pinning information

### 6.1 Pinning

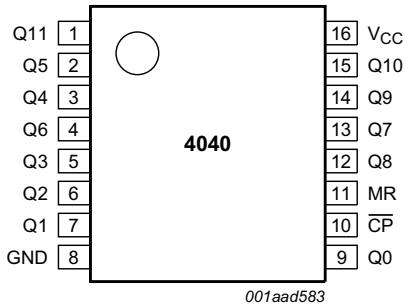


Fig 5. Pin configuration SO16, SSOP16 and TSSOP16

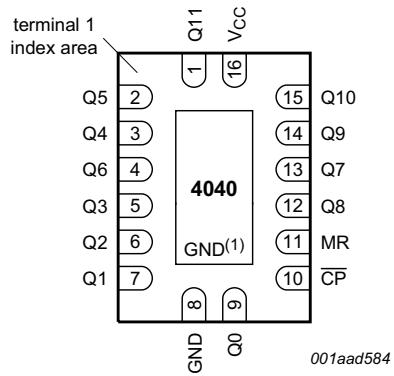


Fig 6. Pin configuration DHVQFN16

- (1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

## 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q11	1	output 11
Q5	2	output 5
Q4	3	output 4
Q6	4	output 6
Q3	5	output 3
Q2	6	output 2
Q1	7	output 1
GND	8	ground (0 V)
Q0	9	output 0
CP	10	clock input (HIGH-to-LOW, edge-triggered)
MR	11	master reset input (active HIGH)
Q8	12	output 8
Q7	13	output 7
Q9	14	output 9
Q10	15	output 10
V <sub>CC</sub>	16	positive supply voltage

## 7. Functional description

### 7.1 Function table

Table 3. Function table

Input		Output
CP	MR	Q0 to Q11
↑	L	no change
↓	L	count
X	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

## 7.2 Timing diagram

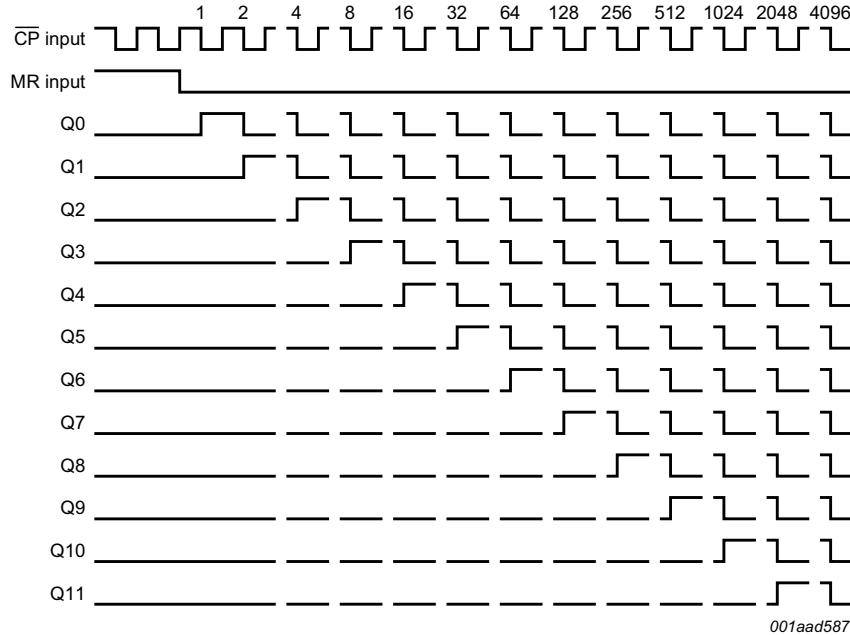


Fig 7. Timing diagram

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	[1]	-	$\pm 20$ mA
$I_{OK}$	output clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	[1]	-	$\pm 20$ mA
$I_O$	output current	$-0.5 \text{ V} < V_O < V_{CC} + 0.5 \text{ V}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	$\pm 50$	mA
$I_{GND}$	ground current		-	$\pm 50$	mA
$T_{stg}$	storage temperature		-65	+150	$^{\circ}\text{C}$
$P_{tot}$	total power dissipation	$T_{amb} = -40 \text{ }^{\circ}\text{C}$ to $+125 \text{ }^{\circ}\text{C}$	[2]		
		SO16, SSOP16, TSSOP16 and DHVQFN16 packages	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above  $70 \text{ }^{\circ}\text{C}$ .

For SSOP16 and TSSOP16 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above  $60 \text{ }^{\circ}\text{C}$ .

For DHVQFN16 packages:  $P_{tot}$  derates linearly with 4.5 mW/K above  $60 \text{ }^{\circ}\text{C}$ .

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC4040			74HCT4040			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5$ V	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0$ V	-	-	83	-	-	-	ns/V

## 10. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC4040</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5$ V	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0$ V	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0$ V	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5$ V	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0$ V	-	2.8	1.8	-	1.8	-	1.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -20$ µA; $V_{CC} = 2.0$ V	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20$ µA; $V_{CC} = 4.5$ V	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20$ µA; $V_{CC} = 6.0$ V	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0$ mA; $V_{CC} = 4.5$ V	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -5.2$ mA; $V_{CC} = 6.0$ V	5.48	5.81	-	5.34	-	5.2	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 20$ µA; $V_{CC} = 2.0$ V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20$ µA; $V_{CC} = 4.5$ V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20$ µA; $V_{CC} = 6.0$ V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0$ mA; $V_{CC} = 4.5$ V	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2$ mA; $V_{CC} = 6.0$ V	-	0.16	0.26	-	0.33	-	0.4	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±0.1	-	±1.0	-	±1.0	µA
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	8.0	-	80	-	160	µA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$C_I$	input capacitance		-	3.5	-					pF
<b>74HCT4040</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	1.2	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = -20 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4 \text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = 20 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}$	-	0.15	0.26	-	0.33	-	0.4	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μA
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	8.0	-	80	-	160	μA
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; $I_O = 0 \text{ A}$ ; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		pin $\overline{CP}$	-	85	306	-	383	-	417	μA
		pin MR	-	110	396	-	495	-	539	μA
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit, see [Figure 9](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC4040</b>										
$t_{pd}$	propagation delay	CP to Q0; see <a href="#">Figure 8</a> [1]								
		$V_{CC} = 2.0 \text{ V}$	-	47	150	-	190	-	225	ns
		$V_{CC} = 4.5 \text{ V}$	-	17	30	-	38	-	45	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	14	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	14	26	-	33	-	38	ns
		Qn to Qn+1; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0 \text{ V}$	-	28	100	-	125	-	150	ns
		$V_{CC} = 4.5 \text{ V}$	-	10	20	-	25	-	30	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	8	-	-	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	-	8	17	-	21	-	26	ns
$t_{PHL}$	HIGH to LOW propagation delay	MR to Qn; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0 \text{ V}$	-	61	185	-	230	-	280	ns
		$V_{CC} = 4.5 \text{ V}$	-	22	37	-	46	-	56	ns
		$V_{CC} = 6.0 \text{ V}$	-	18	31	-	39	-	48	ns
$t_t$	transition time	Qn; see <a href="#">Figure 8</a> [2]								
		$V_{CC} = 2.0 \text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0 \text{ V}$	-	6	13	-	16	-	19	ns
$t_w$	pulse width	CP input, HIGH or LOW; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0 \text{ V}$	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$	14	4	-	17	-	20	-	ns
		MR input, HIGH; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0 \text{ V}$	80	22	-	100	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$	16	8	-	20	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$	14	6	-	17	-	20	-	ns
		MR to CP; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0 \text{ V}$	50	8	-	65	-	75	-	ns
$t_{rec}$	recovery time	$V_{CC} = 4.5 \text{ V}$	10	3	-	13	-	15	-	ns
		$V_{CC} = 6.0 \text{ V}$	9	2	-	11	-	13	-	ns
$f_{max}$	maximum frequency	CP input; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0 \text{ V}$	6	27	-	4.8	-	4	-	MHz
		$V_{CC} = 4.5 \text{ V}$	30	82	-	24	-	20	-	MHz
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	90	-	-	-	-	-	MHz
		$V_{CC} = 6.0 \text{ V}$	35	98	-	28	-	24	-	MHz

Table 7. Dynamic characteristics ...continued

GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit, see [Figure 9](#).

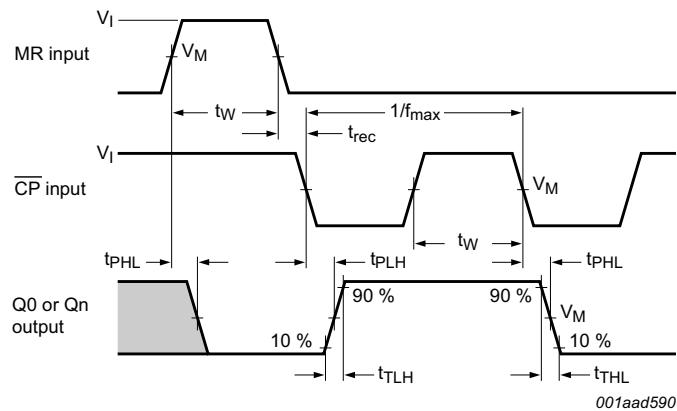
Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$C_{PD}$	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$ <a href="#">[3]</a>	-	20	-	-	-	-	-	pF
<b>74HCT4040</b>										
$t_{pd}$	propagation delay	$\overline{CP}$ to $Q_0$ ; see <a href="#">Figure 8</a> <a href="#">[1]</a>								
		$V_{CC} = 4.5 \text{ V}$	-	19	40	-	50	-	60	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	16	-	-	-	-	-	ns
		$Q_n$ to $Q_{n+1}$ ; see <a href="#">Figure 8</a>								
		$V_{CC} = 4.5 \text{ V}$	-	10	20	-	25	-	30	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	8	-	-	-	-	-	ns
$t_{PHL}$	HIGH to LOW propagation delay	MR to $Q_n$ ; see <a href="#">Figure 8</a>								
		$V_{CC} = 4.5 \text{ V}$	-	23	45	-	56	-	68	ns
$t_t$	transition time	$Q_n$ ; see <a href="#">Figure 8</a> <a href="#">[2]</a>								
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
$t_w$	pulse width	$\overline{CP}$ input, HIGH or LOW; see <a href="#">Figure 8</a>								
		$V_{CC} = 4.5 \text{ V}$	16	7	-	20	-	24	-	ns
		MR input, HIGH; see <a href="#">Figure 8</a>								
		$V_{CC} = 4.5 \text{ V}$	16	6	-	20	-	24	-	ns
$t_{rec}$	recovery time	MR to $\overline{CP}$ ; see <a href="#">Figure 8</a>								
		$V_{CC} = 4.5 \text{ V}$	10	2	-	13	-	15	-	ns
$f_{max}$	maximum frequency	$\overline{CP}$ input; see <a href="#">Figure 8</a>								
		$V_{CC} = 4.5 \text{ V}$	30	72	-	24	-	20	-	MHz
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	79	-	-	-	-	-	MHz
$C_{PD}$	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$ <a href="#">[3]</a>	-	20	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PHL}$ ,  $t_{PLH}$ .[2]  $t_t$  is the same as  $t_{THL}$ ,  $t_{TLH}$ .[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where: $f_i$  = input frequency in MHz; $f_o$  = output frequency in MHz; $C_L$  = output load capacitance in pF; $V_{CC}$  = supply voltage in V;

N = number of inputs switching;

 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

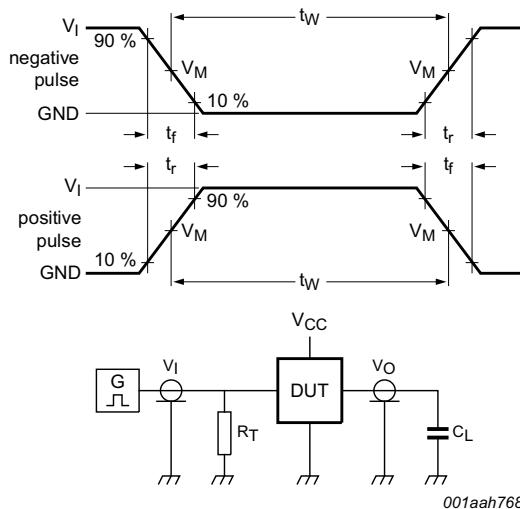
## 12. Waveform and test circuit



74HC4040:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .

74HCT4040:  $V_M = 1.3\text{ V}$ ;  $V_I = \text{GND to } 3\text{ V}$ .

**Fig 8. Clock propagation delays, pulse width, transition times, maximum pulse frequency and master resets**



Test data is given in [Table 8](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

**Fig 9. Test circuit for measuring switching times**

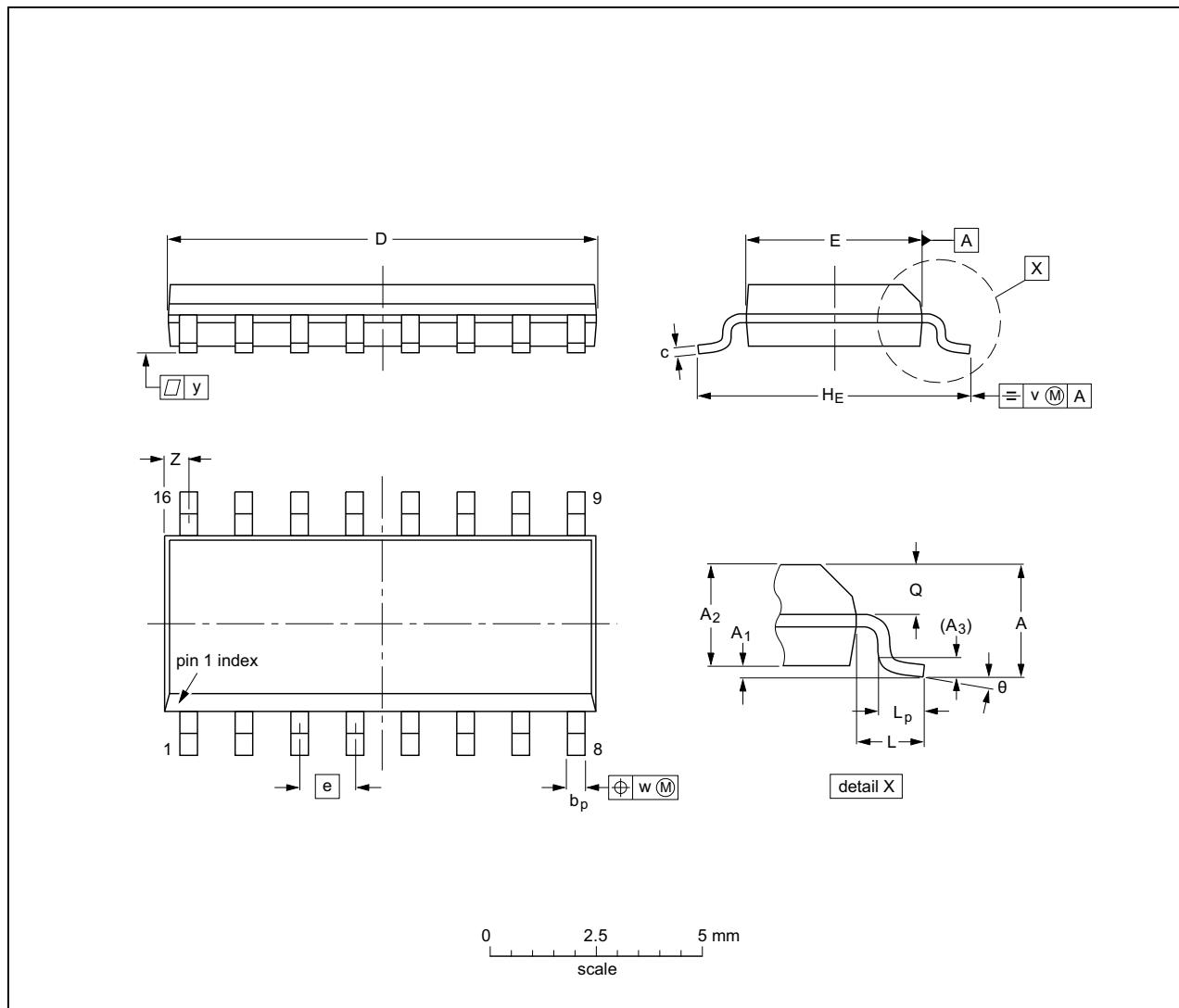
**Table 8. Test data**

Type	Input		Load	Test
	$V_I$	$t_r, t_f$		
74HC4040	$V_{CC}$	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74HCT4040	3.0 V	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

## 13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75 0.10	0.25 1.25	1.45	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 10. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

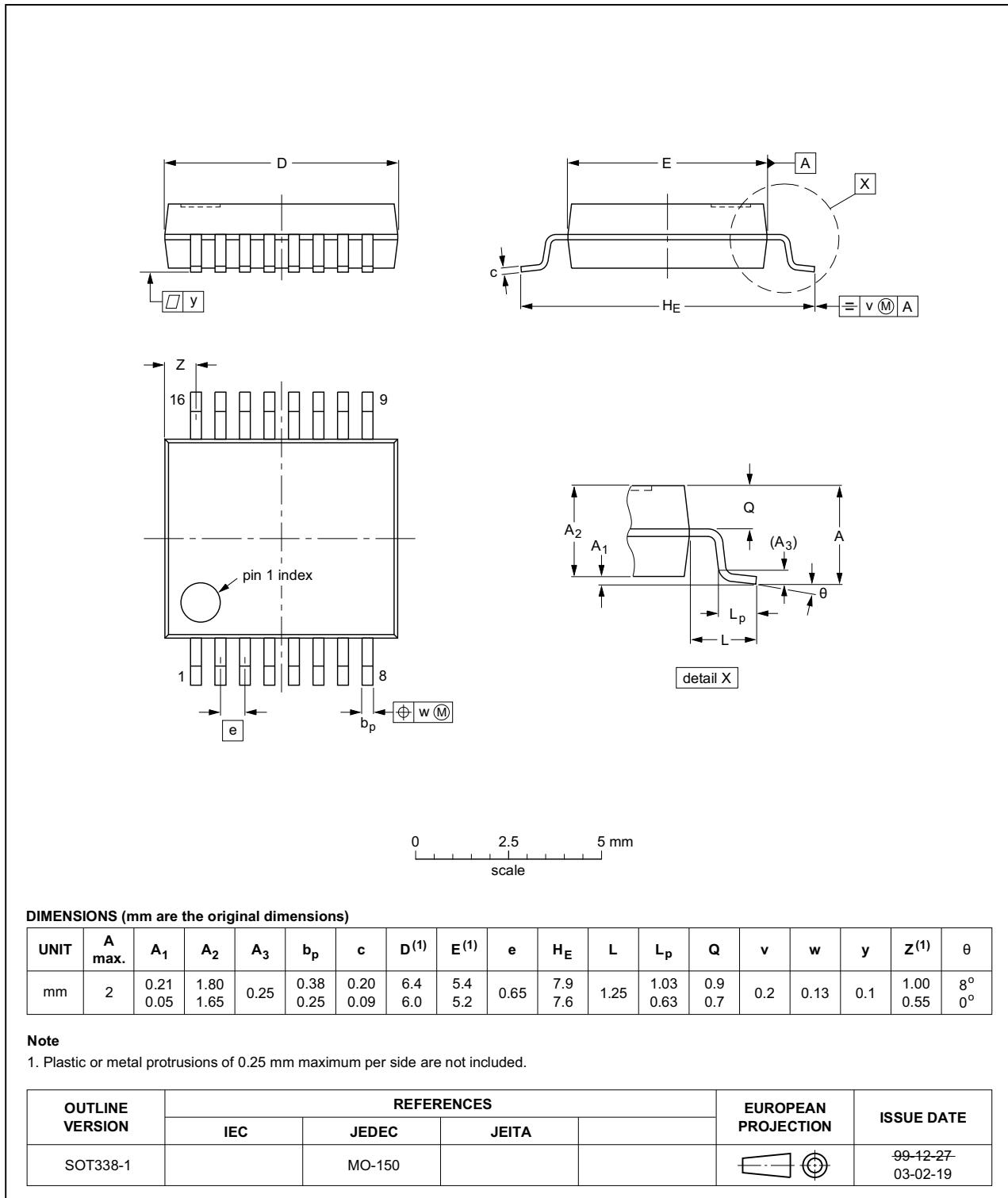


Fig 11. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

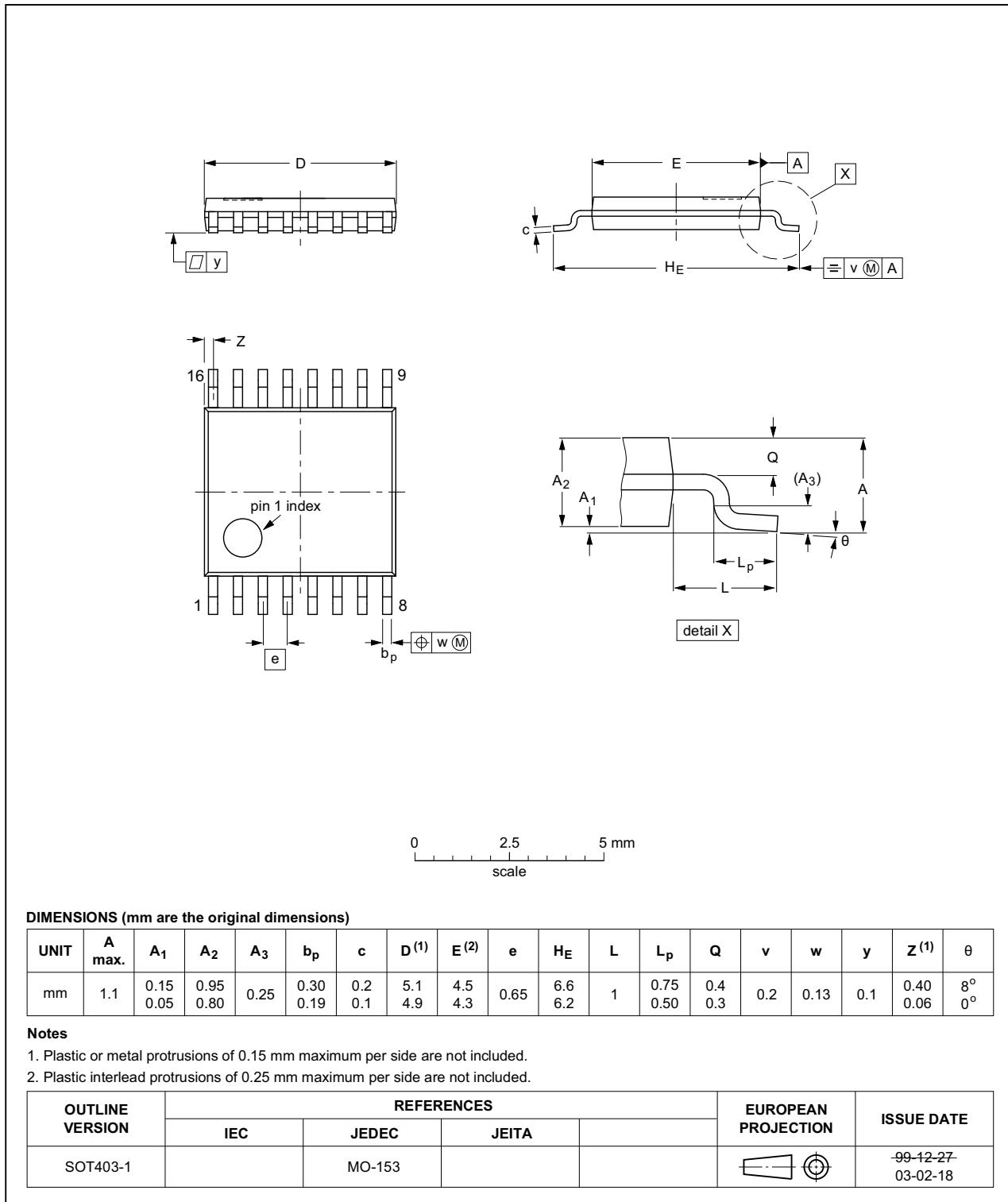


Fig 12. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

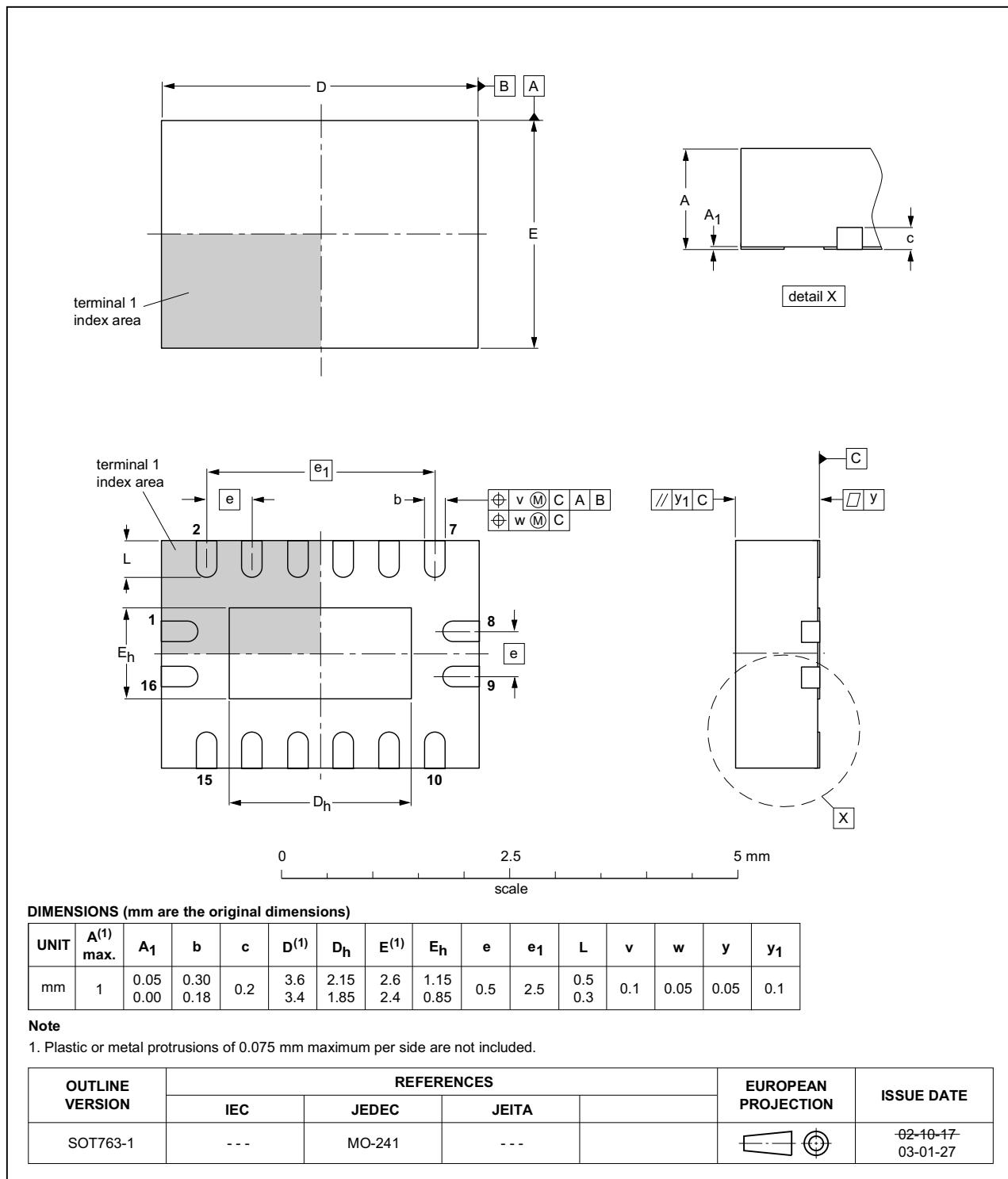


Fig 13. Package outline SOT763-1 (DHVQFN16)

## 14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charge-Device Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4040 v.5	20160203	Product data sheet	-	74HC_HCT4040 v.4
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74HC4040N and 74HCT4040N (SOT38-4) removed.</li> </ul>			
74HC_HCT4040 v.4	20140320	Product data sheet	-	74HC_HCT4040 v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74HC_HCT4040 v.3	20050914	Product data sheet	-	74HC_HCT4040_CNV v.2
74HC_HCT4040_CNV v.2	19901231	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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