



Winbond
Bus Termination Regulator
W83310S-R2
W83310G-R2

W83310S-R2/W83310G-R2



W83310S-R2
Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	N.A.	03/Mar.	0.5	N.A.	All versions before 0.5 are for internal use only
2	4	03/Jul.	0.51	N.A.	Recommend circuit update
3	All	05/Jan.	0.52	N.A.	Add Pb-free part no:W83310G-R2
4	1,2	06/Jan.	0.53	N.A.	Add description of supporting cont. 1.8 Amp driving and sinking current.

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LIFE SUPPORT APPLICATIONS

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1. GENERAL DESCRIPTION

The W83310S-R2 is a linear regulator which provides achieves peak 2.0 Amp/cont. 1.8 Amp bi-directional sinking and driving capability for DDR SDRAM bus terminator application. The chip simply implement a stable power supply which can track half of input power dynamically for bus terminator with a single chip; that is the chip integrates two power MOSFETs. There is no any external power device needed. The W83310S-R2 is promoted with small footprint 8-SOP 150mil package. With W83301S-R2 design, a high integration, high performance, and cost-effective solution is promoted.

2. FEATURES

- Regulates a bi-directional power with driving and sinking capability
- Provides achieve peak 2.0 Amp/cont. 1.8 Amp driving and sinking current
- Power MOSFET integrated
- Low external component count
- Low output voltage offset
- Operates with +3.3V and +2.5V control power
- Small package
- Low cost and easy to use

3. APPLICATIONS

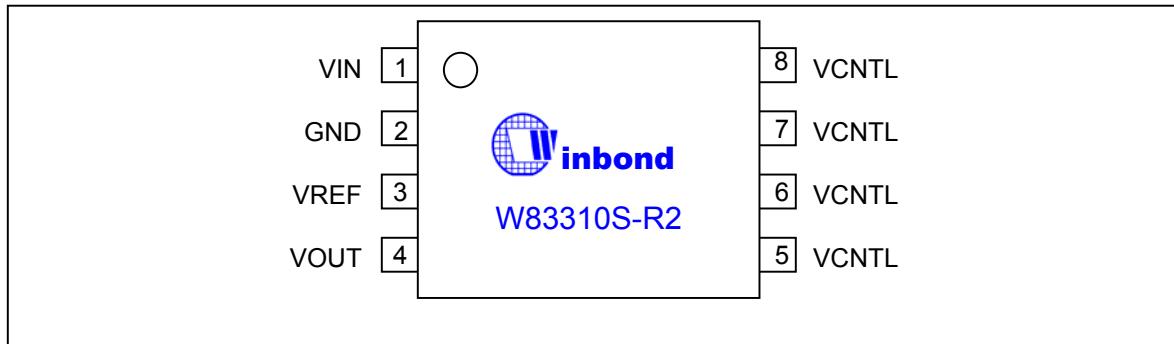
- DDR Bus Termination Regulator
- Active Termination Bus
- SSTL-2
- SSTL-3

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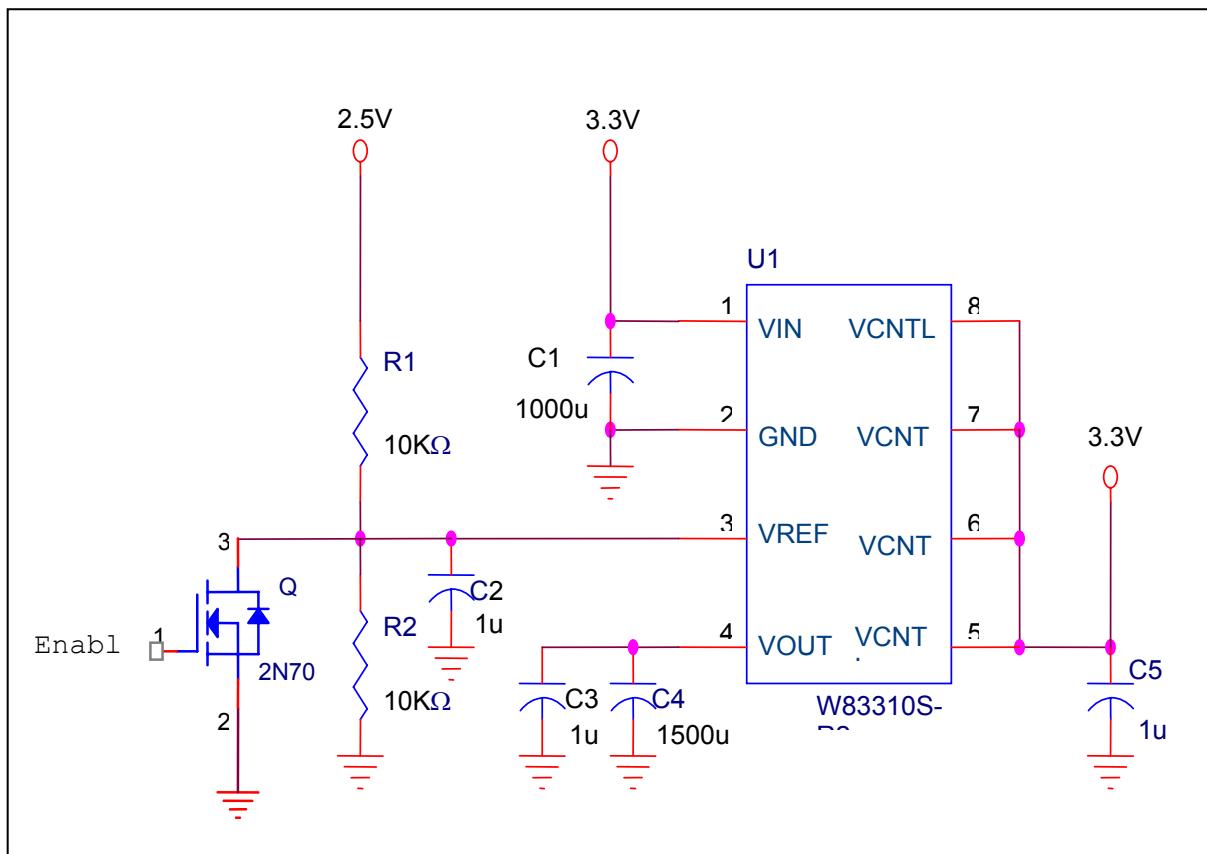
4. PIN CONFIGURATION AND DESCRIPTION

- W83310S-R2



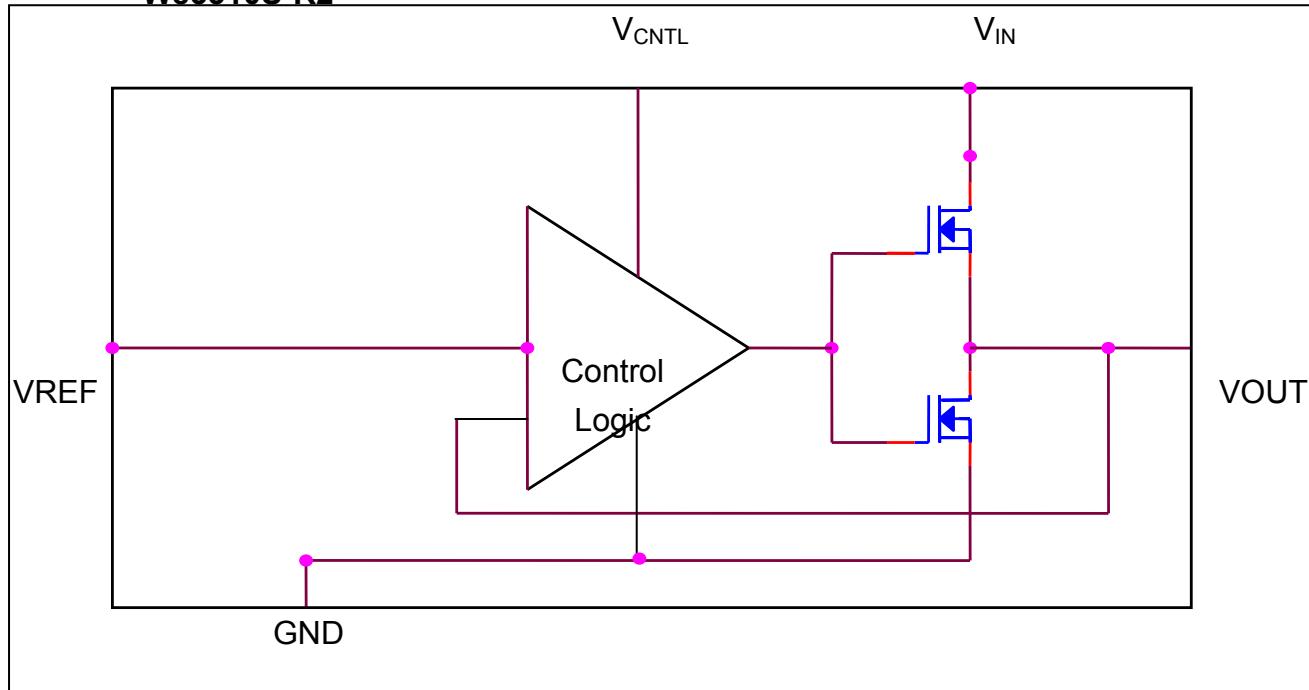
SYMBOL	PIN	FUNCTION
VIN	1	Power input pin.
GND	2	Ground.
VREF	3	Reference voltage and Chip enable.
VOUT	4	Output voltage.
VCNTL	5	Gate drive voltage.
VCNTL	6	Gate drive voltage.
VCNTL	7	Gate drive voltage.
VCNTL	8	Gate drive voltage.

5. APPLICATION CIRCUIT



6. INTERNAL BLOCK DIAGRAM

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7. ELECTRICAL CHARACTERISTICS

7.1 AC CHARACTERISTICS

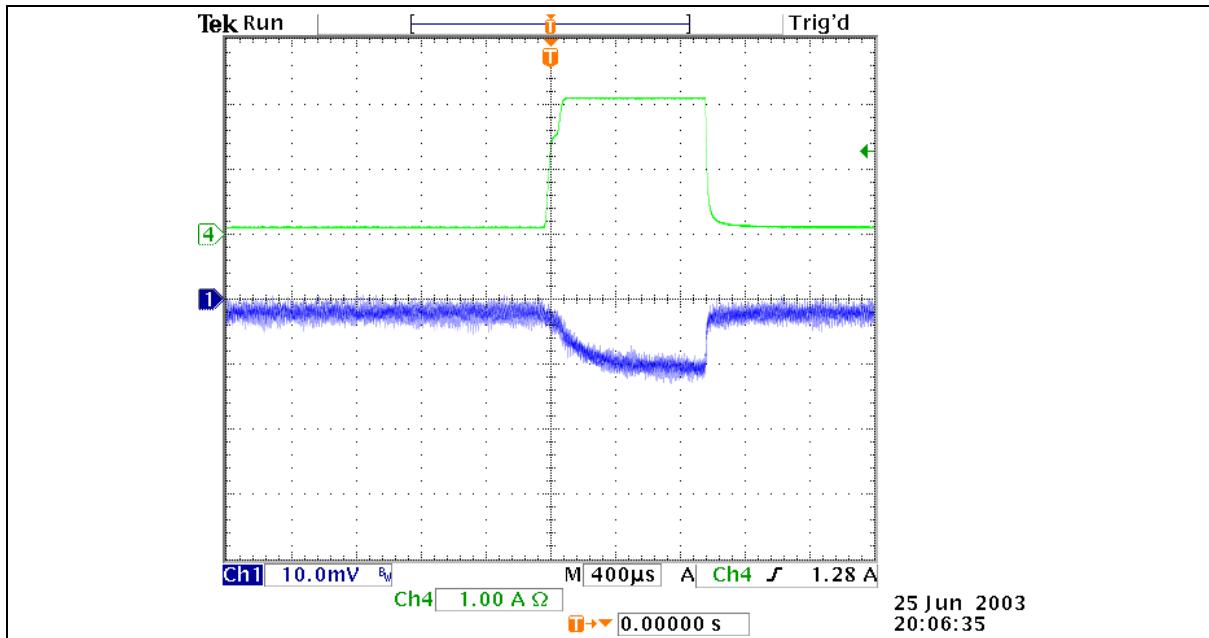
W83310S-R2						
$V_{IN}=2.5V, V_{CNTL}=3.3V, V_{REF}=1.25V, C_{out}=100\mu F, T_A = 0^{\circ}C \text{ to } +70^{\circ}C$						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Output Offset Voltage	V_{os}	-5	0	+5	mV	$I_{OUT}=0A$
Load Regulation			1.0		%	Loading: $0A \rightarrow 2.0A$
			1.0			Loading: $0A \rightarrow -2.0A$
Input Voltage Range	V_{IN}		2.5	3.63	V	
	V_{CNTL}		3.3	3.63		
Operating Current of V_{CNTL}	I_{CNTL}		0.5	1.0	mA	No Load($I_{OUT}=0A$)
Shutdown Threshold Trigger		0.8			V	Output=High
				0.2	V	Output=Low
Shutdown Current	I_{SHDN}		10		uA	$V_{REF}<0.2V$ Loading=0.7A
Short Current Limit	I_{LMT}		4.0		A	

Note: Load regulation is tested with a 1ms duty pulse current and measuring V_{OUT} .

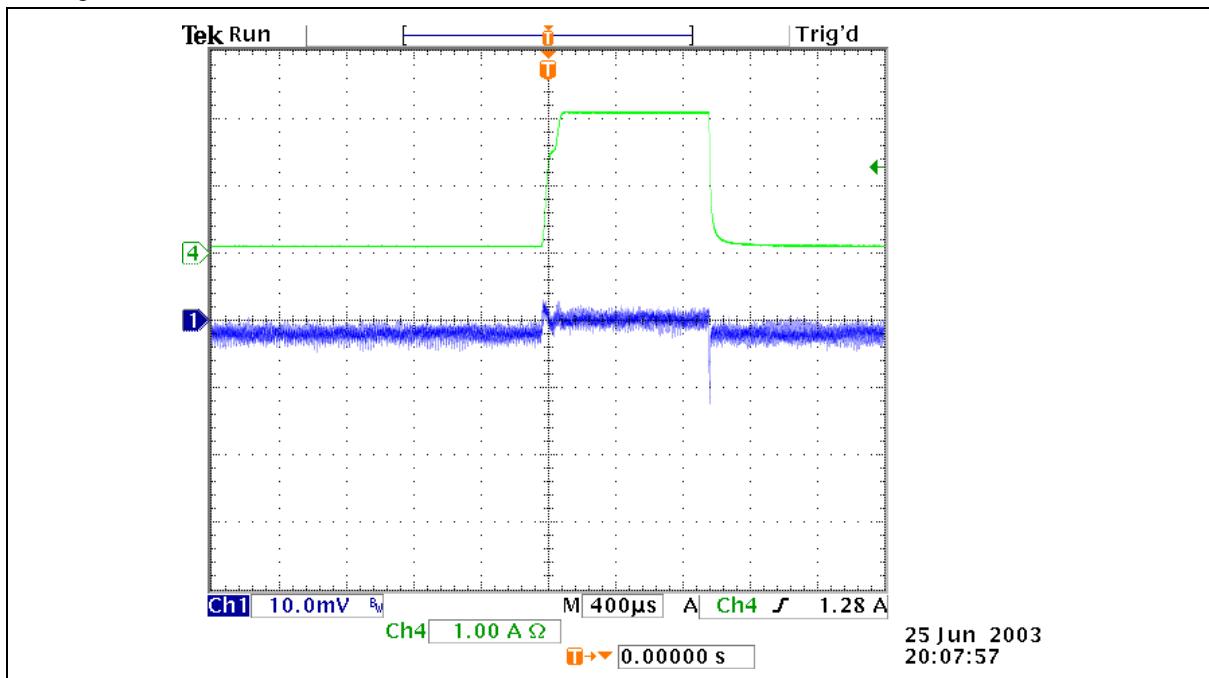


8. TYPICAL OPERATING WAVEFORM

Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.25V$; 2.0Amp 1ms duty pulse driving current. $\Delta V \approx 9mV$.



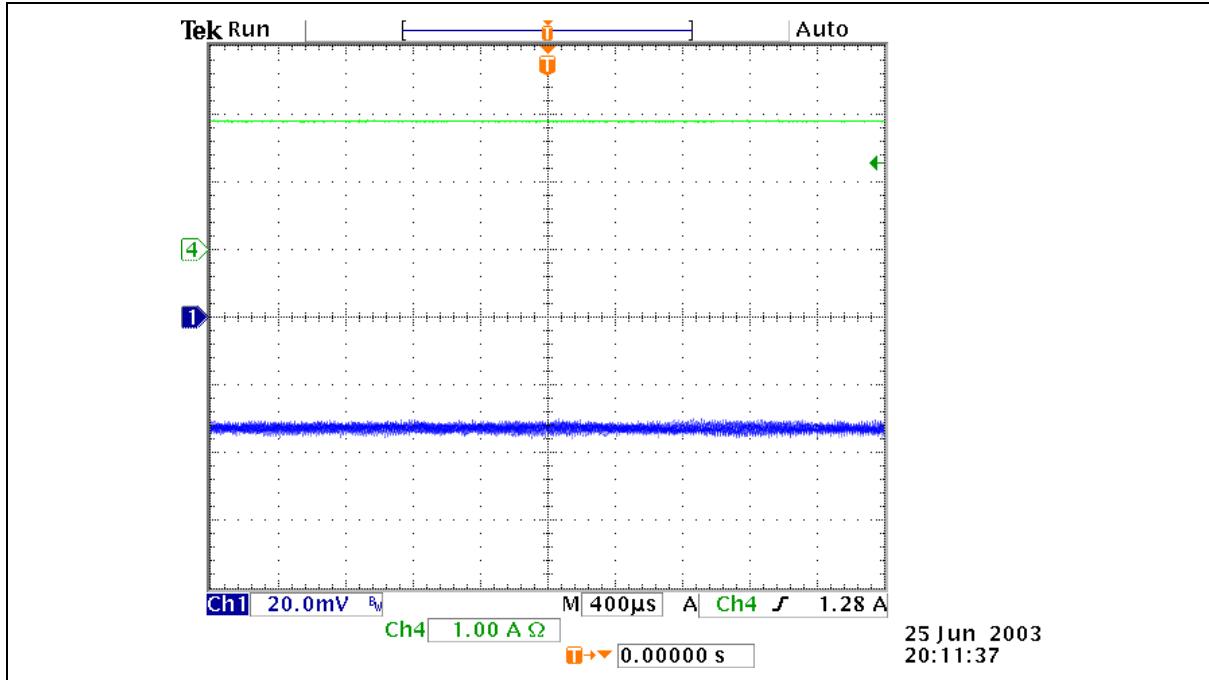
Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.25V$; 2.0Amp 1ms duty pulse sinking current. $\Delta V \approx 4mV$.



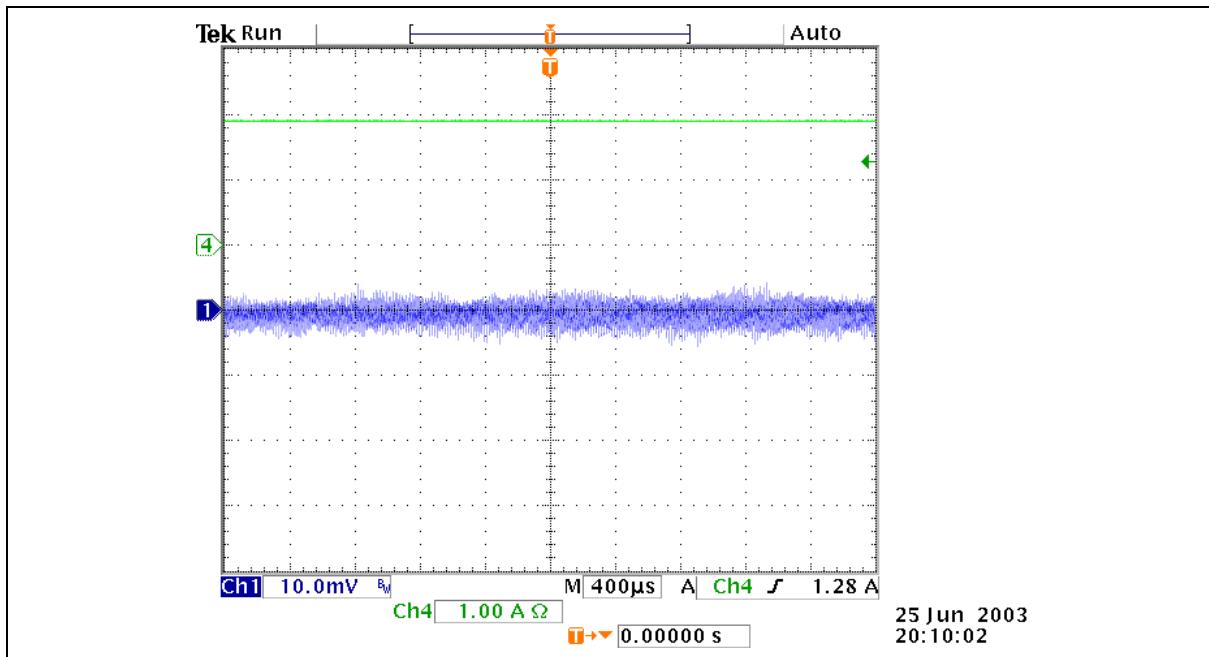
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Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.25V$; 1.8Amp cont. driving current. $\Delta V \approx 32mV$ @ $\sim 85^{\circ}\text{C}$.



Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.25V$; 1.8Amp cont. sinking current. $\Delta V \approx 2mV$ @ $\sim 85^{\circ}\text{C}$.

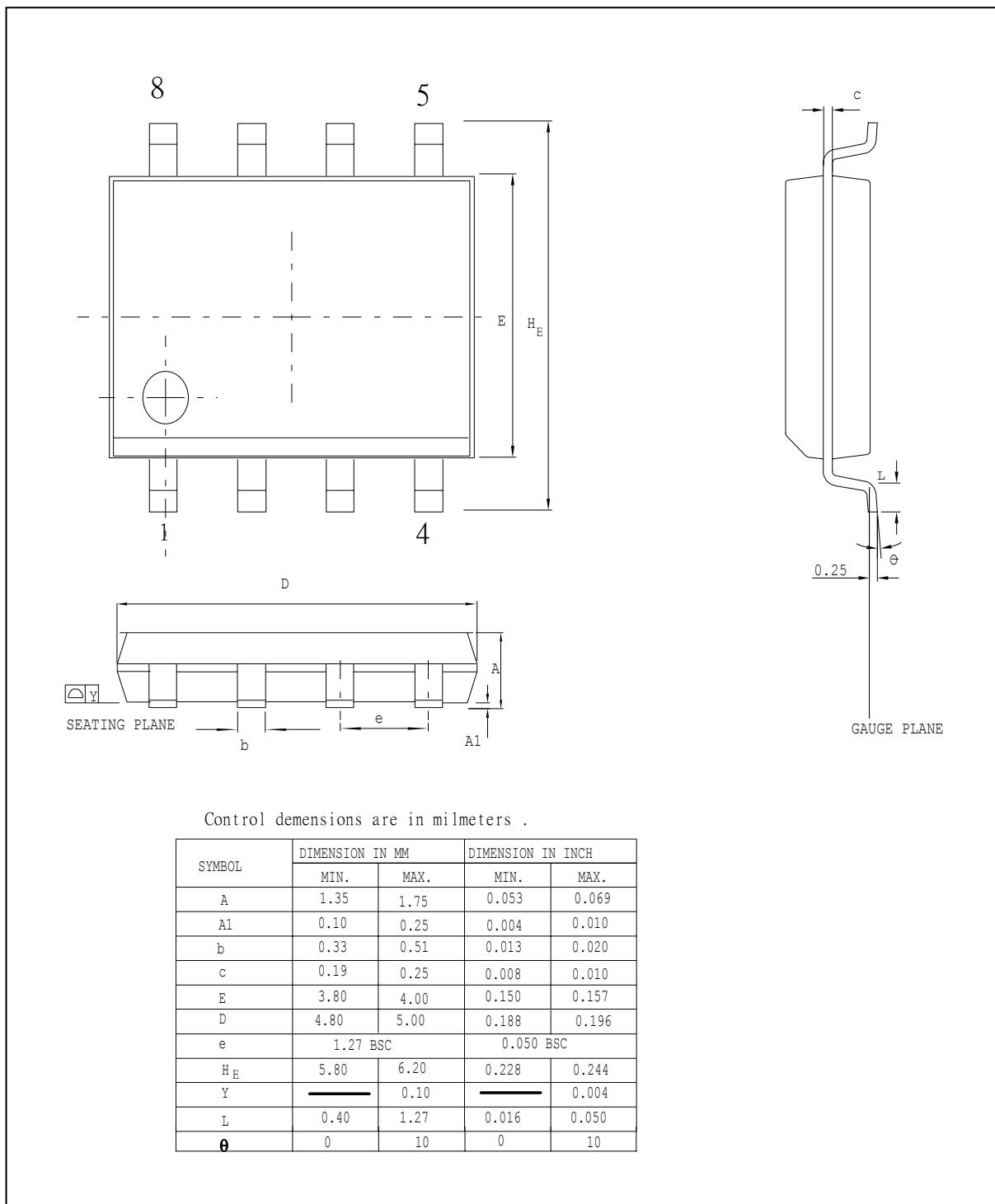


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9. PACKAGE DIMENSION

8L SOP 150mil



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10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83310S-R2	8 PIN SOP	Commercial, 0°C to +70°C
W83310G-R2	8 PIN SOP(Pb-free package)	Commercial, 0°C to +70°C

11. HOW TO READ THE TOP MARKING



Left line: Winbond logo

1st & 2nd line: W83310S-R2 – the part number , W83310G-R2-the Pb-free part number

3rd line: Tracking code Tracking code 249 O A

249: packages assembled in Year 02', week 49

O: assembly house ID; O means OSE, G means GR, etc.

B: the IC version

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