

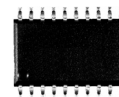


# 3.3V/5V PECL/ECL 3GHz DUAL DIFFERENTIAL 2:1 MULTIPLEXER

ECL Pro™  
SY100EP56V

## FEATURES

- Dual, fully differential 2:1 PECL/ECL multiplexer
- Guaranteed AC parameters over temperature/voltage:
  - > 3GHz  $f_{MAX}$  (toggle)
  - < 100ps within device skew
  - < 230ps rise/fall times
  - < 500ps propagation delay
- Flexible power supply: 3.0V to 5.5V
- Wide operating temperature range: -40°C to +85°C
- $V_{BB}$  reference for AC-coupled and single-ended applications
- Both channels have independent input select or common select control
- 100k PECL/ECL compatible logic
- Available in 20-pin TSSOP package



ECL Pro™

## DESCRIPTION

The SY100EP56V is a high-speed, low-skew, fully differential Dual PECL/ECL 2:1 multiplexer. This device is a pin-for-pin, plug-in replacement to the MC10/100EP56DT. Two separate 2:1 multiplexers (Channel 0 and Channel 1) with dedicated select control pins (SEL0 and SEL1) are implemented in a 20-pin TSSOP package. The signal-path inputs (D0a, D0b and D1a, D1b) accept differential signals as low as 150mV pk-pk. For applications that require common select control for both channels A & B, a common select pin (COM\_SEL) is available. All I/O pins are 100k PECL/ECL logic compatible.

AC-performance is guaranteed over the industrial -40°C to +85°C temperature range and 3.0V to 5.5V supply voltage range. This device will operate in PECL/LVPECL or ECL/LVECL mode. The 500ps max (400 typ) propagation delay is matched for all signal and logic select paths: D-to- $Q_{OUT}$ , SEL-to- $Q_{OUT}$ , and COM\_SEL-to- $Q_{OUT}$ . Two  $V_{BB}$  output reference pins (approx equal to  $V_{CC} - 1.4V$ ) are available for AC-coupled or single-ended applications.

The SY100EP56V is part of Micrel's high-speed, Precision Edge timing and distribution family. For applications that require a different I/O combination, consult the Micrel website at [www.micrel.com](http://www.micrel.com), and choose from a comprehensive product line of high-speed, low skew fanout buffers, translators, and clock dividers.

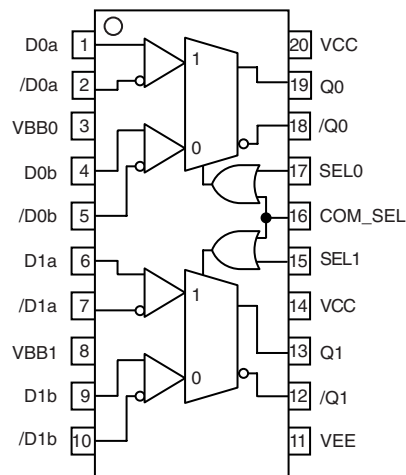
## CROSS REFERENCE TABLE

Micrel Semiconductor	ON Semiconductor
SY100EP56VK4I	MC100EP56DT
SY100EP56VK4ITR	MC100EP56DTR2

## MUX SELECT TRUTH TABLE

SEL0	SEL1	COM_SEL	Q0, /Q0	Q1, /Q1
X	X	H	a	a
L	L	L	b	b
L	H	L	b	a
H	H	L	a	a
H	L	L	a	b

## PACKAGE/ORDERING INFORMATION



20-Pin TSSOP (K4-20-1)

Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100EP56VK4I	K4-20-1	Industrial	XEP56V	Sn-Pb
SY100EP56VK4ITR <sup>(2)</sup>	K4-20-1	Industrial	XEP56V	Sn-Pb
SY100EP56VK4G <sup>(3)</sup>	K4-20-1	Industrial	XEP56V with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EP56VK4GTR <sup>(2, 3)</sup>	K4-20-1	Industrial	XEP56V with Pb-Free bar-line indicator	Pb-Free NiPdAu

## Notes:

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

## PIN DESCRIPTION

Pin	Pin Number	Function
D0a, /D0a D0b, /D0b	1, 2, 4, 5	Channel 0 PECL/ECL differential signal inputs. Multiplexing of these two differential inputs is controlled by SEL0, or COM_SEL. The signal inputs include internal 75k $\Omega$ pull-down resistors. Default condition is LOW when left floating. The input signal should be terminated externally. See "Termination" section
D1a, /D1a D1b, /D1b	6, 7 9, 10	Channel 1 PECL/ECL differential signal inputs. Multiplexing of these two differential inputs is controlled by SEL1, or COM_SEL. The signal inputs include internal 75k $\Omega$ pull-down resistors. Default condition is a logic LOW when left floating. The input signal should be terminated externally. See "Termination" section
VBB0, VBB1	3, 8	Channel 0 and Channel 1 reference output voltage. This reference is typically used to bias the unused inverting input for single-ended input applications, or as the termination point for AC-coupled differential input applications. $V_{BB}$ reference value is approximately $V_{CC} - 1.4\text{V}$ , and tracks $V_{CC}$ 1:1. Maximum sink/source capability is 0.50mA. For single ended PECL inputs, connect to the unused input through a 50 $\Omega$ resistor. Decouple the $V_{BB}$ pin with a 0.01 $\mu\text{F}$ capacitor. For PECL/LVPECL inputs, the decoupling capacitor is connected to $V_{CC}$ , since PECL signals are referenced to $V_{CC}$ . Leave floating if not used.
VEE	11	Negative Power Supply: For PECL/LVPECL applications, connect to GND.
/Q1, Q1	12, 13	Channel 1 100KEP PECL/ECL compatible differential output. PECL/ECL termination is with a 50 $\Omega$ resistor to $V_{CC} - 2\text{V}$ . Unused output pairs may be left floating. Unused single-ended outputs must have a balanced load. For AC-coupled applications, the output stage emitter follower must have a DC current path to ground. See "Termination" section.
SEL1, SEL0	15, 17	100KEP PECL/ECL compatible Channel 1 and Channel 0 MUX select control. See "MUX Select Truth Table." Each pin includes an internal 75k $\Omega$ pull-down resistor. Default condition when left floating is LOW.
COM_SEL	16	100KEP PECL/ECL compatible Channel 1 and Channel 0 Common MUX select control. This is the common select control pin for both Channels 0 and 1. Includes an internal 75k $\Omega$ pull-down resistor. Default condition when left floating is LOW. Leave floating when not used.
/Q0, Q0	18, 19	Channel 0 100K EP PECL/ECL compatible differential output. PECL/ECL termination is with a 50 $\Omega$ resistor to $V_{CC} - 2\text{V}$ . Unused output pairs may be left floating. Unused single-ended outputs must have a balanced load. For AC-coupled applications, the output stage emitter follower must have a DC current path to ground. See "Termination" section.
VCC	14, 20	Positive Power Supply: Both $V_{CC}$ pins must be connected to the same power supply externally. Bypass with 0.1 $\mu\text{F}$ /0.01 $\mu\text{F}$ low ESR capacitors.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Value	Unit
$V_{CC} - V_{EE}$	Power Supply Voltage	6.0	V
$V_{IN}$	Input Voltage ( $V_{CC} = 0V$ , $V_{IN}$ not more negative than $V_{EE}$ ) Input Voltage ( $V_{EE} = 0V$ , $V_{IN}$ not more positive than $V_{CC}$ )	-6.0 to 0 +6.0 to 0	V V
$I_{OUT}$	Output Current -Continuous -Surge	50 100	mA
$I_{BB}$	$V_{BB}$ Sink/Source Current <sup>(2)</sup>	±0.5	mA
$T_{LEAD}$	Lead Temperature (soldering, 20sec.)	+260	°C
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{store}$	Storage Temperature Range	-65 to +150	°C
$\theta_{JA}$	Package Thermal Resistance (Junction-to-Ambient) -Still-Air (single-layer PCB) -Still-Air (multi-layer PCB) -500lfpm (multi-layer PCB)	115 75 65	°C/W
$\theta_{JC}$	Package Thermal Resistance (Junction-to-Case)	21	°C/W

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Due to the limited drive capability, the  $V_{BB}$  reference should only be used for inputs from the same package device (i.e., do not use for other devices).

**DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$V_{CC}$	Power Supply Voltage (PECL) (LVPECL) (ECL) (LVECL)	4.5 3.0 -5.5 -3.8	5.0 3.3 -5.0 -3.3	5.5 3.8 -4.5 -3.0	4.5 3.0 -5.5 -3.8	5.0 3.3 -5.0 -3.3	5.5 3.8 -4.5 -3.0	4.5 3.0 -5.5 -3.8	5.0 3.3 -5.0 -3.3	5.5 3.8 -4.5 -3.0	V	
$I_{EE}$	Supply Current	—	50	65	—	50	65	—	50	65	mA	No Load
$I_{IH}$	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	$V_{IN} = V_{IH}$
$I_{IL}$	Input LOW Current All Inputs	0.5	—	—	0.5	—	—	0.5	—	—	μA	$V_{IN} = V_{IL}$
$C_{IN}$	Input Capacitance (TSSOP)	—	—	—	—	1.0	—	—	—	—	pF	

**Note:**

1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

**(100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>** $V_{CC} = 3.3V \pm 10\%$ ,  $V_{EE} = 0V$ 

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$V_{IL}$	Input LOW Voltage (Single-Ended)	1355	—	1675	1355	—	1675	1355	—	1675	mV	
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2075	—	2420	2075	—	2420	2075	—	2420	mV	
$V_{OL}$	Output LOW Voltage	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV	50Ω to $V_{CC}-2V$
$V_{OH}$	Output HIGH Voltage	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV	50Ω to $V_{CC}-2V$
$V_{BB}$	Output Reference Voltage	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV	
$V_{IHCMR}$	Input HIGH Voltage <sup>(2)</sup> Common Mode Range	2.0	—	$V_{CC}$	2.0	—	$V_{CC}$	2.0	—	$V_{CC}$	V	

**Notes:**

- 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at  $V_{CC} = 3.3V$ . They vary 1:1 with  $V_{CC}$ .
- The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**(100KEP) PECL DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>** $V_{CC} = 5.0V \pm 10\%$ ,  $V_{EE} = 0V$ 

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$V_{IL}$	Input LOW Voltage (Single-Ended)	3055	—	3375	3055	—	3375	3055	—	3375	mV	
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3775	—	4120	3775	—	4120	3775	—	4120	mV	
$V_{OL}$	Output LOW Voltage	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV	50Ω to $V_{CC}-2V$
$V_{OH}$	Output HIGH Voltage	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV	50Ω to $V_{CC}-2V$
$V_{BB}$	Output Reference Voltage	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV	
$V_{IHCMR}$	Input HIGH Voltage <sup>(2)</sup> Common Mode Range	2.0	—	$V_{CC}$	2.0	—	$V_{CC}$	2.0	—	$V_{CC}$	V	

**Notes:**

- 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at  $V_{CC} = 5.0V$ . They vary 1:1 with  $V_{CC}$ .
- The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**(100KEP) ECL/LVECL DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>** $V_{CC} = 0V$ ,  $V_{EE} = -5.5V$  to  $-3.0V$ 

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$V_{IL}$	Input LOW Voltage	-1945	—	-1625	-1945	—	-1625	-1945	—	-1625	mV	
$V_{IH}$	Input HIGH Voltage	-1225	—	-880	-1225	—	-880	-1225	—	-880	mV	
$V_{OL}$	Output LOW Voltage	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV	$50\Omega$ to $V_{CC}-2V$
$V_{OH}$	Output HIGH Voltage	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV	$50\Omega$ to $V_{CC}-2V$
$V_{BB}$	Output Reference Voltage	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV	
$V_{IHCMR}$	Input HIGH Voltage <sup>(2)</sup> Common Mode Range	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	V	

**Notes:**

- 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500fpm is maintained.
- The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**AC ELECTRICAL CHARACTERISTICS** $V_{CC} = 0V$ ;  $V_{EE} = -3.0V$  to  $-5.5V$  or  $V_{CC} = 3.0V$  to  $5.5V$ ,  $V_{EE} = 0V$ 

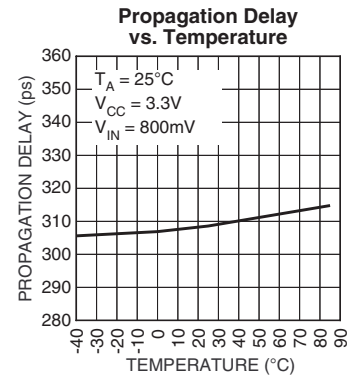
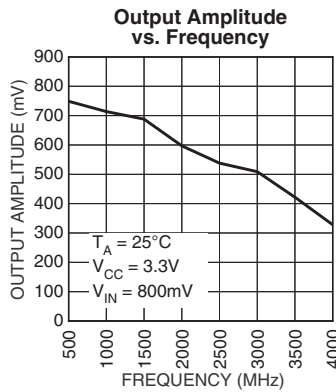
Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$f_{MAX}$	Max. Toggle Frequency <sup>(1)</sup>	3	—	—	3	—	—	3	—	—	GHz	
$t_{PLH}$ $t_{PHL}$	Propagation Delay (Differential) D to Q, /Q SEL to Q, /Q COM_SEL to Q, /Q	230 250 250	290 300 350	450 450 450	230 250 250	290 320 360	470 470 470	230 250 250	300 330 400	500 500 500	ps ps ps	
$t_{SKEW}$	Within-Device Skew <sup>(2)</sup> Q, /Q	—	50	100	—	50	100	—	50	100	ps	
	Part-to-Part Skew <sup>(2)</sup>	—	—	200	—	—	200	—	—	200	ps	
$t_{JITTER}$	Cycle-to-Cycle Jitter (rms)	—	0.2	< 1	—	0.2	< 1	—	0.2	< 1	ps <sub>rms</sub>	
	Random Jitter	—	—	—	—	<1	—	—	—	—	ps <sub>rms</sub>	Note 3
	Deterministic Jitter @ 1.25Gbps @ 2.5Gbps	—	—	—	—	<25 <50	—	—	—	—	ps <sub>pk-pk</sub>	Note 4
$V_{DIFF}$	Input Voltage (Differential)	150	800	1200	150	800	1200	150	800	1200	mV	
$t_r, t_f$	Output Rise/Fall Time Q, /Q (20% to 80%)	—	120	170	—	130	180	—	150	230	ps	

**Notes:**

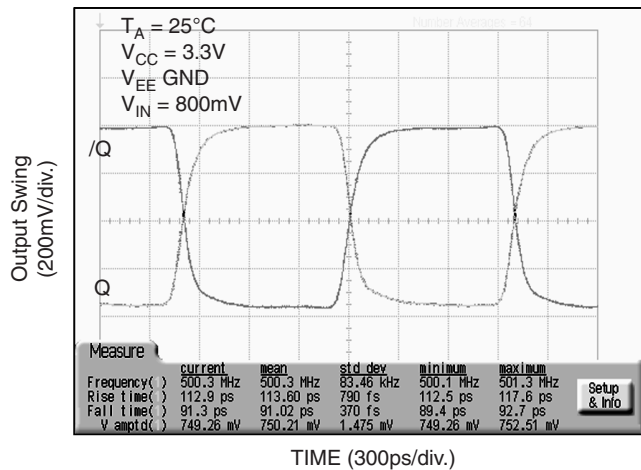
- Measured with 750mV input signal, 50% duty cycle. Output swing  $\geq 400mV$ . All loading with a  $50\Omega$  to  $V_{CC} - 2.0V$ .
- Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
- RJ is measured with a K28.7 comma detect character pattern, measured at 1.25Gbps and 2.5Gbps.
- DJ is measured at 1.25Gbps and 2.5Gbps, with both K28.5 and  $2^{23}-1$  PRBS pattern.

## TYPICAL OPERATING CHARACTERISTICS

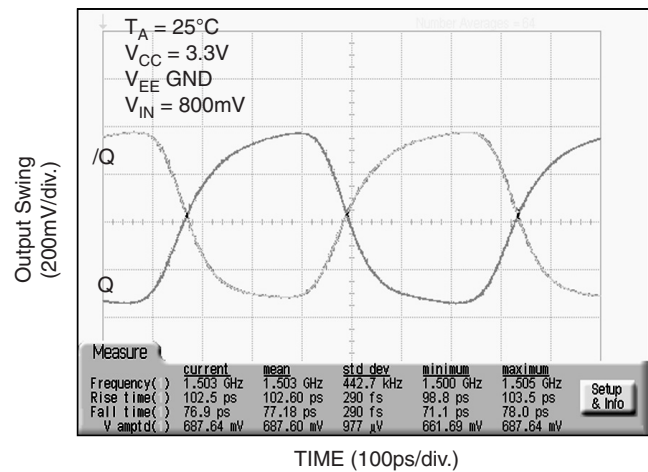
$V_{CC} = 3.3V$ ,  $V_{EE} = GND$ ,  $T_A = 25^\circ C$ , unless otherwise stated.



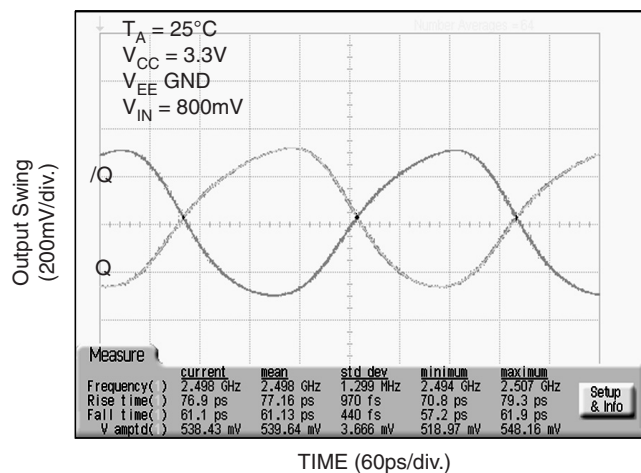
500MHz Output



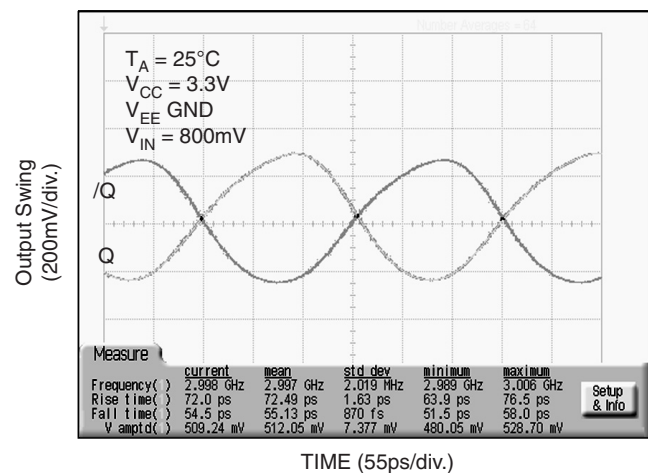
1.5GHz Output



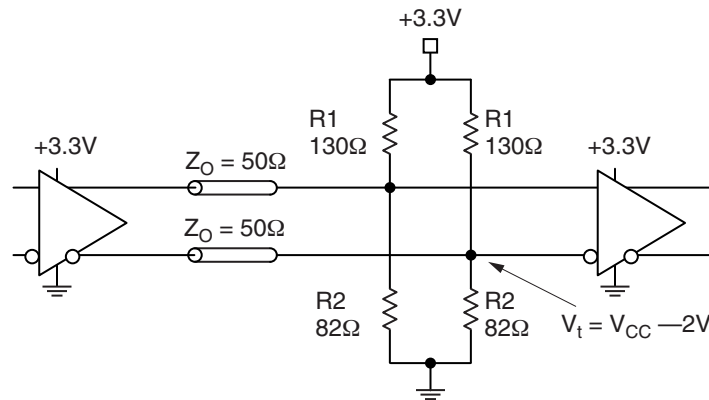
2.5GHz Output



3.0GHz Output



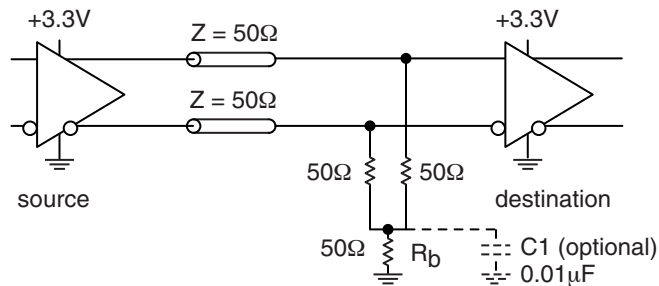
## TERMINATION RECOMMENDATIONS



**Figure 1. Parallel Termination–Thevenin Equivalent**

**Note:**

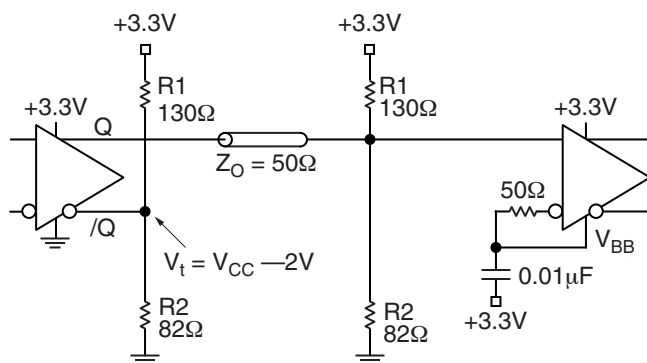
1. For +5.0V systems: R1 = 82Ω, R2 = 130Ω.



**Figure 2. Three-Resistor ‘Y–Termination’**

**Notes:**

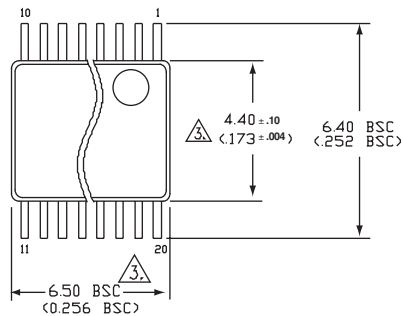
1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3.  $R_b$  resistor sets the DC bias voltage, equal to  $V_t$ . For +3.3V systems  $R_b = 46\Omega$  to  $50\Omega$ . For +5V systems,  $R_b = 110\Omega$ .



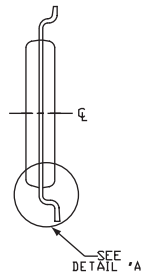
**Figure 3. Terminating Unused I/O**

**Notes:**

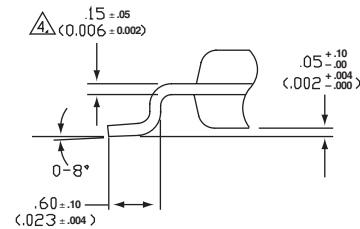
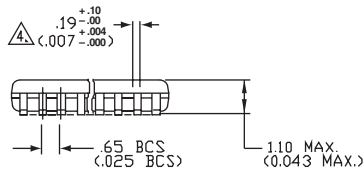
1. Unused output (/Q) must be terminated to balance the output.
2. Micrel's differential I/O logic devices include a  $V_{BB}$  reference pin.
3. Connect unused input through 50Ω to  $V_{BB}$ . Bypass with a 0.01μF capacitor to  $V_{CC}$ , not GND, as PECL is referenced to  $V_{CC}$ .
4. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω.

**20-PIN TSSOP (K4-20-1)**

TOP VIEW



END VIEW

DETAIL 'A'  
(VIEW ROTATED 90° C.W.)

SIDE VIEW

## NOTES:

1. DIMENSIONS ARE IN MM(INCHES).
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254(0.010) MAX.
4. THIS DIMENSION INCLUDES LEAD FINISH.

Rev.01

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