

8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs

High-Performance Silicon-Gate CMOS

MC74HC595A, MC74HCT595A

The MC74HC595A/MC74HCT595A consists of an 8-bit shift register and an 8-bit D-type latch with three-state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8-bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

The device directly interfaces with the SPI serial data port on CMOS MPUs and MCUs. The MC74HC595A device inputs are compatible Standard CMOS outputs; with pullup resistors, they are compatible with TTL outputs. The MC74HCT595A device inputs are compatible Standard CMOS or TTL outputs.

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- Improvements over HC595/HCT595
 - ◆ Improved Propagation Delays
 - ◆ 50% Lower Quiescent Power
 - ◆ Improved Input Noise and Latchup Immunity
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



SOIC-16
D SUFFIX
CASE 751B

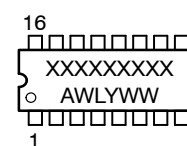


TSSOP-16
DT SUFFIX
CASE 948F

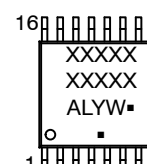


QFN16
MN SUFFIX
CASE 485AW

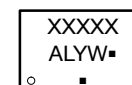
MARKING DIAGRAMS



SOIC-16



TSSOP-16



QFN16

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G, ■	= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

MC74HC595A, MC74HCT595A

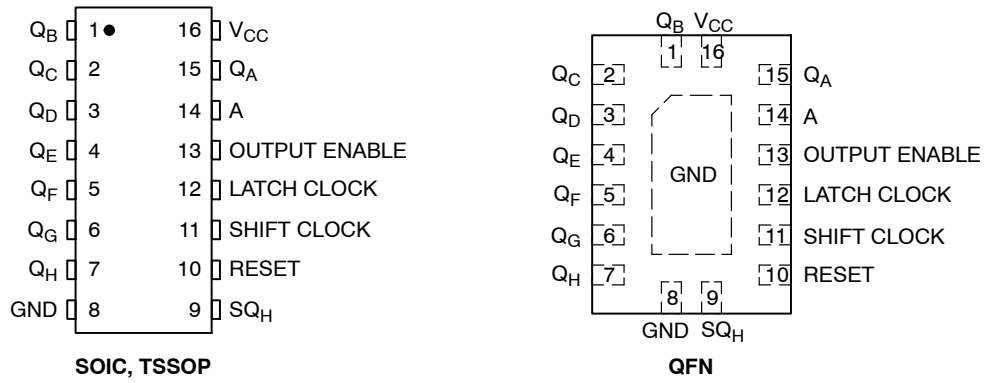
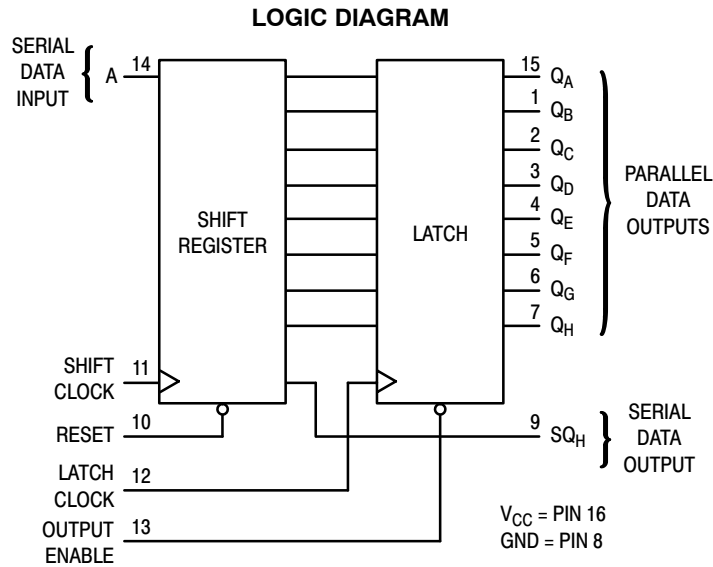


Figure 1. Pin Assignments



MC74HC595A, MC74HCT595A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V _{CC}	DC Supply Voltage	−0.5 to +6.5	V	
V _{IN}	DC Input Voltage	−0.5 to V _{CC} + 0.5	V	
V _{OUT}	DC Output Voltage	−0.5 to V _{CC} + 0.5	V	
I _{IN}	DC Input Current, per Pin	±20	mA	
I _{OUT}	DC Output Current, per Pin	±35	mA	
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA	
I _{IK}	Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{CC})	±20	mA	
I _{OK}	Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{CC})	±20	mA	
T _{STG}	Storage Temperature	−65 to +150	°C	
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C	
T _J	Junction Temperature Under Bias	±150	°C	
θ _{JA}	Thermal Resistance (Note 1)	SOIC−16 QFN16 TSSOP−16	126 118 159	°C/W
P _D	Power Dissipation in Still Air at 25°C	SOIC−16 QFN16 TSSOP−16	995 1062 787	mW
MSL	Moisture Sensitivity	Level 1	–	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	–
V _{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	>3000 >1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
MC74HC				
V _{CC}	DC Supply Voltage	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Note 3)	0	V _{CC}	V
T _A	Operating Free-Air Temperature	−55	+125	°C
t _r , t _f	Input Rise or Fall Time	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 500 400	ns
MC74HCT				
V _{CC}	DC Supply Voltage	4.5	5.5	V
V _{IN} , V _{OUT}	DC Input Voltage, DC Output Voltage (Note 3)	0	V _{CC}	V
T _A	Operating Free-Air Temperature	−55	+125	°C
t _r , t _f	Input Rise or Fall Time	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MC74HC595A, MC74HCT595A

DC ELECTRICAL CHARACTERISTICS (MC74HC595A)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage, Q _A - Q _H	V _{IN} = V _{IH} or V _{IL}					V
		I _{OUT} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	
		I _{OUT} ≤ 2.4 mA	3.0	2.48	2.34	2.2	
		I _{OUT} ≤ 6.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Minimum Low-Level Output Voltage, Q _A - Q _H	V _{IN} = V _{IH} or V _{IL}					V
		I _{OUT} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	
		I _{OUT} ≤ 2.4 mA	3.0	0.26	0.33	0.4	
		I _{OUT} ≤ 6.0 mA	4.5	0.26	0.33	0.4	
V _{OH}	Minimum High-Level Output Voltage, SQ _H	V _{IN} = V _{IH} or V _{IL}					V
		I _{OUT} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	
		I _{OUT} ≤ 2.4 mA	3.0	2.48	2.34	2.2	
		I _{OUT} ≤ 4.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Minimum Low-Level Output Voltage, SQ _H	V _{IN} = V _{IH} or V _{IL}					V
		I _{OUT} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	
		I _{OUT} ≤ 2.4 mA	3.0	0.26	0.33	0.4	
		I _{OUT} ≤ 4.0 mA	4.5	0.26	0.33	0.4	
I _{IN}	Maximum Input Leakage Current	V _{IN} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{IN} = V _{IL} or V _{IH} V _{OUT} = V _{CC} or GND	6.0	±0.5	±5.0	±10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = V _{CC} or GND	6.0	4.0	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC74HC595A, MC74HCT595A

AC ELECTRICAL CHARACTERISTICS (MC74HC595A)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Shift Clock to SQ _H (Figures 1 and 7)	2.0 3.0 4.5 6.0	140 100 28 24	175 125 35 30	210 150 42 36	ns
t _{PHL}	Maximum Propagation Delay, Reset to SQ _H (Figures 2 and 7)	2.0 3.0 4.5 6.0	145 100 29 25	180 125 36 31	220 150 44 38	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Clock to Q _A – Q _H (Figures 3 and 7)	2.0 3.0 4.5 6.0	140 100 28 24	175 125 35 30	210 150 42 36	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q _A – Q _H (Figures 4 and 8)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q _A – Q _H (Figures 4 and 8)	2.0 3.0 4.5 6.0	135 90 27 23	170 110 34 29	205 130 41 35	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Q _A – Q _H (Figures 3 and 7)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 31 18 15	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, SQ _H (Figures 1 and 7)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C _{in}	Maximum Input Capacitance	–	10	10	10	pF
C _{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State), Q _A – Q _H	–	15	15	15	pF
			Typical @ 25°C, V _{CC} = 5.0 V			
C _{PD}	Power Dissipation Capacitance (Per Package)*	300			pF	

MC74HC595A, MC74HCT595A

TIMING REQUIREMENTS (MC74HC595A)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to –55°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0	50	65	75	ns
		3.0	40	50	60	
		4.5	10	13	15	
		6.0	9.0	11	13	
t _{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0	75	95	110	ns
		3.0	60	70	80	
		4.5	15	19	22	
		6.0	13	16	19	
t _h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0	5.0	5.0	5.0	ns
		3.0	5.0	5.0	5.0	
		4.5	5.0	5.0	5.0	
		6.0	5.0	5.0	5.0	
t _{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0	50	65	75	ns
		3.0	40	50	60	
		4.5	10	13	15	
		6.0	9.0	11	13	
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0	60	75	90	ns
		3.0	45	60	70	
		4.5	12	15	18	
		6.0	10	13	15	
t _w	Minimum Pulse Width, Shift Clock (Figure 1)	2.0	50	65	75	ns
		3.0	40	50	60	
		4.5	10	13	15	
		6.0	9.0	11	13	
t _w	Minimum Pulse Width, Latch Clock (Figure 6)	2.0	50	65	75	ns
		3.0	40	50	60	
		4.5	10	13	15	
		6.0	9.0	11	13	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

MC74HC595A, MC74HCT595A

DC ELECTRICAL CHARACTERISTICS (MC74HCT595A)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High–Level Input Voltage	V _{out} = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA	4.5 to 5.5	2.0	2.0	2.0	V
V _{IL}	Maximum Low–Level Input Voltage	V _{out} = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA	4.5 to 5.5	0.8	0.8	0.8	V
V _{OH}	Minimum High–Level Output Voltage, Q _A – Q _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5	4.4	4.4	4.4	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low–Level Output Voltage, Q _A – Q _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5	0.1	0.1	0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA	4.5	0.26	0.33	0.4	
V _{OH}	Minimum High–Level Output Voltage, SQ _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5	4.4	4.4	4.4	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low–Level Output Voltage, SQ _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5	0.1	0.1	0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA	4.5	0.26	0.33	0.4	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I _{OZ}	Maximum Three–State Leakage Current, Q _A – Q _H	Output in High–Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	5.5	± 0.5	± 5.0	± 10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	5.5	4.0	40	160	μA
ΔI _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0μA	5.5	≥ –55°C	25 to 125°C		mA
				2.9	2.4		

MC74HC595A, MC74HCT595A

AC ELECTRICAL CHARACTERISTICS (MC74HCT595A)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	4.5 to 5.5	30	24	20	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Shift Clock to SQ _H (Figures 1 and 7)	4.5 to 5.5	28	35	42	ns
t _{PHL}	Maximum Propagation Delay, Reset to SQ _H (Figures 2 and 7)	4.5 to 5.5	29	36	44	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Clock to Q _A – Q _H (Figures 3 and 7)	4.5 to 5.5	28	35	42	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q _A – Q _H (Figures 4 and 8)	4.5 to 5.5	30	38	45	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q _A – Q _H (Figures 4 and 8)	4.5 to 5.5	27	34	41	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Q _A – Q _H (Figures 3 and 7)	4.5 to 5.5	12	15	18	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, SQ _H (Figures 1 and 7)	4.5 to 5.5	15	19	22	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State), Q _A – Q _H	—	15	15	15	pF

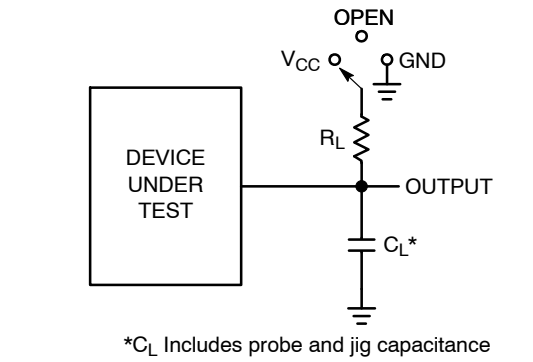
C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		300	

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (MC74HCT595A)

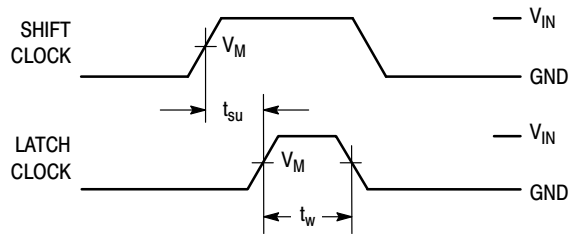
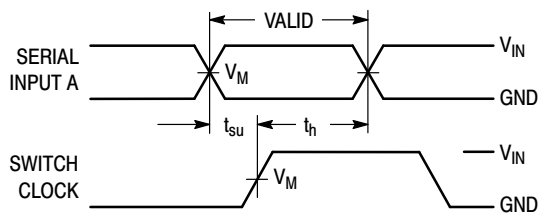
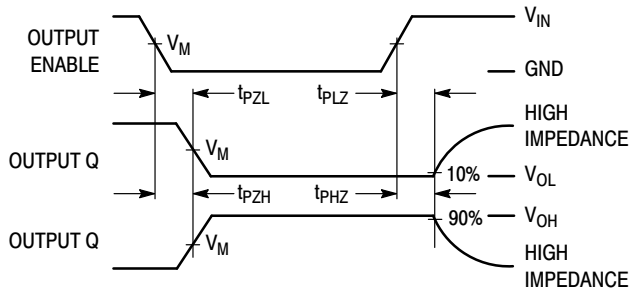
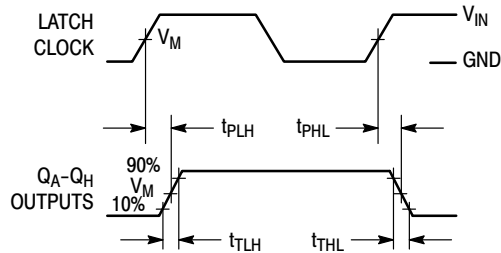
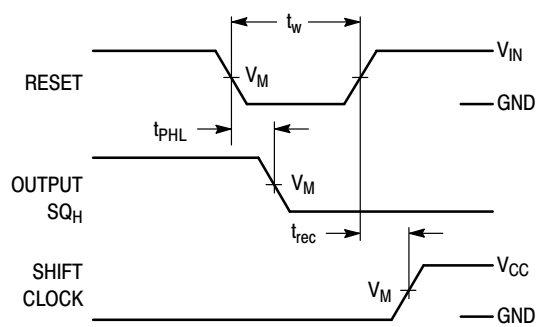
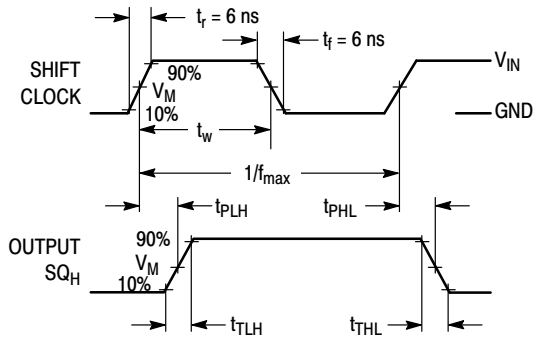
Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to –55°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	4.5 to 5.5	10	13	15	ns
t _{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	4.5 to 5.5	15	19	22	ns
t _h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	4.5 to 5.5	5.0	5.0	5.0	ns
t _{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	4.5 to 5.5	10	13	15	ns
t _w	Minimum Pulse Width, Reset (Figure 2)	4.5 to 5.5	12	15	18	ns
t _w	Minimum Pulse Width, Shift Clock (Figure 1)	4.5 to 5.5	10	13	15	ns
t _w	Minimum Pulse Width, Latch Clock (Figure 6)	4.5 to 5.5	10	13	15	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	4.5 to 5.5	500	500	500	ns

MC74HC595A, MC74HCT595A



Test	Switch Position	C _L	R _L
t _{PLH} / t _{PHL}	Open	50 pF	1 kΩ
t _{PLZ} / t _{PZL}	V _{CC}		
t _{PHZ} / t _{PZH}	GND		

Figure 1. Test Circuit



Device	V _{IN} , V	V _m , V
MC74HC595A	V _{CC}	50% x V _{CC}
MC74HCT595A	3 V	1.3 V

Figure 2. Switching Waveforms

MC74HC595A, MC74HCT595A

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output SQ _H	Parallel Outputs Q _A – Q _H
Reset shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	D → SR _A ; SR _N → SR _{N+1}	U	SR _G → SR _H	U
Shift register remains unchanged	H	X	L, H, ↓	L, H, ↓	L	U	U	U	U
Transfer shift register contents to latch register	H	X	L, H, ↓	↑	L	U	SR _N → LR _N	U	SR _N
Latch register remains unchanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents
LR = latch register contents

D = data (L, H) logic level
U = remains unchanged

↑ = Low-to-High
↓ = High-to-Low

* = depends on Reset and Shift Clock inputs
** = depends on Latch Clock input

PIN DESCRIPTIONS

INPUTS

A (Pin 14)

Serial Data Input. The data on this pin is shifted into the 8-bit serial shift register.

CONTROL INPUTS

Shift Clock (Pin 11)

Shift Register Clock Input. A low-to-high transition on this input causes the data at the Serial Input pin to be shifted into the 8-bit shift register.

Reset (Pin 10)

Active-low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8-bit latch is not affected.

Latch Clock (Pin 12)

Storage Latch Clock Input. A low-to-high transition on this input latches the shift register data.

Output Enable (Pin 13)

Active-low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs (Q_A–Q_H) into the high-impedance state. The serial output is not affected by this control unit.

OUTPUTS

Q_A – Q_H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

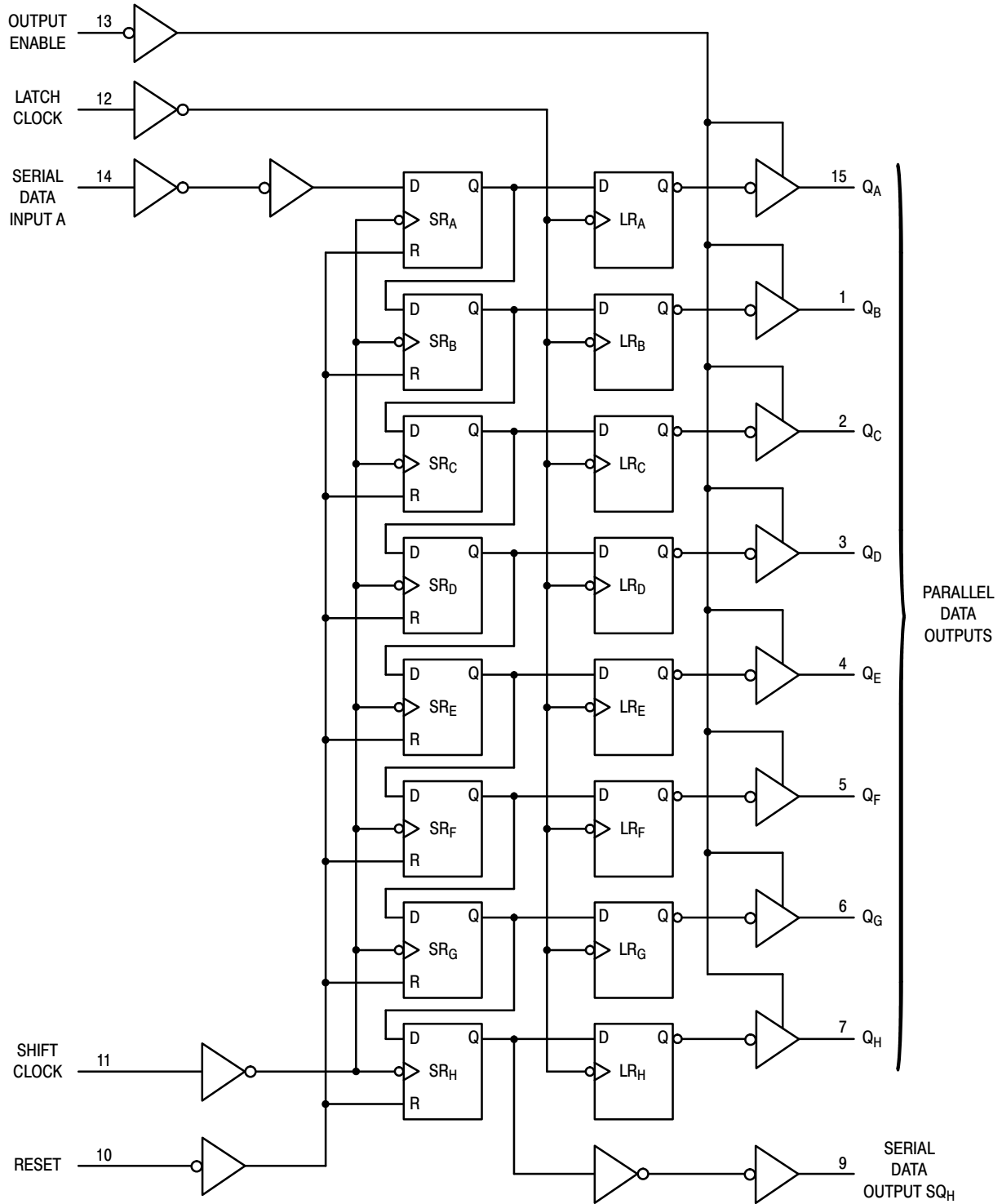
Noninverted, 3-state, latch outputs.

SQ_H (Pin 9)

Noninverted, Serial Data Output. This is the output of the eighth stage of the 8-bit shift register. This output does not have three-state capability.

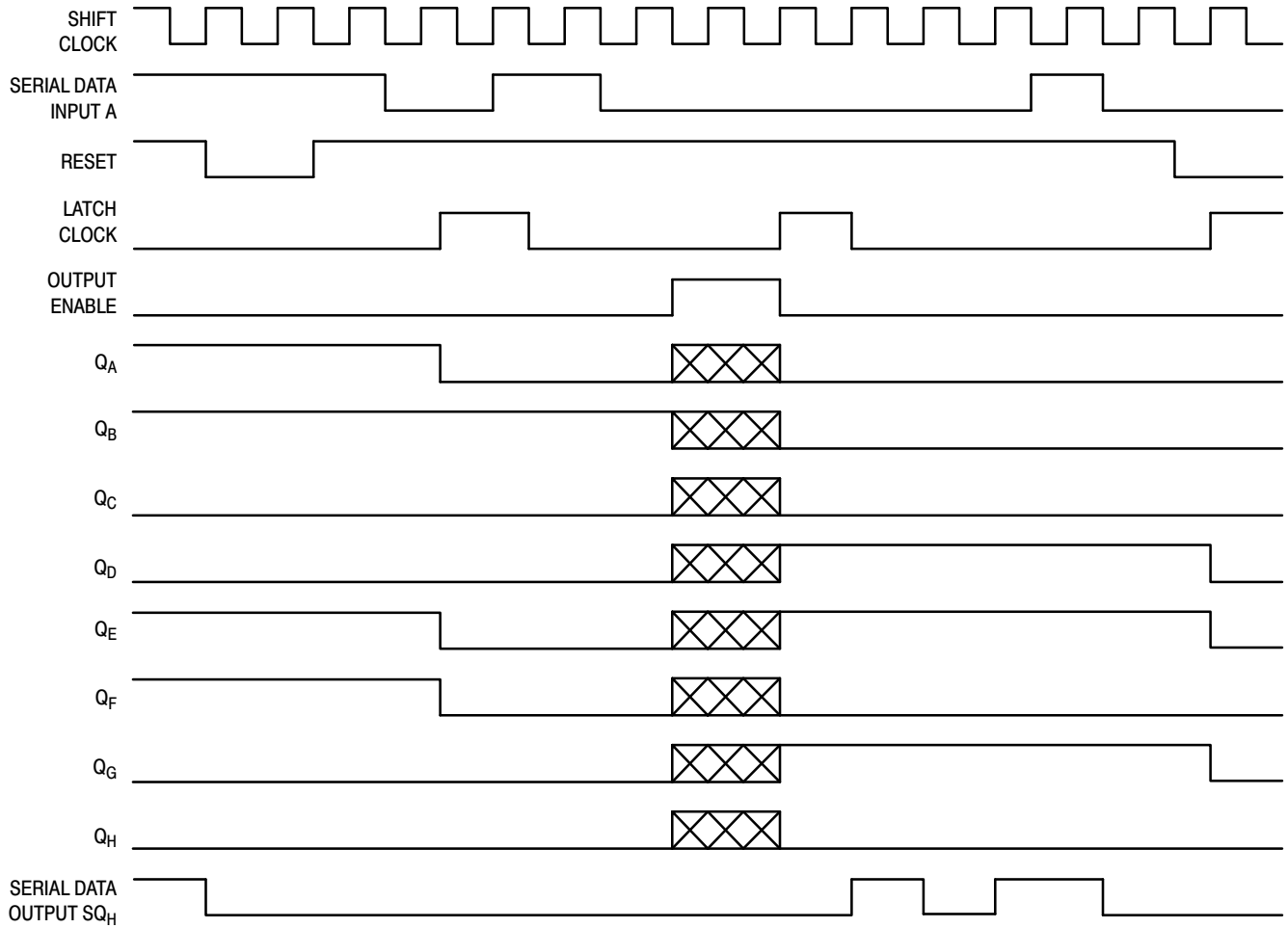
MC74HC595A, MC74HCT595A

EXPANDED LOGIC DIAGRAM



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TIMING DIAGRAM



NOTE:  implies that the output is in a high-impedance state.

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ORDERING INFORMATION

Device	Package	Marking	Shipping [†]
MC74HC595ADG	SOIC-16	HC595A	48 Units / Rail
MC74HC595ADR2G	SOIC-16	HC595A	2500 / Tape & Reel
MC74HC595ADR2G-Q*	SOIC-16	HC595A	2500 / Tape & Reel
MC74HC595ADTG	TSSOP-16	HC 595A	96 Units / Rail
MC74HC595ADTR2G	TSSOP-16	HC 595A	2500 / Tape & Reel
MC74HC595ADTR2G-Q*	TSSOP-16	HC 595A	2500 / Tape & Reel
MC74HC595AMN1TWG-Q*	QFN16	V595A	3000 / Tape & Reel (8mm pitch carrier tape)
MC74HCT595ADG	SOIC-16	HCT595A	48 Units / Rail
MC74HCT595ADR2G	SOIC-16	HCT595A	2500 / Tape & Reel
MC74HCT595ADTG	TSSOP-16	HCT 595A	96 Units / Rail
MC74HCT595ADTR2G	TSSOP-16	HCT 595A	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable



DATE 11 DEC 2008



1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

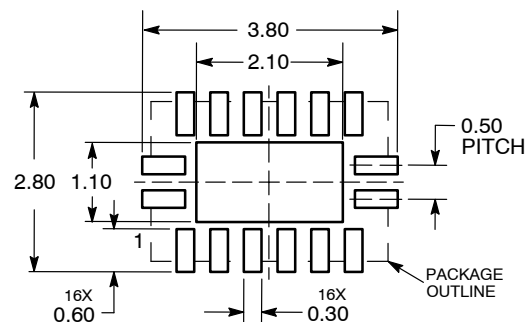
DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

XXXX
ALYW■

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

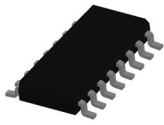
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

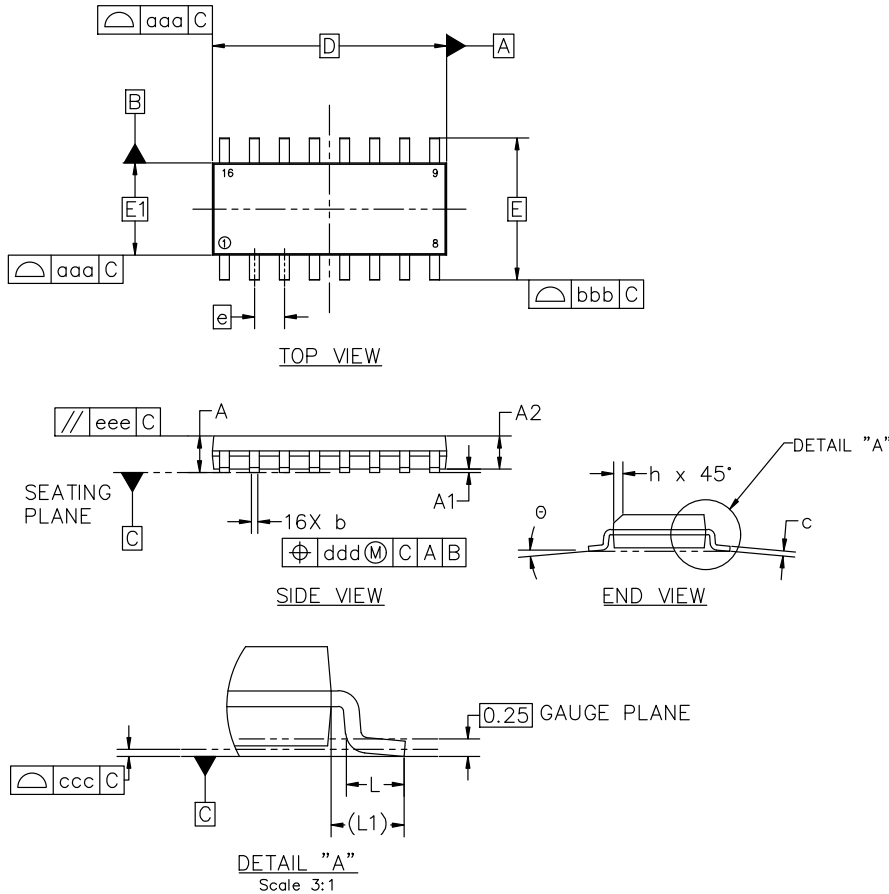
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SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

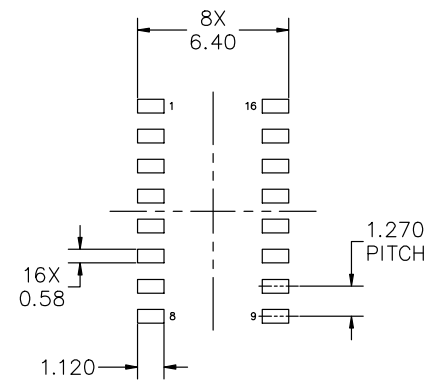
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE onsemi SOLDERING
AND MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERM/D

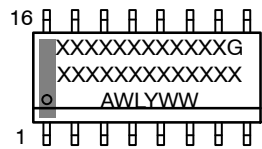
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DESCRIPTION:	SOIC-16 9.90X3.90X1.37 1.27P	PAGE 1 OF 2

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SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC
MARKING DIAGRAM*

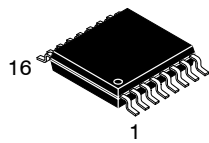


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

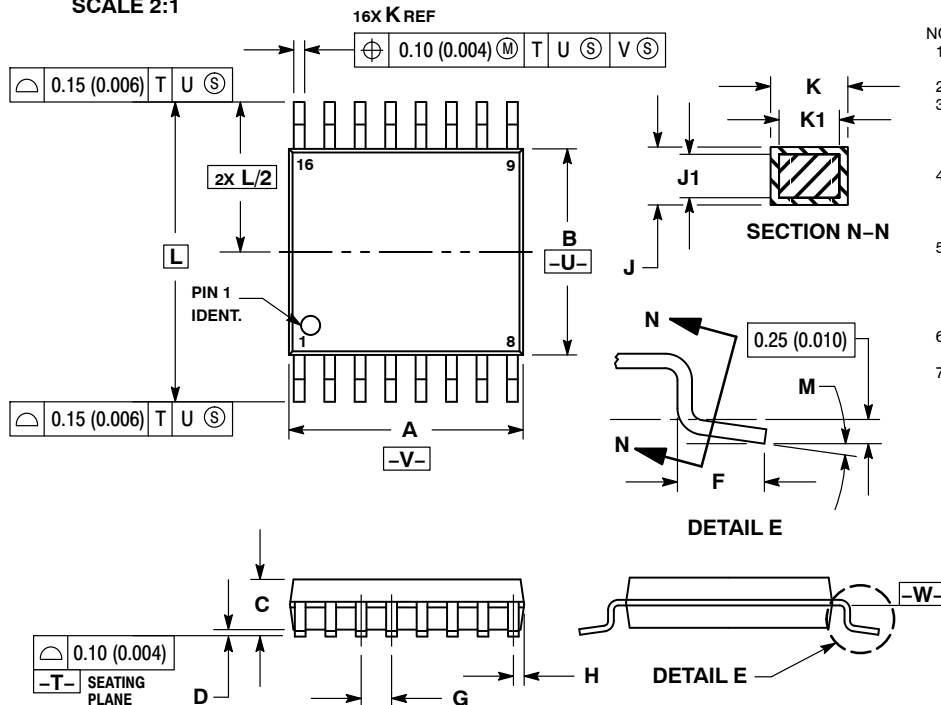
STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR	STYLE 2: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE	STYLE 3: PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4	STYLE 4: PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1
STYLE 5: PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE	STYLE 7: PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH	

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TSSOP-16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

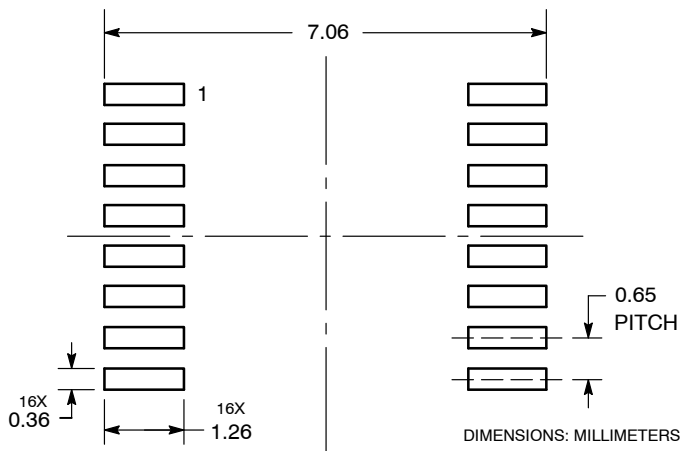


NOTES:

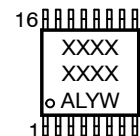
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED
SOLDERING FOOTPRINT*



GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	TSSOP-16	PAGE 1 OF 1

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