

## Phase Shifter, S-Band, 6 Bit 2.3-4.1 GHz

**MAPCGM0003**  
903218 B

### Features

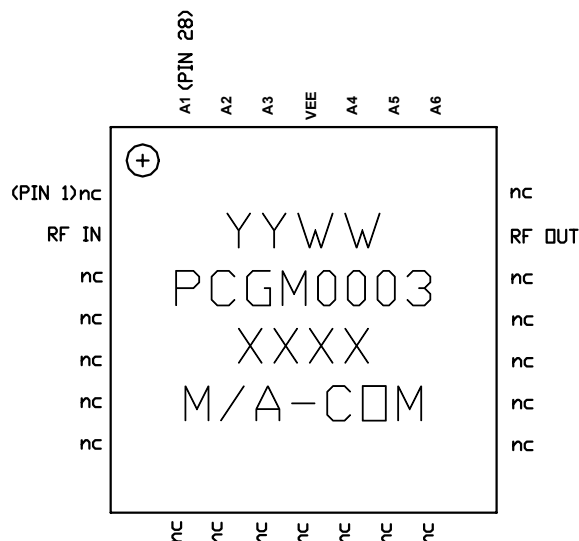
- ◆ 2.3 to 4.1 GHz Operation
- ◆ 6 Bit Phase Shifter
- ◆ 360° Coverage, LSB = 5.6°
- ◆ TTL Control Inputs
- ◆ MSAG™ Process
- ◆ 6mm, 28 Lead, PQFN Package

### Description

The MAPCGM0003 is a 6-bit Phase Shifter with Parallel TTL Input Control and is packaged in a micro lead package (MLP). This product is fully matched to 50 ohms on both the input and output. This part has 360° of phase coverage in 5.6° increments.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate MSAG™ Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.



### Primary Applications

| Pin Number | Designation   |
|------------|---------------|
| 2          | RF IN         |
| 20         | RF OUT        |
| 22         | A6 (180°)     |
| 23         | A5 (90°)      |
| 24         | A4 (45°)      |
| 25         | VEE           |
| 26         | A3 (22.5°)    |
| 27         | A2 (11.25°)   |
| 28         | A1 (5.6°)     |
| 1,3-19,21  | No connection |

### Maximum Operating Conditions <sup>1</sup>

| Parameter            | Symbol           | Absolute Maximum | Units |
|----------------------|------------------|------------------|-------|
| Input Power          | P <sub>IN</sub>  | 30               | dBm   |
| Supply Voltage       | V <sub>EE</sub>  | -6               | V     |
| Junction Temperature | T <sub>J</sub>   | 180              | °C    |
| Storage Temperature  | T <sub>STG</sub> | -55 to +150      | °C    |

**1. Operation outside of these ranges may reduce product reliability. Operation at other than the typical values may result in performance outside the guaranteed limits.**

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**Recommended Operating Conditions**

| Characteristic       | Symbol         | Min  | Typ  | Max  | Unit |
|----------------------|----------------|------|------|------|------|
| Supply Voltage       | VEE            | -5.2 | -5.0 | -4.8 | V    |
| Control Voltage      | A1 thru A6     |      |      |      |      |
| Logic High           |                | 3    | 5    | 5    | V    |
| Logic Low            |                | 0    | 0    | 0.4  | V    |
| Junction Temperature | T <sub>J</sub> |      |      | 150  | °C   |

**Electrical Characteristics (25°C, Z<sub>0</sub> = 50Ω, V<sub>EE</sub> = -5V)**

| Parameter                                      | Symbol                         | Minimum | Typical <sup>3</sup> | Maximum | Units |
|------------------------------------------------|--------------------------------|---------|----------------------|---------|-------|
| Bandwidth                                      | f                              | —       | 2.3-4.1              | —       | GHz   |
| Insertion Loss                                 | IL                             | 4       | 6                    | 10      | dB    |
| Input VSWR (At Reference)                      | VSWR                           | —       | 1.5:1                | 4.4:1   |       |
| Output VSWR (At Reference)                     | VSWR                           | —       | 1.2:1                | 2.3:1   |       |
| RMS Phase Error                                | RMS                            | —       | 6                    | —       | °     |
| RMS Phase Error — Calibrated                   | RMS                            | —       | 3                    | —       | °     |
| Phase Range                                    | ΔΦ                             | —       | 360                  | —       | °     |
| Phase Accuracy — 5.6° Bit                      | ΔΦ <sub>REF</sub> <sup>3</sup> | -7.2    | -5.6                 | -4.2    | °     |
| Phase Accuracy — 11.2° Bit                     | ΔΦ <sub>REF</sub>              | -11.8   | -11.2                | -8.4    | °     |
| Phase Accuracy — 22.5° Bit                     | ΔΦ <sub>REF</sub>              | -34     | -22.5                | -16     | °     |
| Phase Accuracy — 45° Bit                       | ΔΦ <sub>REF</sub>              | -59     | -45                  | -35     | °     |
| Phase Accuracy — 90° Bit                       | ΔΦ <sub>REF</sub>              | -98     | -90                  | -84     | °     |
| Phase Accuracy — 180° Bit                      | ΔΦ <sub>REF</sub>              | -200    | -180                 | -170    | °     |
| Phase Accuracy — All Bits                      | ΔΦ <sub>REF</sub>              | -390    | -360                 | -340    | °     |
| Gain Variation over all Phase Shifter settings | ΔG                             | —       | < 3                  | —       | dB    |
| Digital Supply Current                         | I <sub>EE</sub>                | —       | < 10                 | —       | mA    |
| Input Third Order Intercept                    | ITOI                           | —       | 36                   | —       | dBm   |
| Input 1-dB Compression Point                   | P <sub>1dB</sub>               | —       | 23                   | —       | dBm   |

**2. Typical values shown for reference only.**

**3. All ΔΦ<sub>REF</sub> values are relative to the Reference State (i.e. All phase bits set to 0V).**

**Operating Instructions**

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V<sub>EE</sub> = -5 V.
2. Apply Logic Voltages to control circuit as listed in Recommended Operating Conditions Table.



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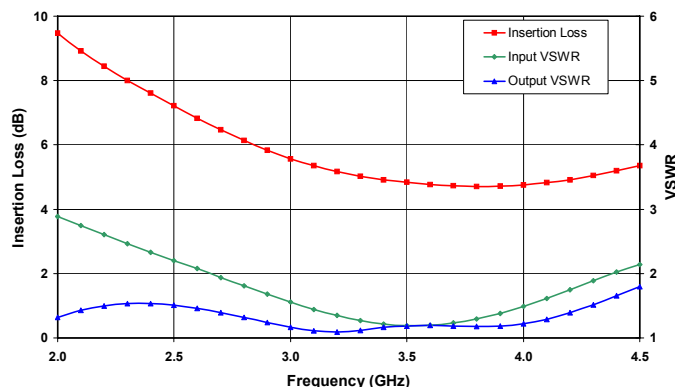


Figure 1. Reference State Insertion Loss, Input and Output VSWR vs. Frequency

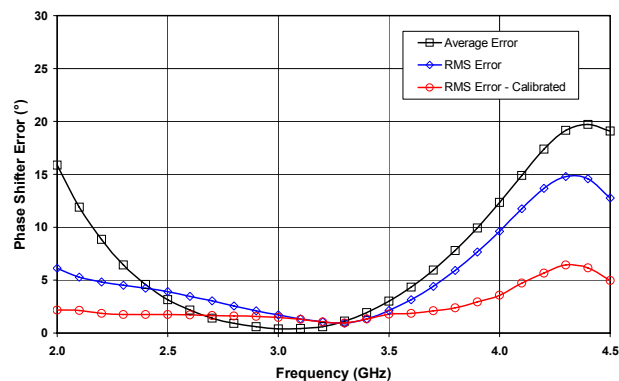


Figure 2. Phase Shifter Figures of Merit: Average Error vs. Reference State, RMS Error and Calibrated RMS Error Over All States

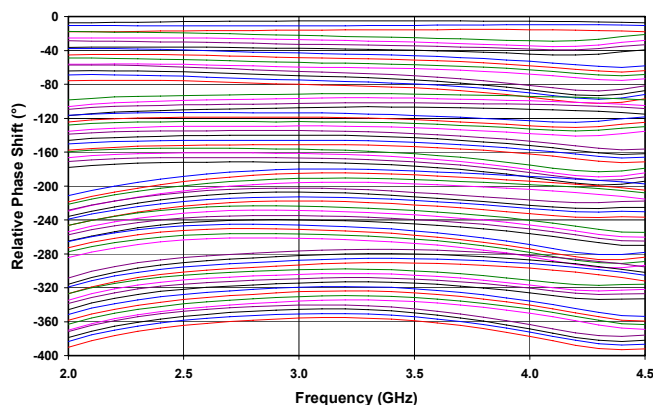


Figure 3. Relative Phase Shift vs. Phase Shifter State

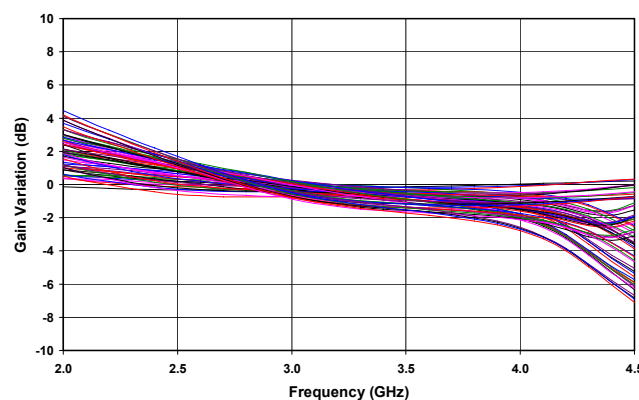


Figure 4. Relative Gain Change vs. Phase Shifter State

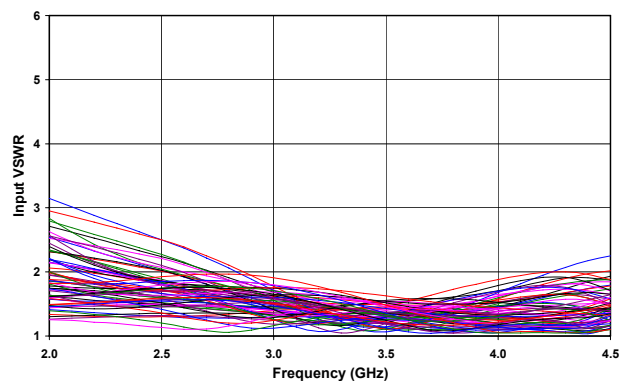


Figure 5. Input VSWR vs. Phase Shifter State

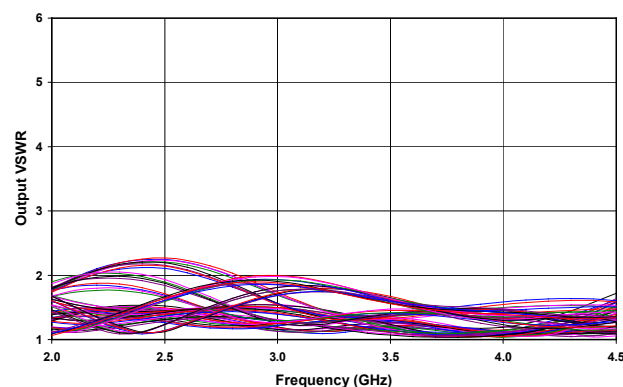
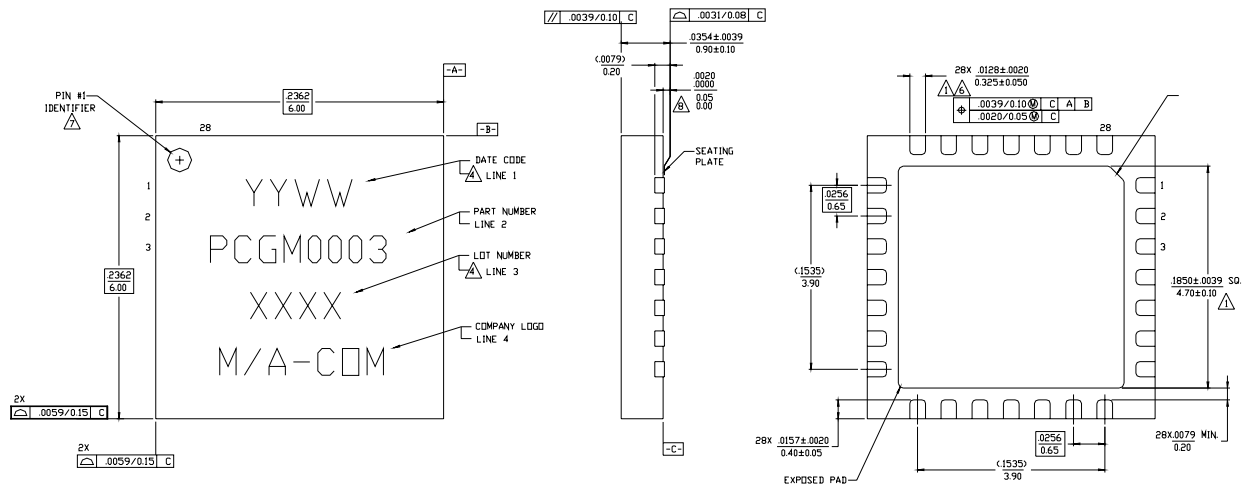


Figure 6. Output VSWR vs. Phase Shifter State

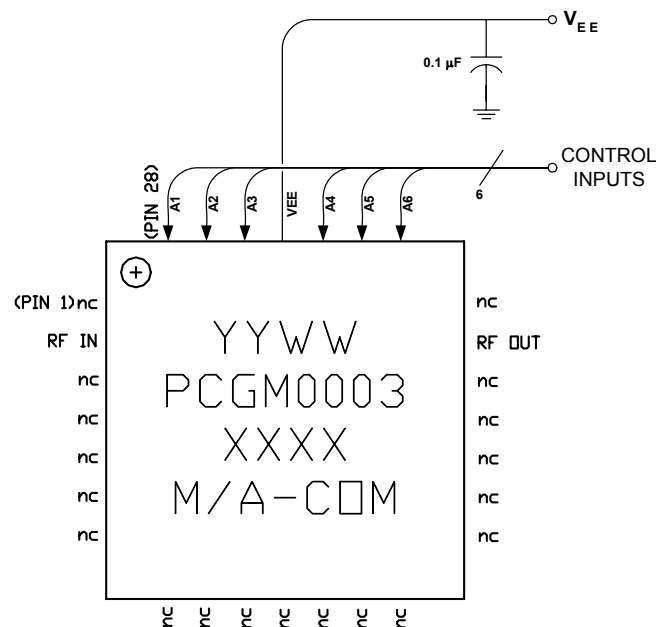
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### Figure 7. PQFN, 6mm, 28 Lead Package Drawing

Reference JEDEC M0-220 (see <http://www.jedec.org>), VAR. VJJC-3 (Issue E) for additional dimensional and tolerance information.



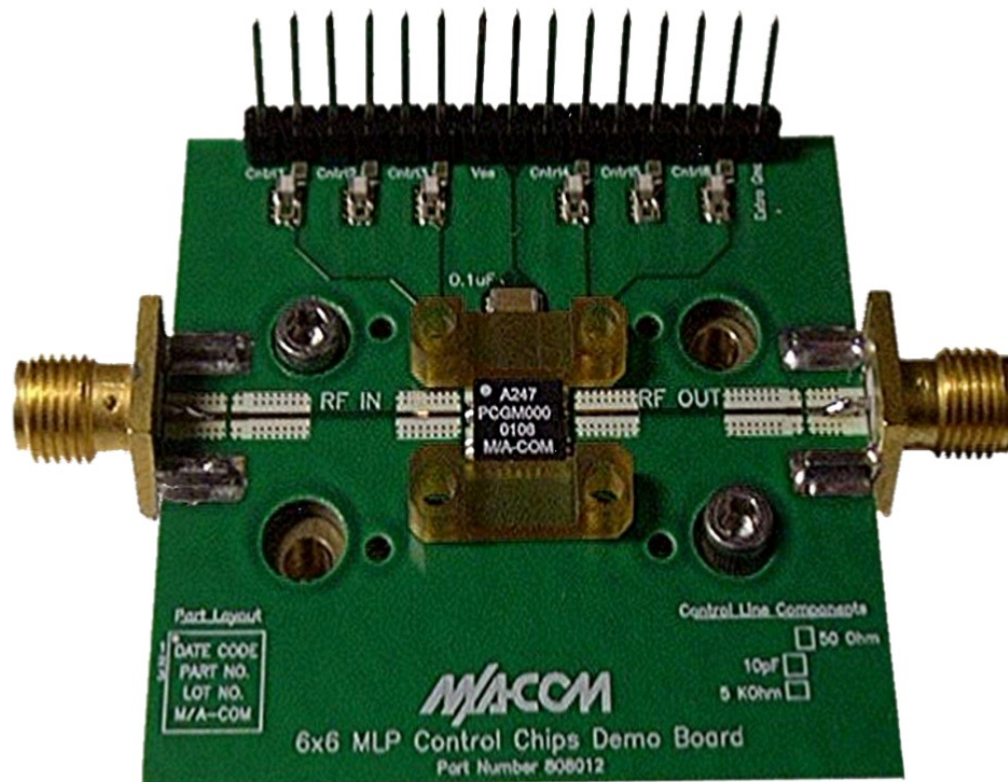
### Figure 8. Recommended Bias Configuration

Refer to M/A-COM Application Note ***Surface Mounting Instructions for PQFN Packages #S2083\**** for assembly guidelines.

Application Notes can be found by going to the Site Search Page on M/A-COM's web page (<http://www.macom.com/search/search.jsp>) and searching for the required Application Note.

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**Figure 9. Demonstration Board (available upon request).**