TH8080

SoloLIN Transceiver

Features

- Compatible to LIN Specification Version 1.3 and 2.0
- Compatible to ISO9141 functions
- Baud rate up to 20 kBaud
- Operating voltage V_S = 7 to 18 V
- Low current consumption of typ. 24µA
- Wake-up via LIN bus traffic
- Slew rate control for good EME behavior
- High EMI immunity
- Fully integrated receiver filter
- Bus terminals proof against short-circuits and transients in the automotive environment
- High impedance BUS pin in case of loss of ground and undervoltage condition
- High signal symmetry for using in RC – based slave nodes up to 2% clock tolerance
- Automotive Temperature Range of –40°C to 125°C
- CMOS compatible interface to microcontroller
- Thermal overload protection
- Load dump protection (40V)
- ±4kV ESD protection
- Small SOIC8 package

Ordering Information

Part No.	***Temperature Range***	***Package***
TH8080 KDC	K (-40 to 125 °C)	DC (SOIC8)

General Description

The TH8080 is a physical layer device for a single wire data link capable of operating in applications where high data rate is not required and a lower data rate can achieve cost reductions in both the physical media components and in the microprocessor which use the network. The TH8080 is designed in accordance to the physical layer definition of the LIN Protocol Specification, Rev. 1.3 and 2.0.The IC furthermore can be used in ISO9141 systems.

Because of the very low current consumption of the TH8080 in recessive state it's suitable for ECU applications with hard standby current requirements, whereby no sleep/wake up control from the microprocessor is necessary.

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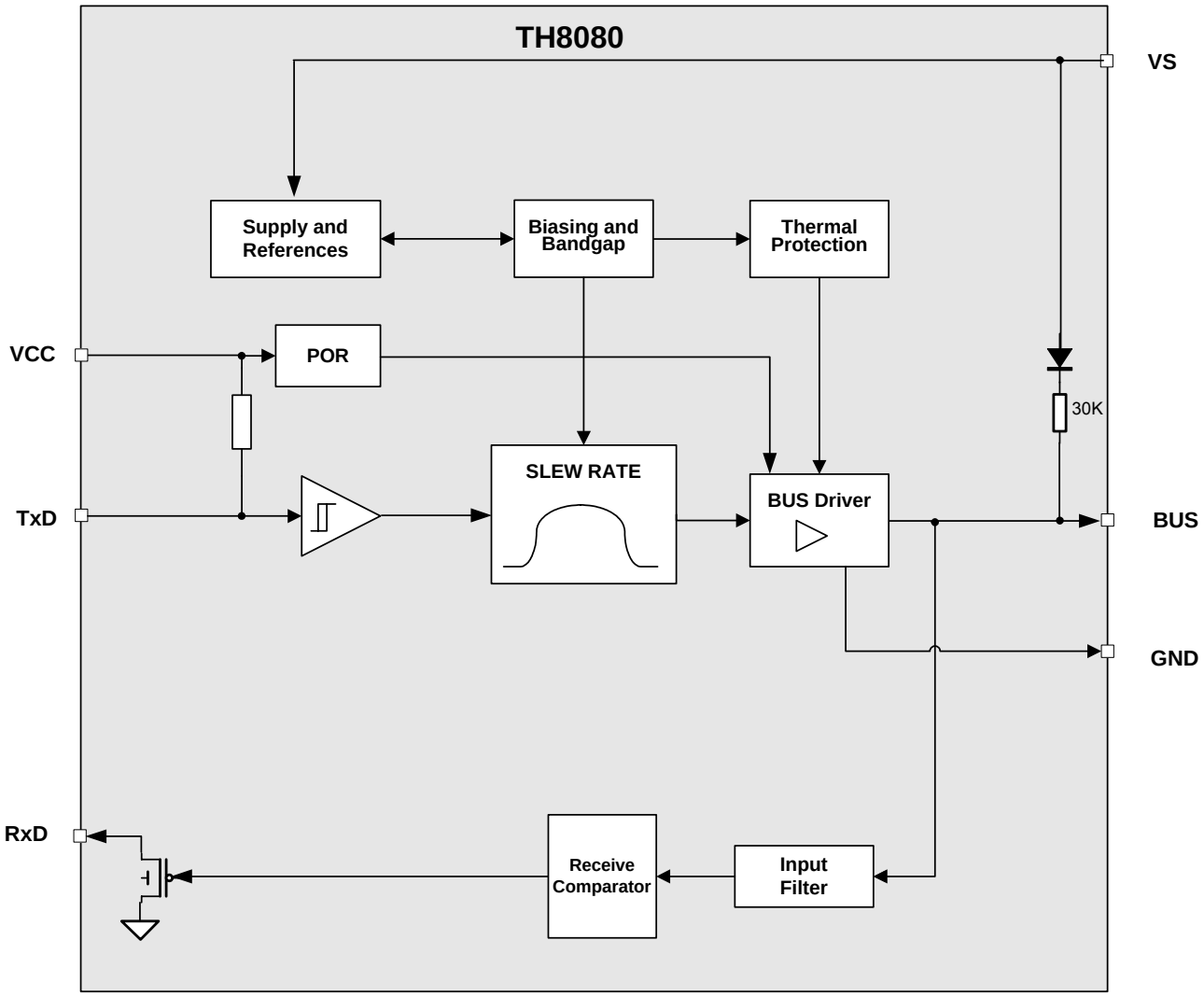


Figure 1 - Block Diagram

2. Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC.
The absolute maximum ratings (in accordance with IEC 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may effect the reliability of the device.

2.1 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Battery supply voltage [1]	V_S	7	18	V
Supply voltage	V_{CC}	4.5	5.5	V
Operating ambient temperature	T_{amb}	-40	+125	°C

[1] Vs is the IC supply voltage including voltage drop of reverse battery protection diode, V_{DROP} = 0.4 to 1V, V_{BAT_ECU} voltage range is 8 to 18V

2.2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Battery Supply Voltage	V_S	t < 1 min	-0.3	30	V
		Load dump, t < 500ms		40	
Supply Voltage	V_{CC}		-0.3	+7	V
Transient supply voltage	$V_{S.tr1}$	ISO 7637/1 pulse 1[1]	-150		V
Transient supply voltage	$V_{S..tr2}$	ISO 7637/1 pulses 2[1]		100	V
Transient supply voltage	$V_{S..tr3}$	ISO 7637/1 pulses 3A, 3B	-150	150	V
BUS voltage	V_{BUS}	t < 500ms , Vs = 18V	-27	40	V
		t < 500ms ,Vs = 0V	-40		
Transient bus voltage	$V_{BUS..tr1}$	ISO 7637/1 pulse 1 [2]	-150		V
Transient bus voltage	$V_{BUS.tr2}$	ISO 7637/1 pulses 2 [2]		100	V
Transient bus voltage	$V_{BUS.tr3}$	ISO 7637/1 pulses 3A, 3B [2]	-150	150	V
DC voltage on pins TxD, RxD	V_{DC}		-0.3	7	V
ESD capability of pin LIN,VS	ESD_{HB}	Human body model, equivalent to discharge 100pF with 1.5kΩ,	-4	4	kV
ESD capability of pin RxD, TxD, VCC	ESD_{HB}	Human body model, equivalent to discharge 100pF with 1.5kΩ,	-2	2	kV
Maximum latch - up free current at any Pin	I_{LATCH}		-500	500	mA
Thermal impedance	Θ_{JA}	in free air		152	K/W
Storage temperature	T_{stg}		-55	+150	°C
Junction temperature	T_{vj}		-40	+150	°C

[1] ISO 7637 test pulses are applied to VS via a reverse polarity diode and >2uF blocking capacitor.
[2] ISO 7637 test pulses are applied to BUS via a coupling capacitance of 1 nF.

2.3 Static Characteristics

Unless otherwise specified all values in the following tables are valid for V_S = 7 to 18V, V_{CC} = 4.5 to 5.5V and T_{AMB}= -40 to 125°C. All voltages are referenced to ground (GND), positive currents are flow into the IC.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PIN VS, VCC						
V_{CC} undervoltage lockout	V_{CC_UV}	V_S > 7V, TxD=L	2.75		4.3	V
Supply current, dominant	I_{Sd}	V_S = 18V,V_{CC} = 5.5V, TxD = L		1	3	mA
Supply current, dominant	I_{CCd}	V_S = 18V,V_{CC} = 5.5V, TxD = L		0.8	1.5	mA
Supply current, recessive	I_{Sr}	V_S = 18V,V_{CC} = 5.5V,TxD=open		10	20	µA
Supply current, recessive	I_{CCr}	V_S = 18V,V_{CC} = 5.5V,TxD=open		18	30	µA
Supply current, recessive	I_{Sr} + I_{CCr}	V_S = 12V,V_{CC} = 5V, TxD=open, T_{amb}= 25°		24		µA
PIN BUS – Transmitter						
Short circuit bus current [2] [3]	I_{BUS_LIM}	V_{BUS} = V_S, driver on		120	200	mA
Pull up current bus [2] [3]	I_{BUS_PU}	V_{BUS} = 0, V_S = 12V, driver off	-600		-200	mA
Bus reverse current, recessive [2] [3]	$I_{BUS\_PAS\_rec}$	V_{BUS} > V_S , 7V < V_{BUS} < 18V 7V < V_S < 18V, driver off			5	µA
Bus reverse current loss of battery [2] [3]	I_{BUS}	V_S = 0V, 0V < V_{BUS} < 18V			5	µA
Bus current during loss of Ground [2] [3]	$I_{BUS\_NO\_GND}$	V_S = 12V, 0 < V_{BUS} < 18V	-1		1	mA
Transmitter dominant voltage [1] [2]	$V_{BUSdom\_DRV\_2}$	VS = 7V, load = 500Ω			1.2	V
Transmitter dominant voltage [2]	$V_{BUSdom\_DRV\_3}$	V_S = 18V, load = 500Ω			2	V
Bus input capacitance [1]	C_{BUS}	Pulse response via 10kΩ, V_{PULSE}=12V, V_S open		25	35	pF
PIN BUS – Receiver						
Receiver dominant voltage [2] [3]	V_{BUSdom}		0.4 *V_S			V
Receiver recessive voltage [2] [3]	V_{BUSrec}				0.6 *V_S	V
Center point of receiver threshold [1] [2] [3]	V_{BUS_CNT}	V_{BUS_CNT} = (V_{BUSdom} + V_{BUSrec})/2	0.487 *V_S	0.5 *V_S	0.512 *V_S	V
Receiver hysteresis [1] [2] [3]	V_{HYS}	V_{BUS_CNTt} = (V_{BUSrec} -V_{BUSdom})		0.175 *V_S	0.187 *V_S	V
PIN TXD						
High level input voltage	V_{ih}	Rising edge			0.7*V_{CC}	V
Low level input voltage	V_{il}	Falling edge	0.3*V_{CC}			V
TxD pull up resistor	R_{IH_TXD}	V_{TxD} = 0V	10	15	20	kΩ
PIN RXD						
Low level output voltage	V_{ol_rxd}	I_{RxD} = 2mA			0.9	V
Leakage Current	V_{leak_rxd}	V_{RxD} = 5.5V, recessive	-10		10	µA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Protection						
Thermal shutdown	T_{sd} [1]		155		180	°C
Thermal recovery	T_{hys} [1]		126		150	°C

[1] No production test, guaranteed by design and qualification
[2] In accordance to LIN physical layer specification 1.3
[3] In accordance to LIN physical layer specification 2.0

2.4 Dynamic Characteristics

Unless otherwise specified all values in the following table are valid for V_S = 7 to 18V and T_{AMB}= -40 to 125°C.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Propagation delay transmitter [1] [3] [7]	t_{trans_pd}	Bus loads: 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF			5	µs
Propagation delay transmitter symmetry [3] [7]	t_{trans_sym}	Calculate t_{trans_pdf} - t_{trans_pdr}	-2		2	µs
Propagation delay receiver [1] [5] [6] [7] [8]	t_{rec_pdf}	C_{RxD} = 25pF			6	µs
Propagation delay receiver symmetry [7] [8]	t_{rec_sym}	Calculate t_{trans_pdf} - t_{trans_pdr}	-2		2	µs
Slew rate rising and falling edge, high battery [4] [7]	$\|t_{SR\_HB}\|$	Bus load 1KΩ/1nF; 660Ω/6.8nF; 500Ω/10nF V_S = 18V	1	2	3	V/µs
Slew rate rising and falling edge, low battery [4] [7]	$\|t_{SR\_LB}\|$	Bus load 1KΩ/1nF; 660Ω/6.8nF; 500Ω/10nF V_S = 7V	0.5	2	3	V/µs
Slope Symmetry, high battery [4] [7]	t_{ssym_HB}	Bus load 1KΩ/1nF; 660Ω/6.8nF; 500Ω/10nF V_S = 18V Calculate $t_{sdom} - t_{srec}$	-5		+5	µs
Bus duty cycle 1 [8] [9]	D1	Calculate $t_{Bus\_rec(min)}$ / 100µs	0.396			
Bus duty cycle 2 [8] [9]	D2	Calculate $t_{Bus\_rec(max)}$ / 100µs			0.581	
Receiver debounce time [2] [5] [6]	t_{rec_deb}	BUS rising and falling edge	1.5		4	µs

[1] Propagation delays are not relevant for LIN protocol transmission, value only information parameter
[2] No production test, guaranteed by design and qualification
[3] See Figure 2 – Transmit delay
[4] See Figure 7 - Slope time and slew rate calculation in accordance to LIN 1.3
[5] This parameter is tested by applying a square wave signal to the bus. The minimum slew rate for the bus rising and falling edges is 50V/us
[6] See Figure 3 – Receiver debouncing and propagation delay
[7] In accordance to LIN physical layer specification 1.3
[8] In accordance to LIN physical layer specification 2.0
[9] See Figure 8 - Duty cycle calculation in accordance to LIN 2.0

2.5 Timing Diagrams

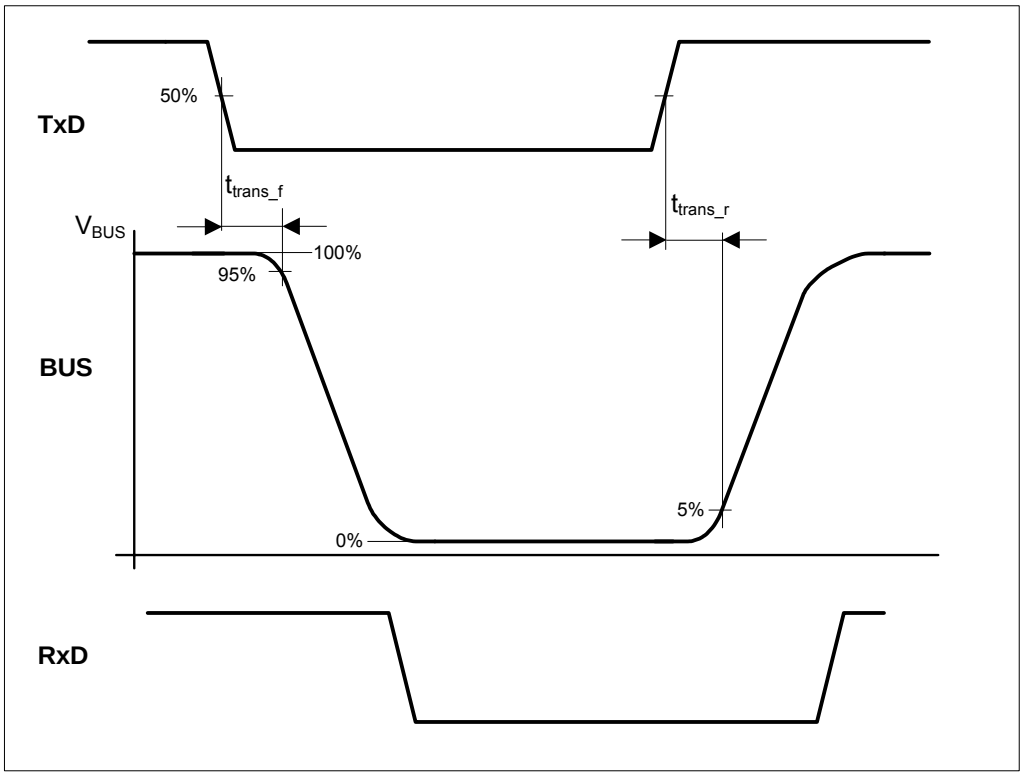


Figure 2 – Transmit delay

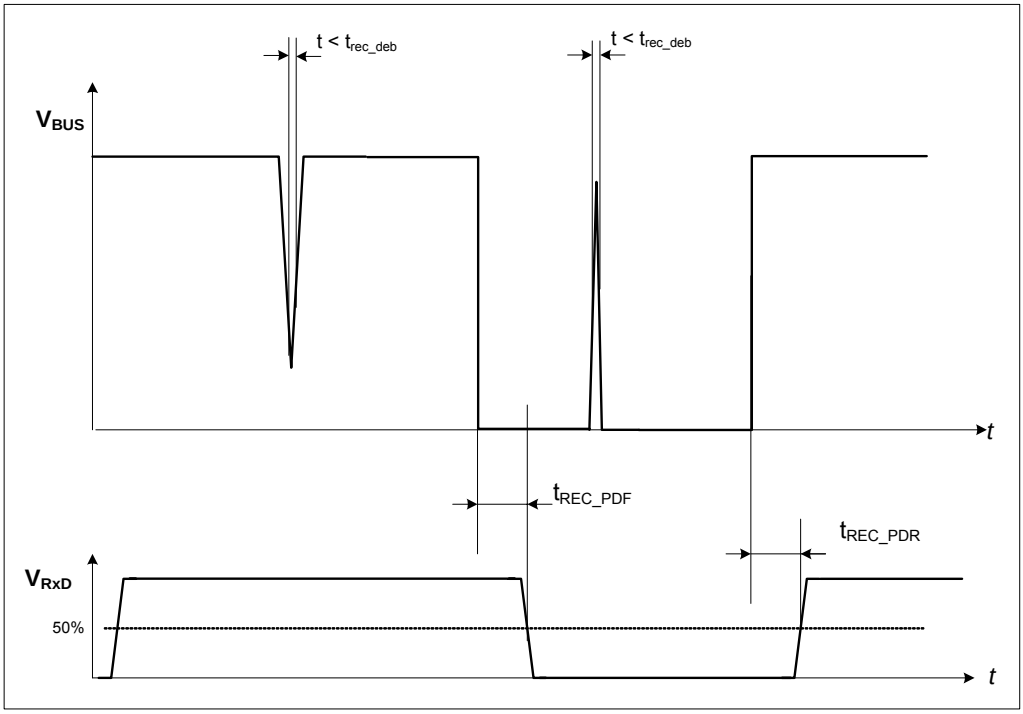


Figure 3 – Receiver debouncing and propagation delay

2.6 Test Circuits for Dynamic and Static Characteristics

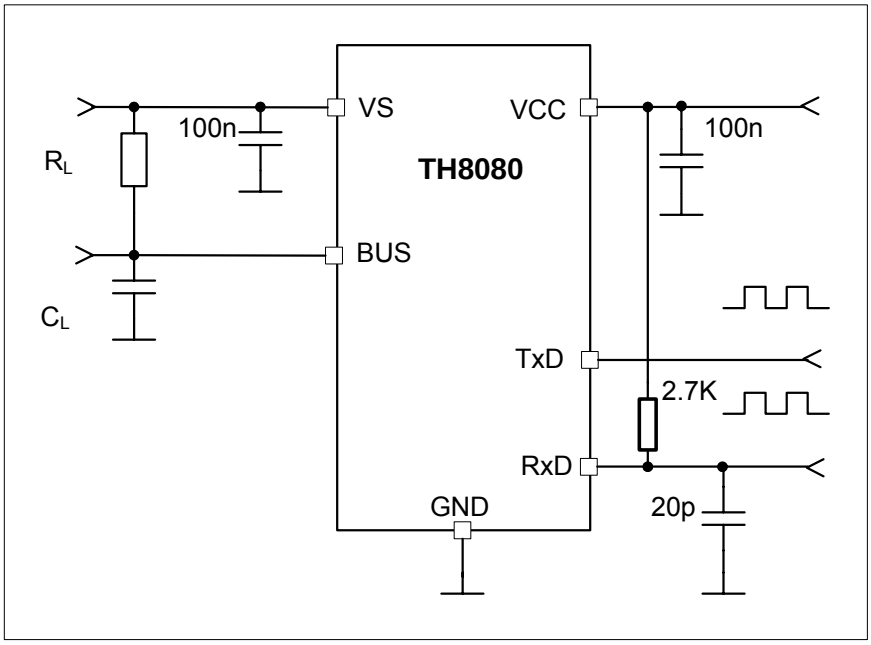


Figure 4 - Test circuit for dynamic characteristics

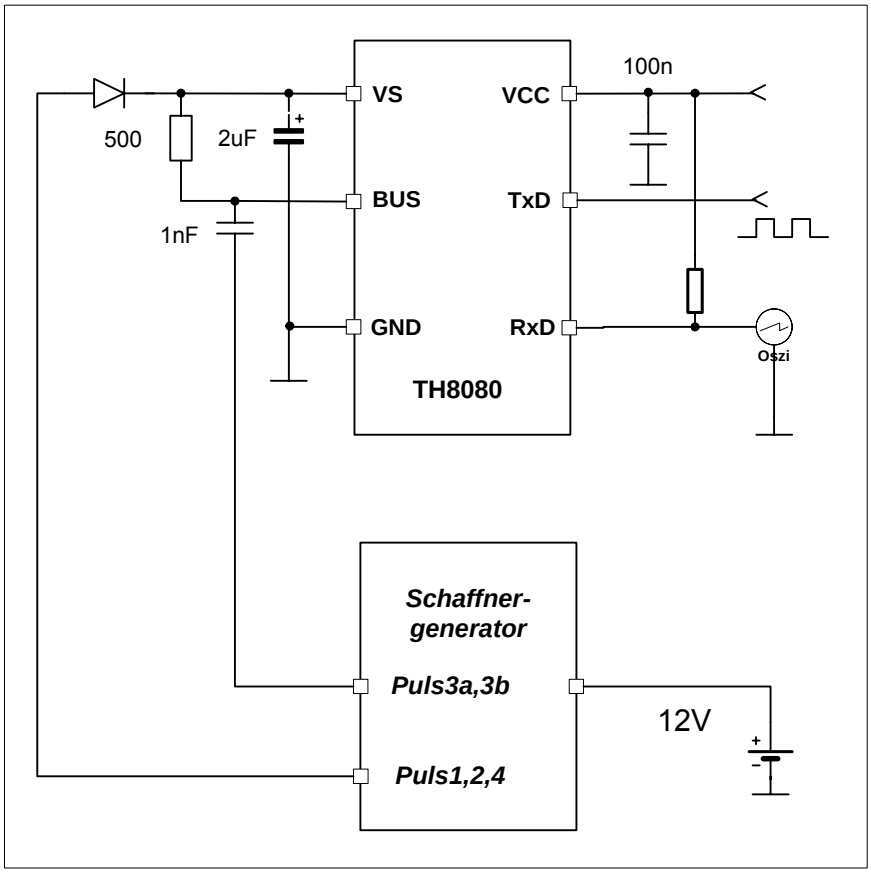


Figure 5 - Test circuit for automotive transients

3. Functional Description

3.1 Initialization

After *power on,* the chip enters automatically the recessive state. If the voltage regulator provides the V_{CC} – supply voltage, normal communication is possible.

3.2 Operating Modes

All operation modes will be handled from the TH8080 automatically.

Normal Mode

After power on, the IC switches automatically to normal mode. Bus communication is possible.
If there is no communication on the bus line the power consumption of the IC is very low and therefore it is no standby management from the MCU necessary.

Thermal Shutdown Mode

If the junction temperature T_J is higher than 155°C, the TH8080 will be switched into the thermal shutdown mode (bus driver will be switched off).
If T_J falls below the thermal shutdown temperature (typ. 140°C) the TH8080 will be switched to the normal mode.

3.3 LIN BUS Transceiver

The transceiver consists a bus-driver with slew rate control, current limitation and as well in the receiver a high voltage comparator followed by a debouncing unit.

BUS Input/Output

The recessive BUS level is generated from the integrated 30k pull up resistor in serial with a diode This diode prevent the reverse current of V_{BUS} during differential voltage between VS and BUS (V_{BUS}>V_S).
No additional termination resistor is necessary to use the TH8080 in LIN slave nodes. If this IC is used for LIN master nodes it is necessary that the BUS pin is terminated via a external 1kΩ resistor in serial with a diode to VBAT.

TxD Input

During transmission the data at the pin TxD will be transferred to the BUS driver for generating a BUS signal. To minimize the electromagnetic emission of the bus line, the BUS driver is equipped with an integrated slew rate control and wave shaping unit.
Transmitting will be interrupted if thermal shutdown is active.

The CMOS compatible input TxD controls directly the BUS level:

TxD = low	->	BUS = low (dominant level)
TxD = high	->	BUS = high (recessive level)

The TxD pin has an internal pull up resistor connected to VCC. This secures that an open TxD pin generates a recessive BUS level.

RxD Output

The data signals from the BUS pin will be transferred continuously to the pin RxD. Short spikes on the bus signal are suppressed by the implemented debouncing circuit.

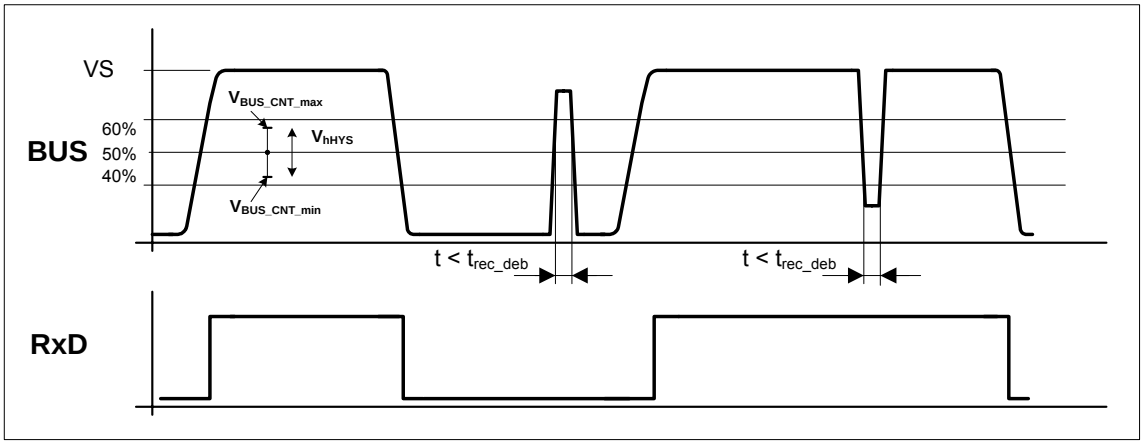


Figure 6 - Receive impulse diagram

The receive threshold values $V_{BUS\_CNT\_max}$ and $V_{BUS\_CNT\_min}$ are symmetrical to the centre voltage of $0.5*V_S$ with a hysteresis of typ. $0.175*V_S$. Including all tolerances the LIN specific receive threshold values of $0.4*V_S$ and $0.6*V_S$ will be secure observed.

The received BUS signal will be output to the RxD pin:

BUS < $V_{BUS\_CNT} - 0.5 * V_{HYS}$	->	RxD = low (BUS dominant)
BUS > $V_{BUS\_CNT} + 0.5 * V_{HYS}$	->	RxD = high, floating (BUS recessive)

This pin is a buffered open drain output with a typical load of:

Resistance: 2.7 kOhm
Capacitance: < 25 pF

Datarate

The TH8080 is a ***constant slew rate*** transceiver that means the bus driver operates with a fixed slew rate range of 0.5 V/µs ≤ ΔV/ΔT ≤ 3V/µs. This principle secures a very good symmetry of the slope times between recessive to dominant and dominant to recessive slopes within the LIN bus load range (C_{BUS}, R_{term}).
The TH8080 guarantees data rates up to 20kbit within the complete bus load range under worst case conditions. The constant slew rate principle is very robust against voltage drops and can operate with RC-oscillator systems with a clock tolerance up to ±2% between 2 nodes.

4. Operating under Disturbance

4.1 Loss of battery

If the ECU is disconnected from the battery, the bus pin is in high impedance state. There is no impact to the bus traffic and to the ECU itself.

4.2 Loss of Ground

In case of an interrupted ECU ground connection there is no influence to the bus line.

4.3 Short circuit to battery

The transmitter output current is limited to the specified value in case of short circuit to battery in order to protect the TH8080 itself against high current densities .

4.4 Short circuit to ground

If the bus line is shorted to negative shifted ground levels, there is no current flow from the ECU ground to the bus and no distortion of the bus traffic occurs.

4.5 Thermal overload

The TH8080 is protected against thermal overloads. If the chip temperature exceeds the specified value, the transmitter is switched off until thermal recovery. The receiver is still working while thermal shutdown.

4.6 Undervoltage Vcc

If the ECU regulated supply voltage is missing or decreases under the specified value, the transmitter is switched off to prevent undefined bus traffic.

5. Application Hints

5.1 Bus loading requirements

Parameter	Symbol	Min	Typ	Max	Unit
Operating voltage range	V_{BAT}	8		18	V
Voltage drop of reverse protection diode	V_{Drop_rev}	0.4	0.7	1	V
Voltage drop at the serial diode in pull up path	$V_{SerDiode}$	0.4	0.7	1	V
Battery shift voltage	V_{Shift_BAT}	0		0.1	V_{BAT}
Ground shift voltage	V_{Shift_GND}	0		0.1	V_{BAT}
Master termination resistor	R_{master}	900	1000	1100	Ω
Slave termination resistor	R_{slave}	20	30	60	kΩ
Number of system nodes	N	2		16	
Total length of bus line	LEN_{BUS}			40	m
Line capacitance	C_{LINE}		100	150	pF/m
Capacitance of master node	C_{Master}		220		pF
Capacitance of slave node	C_{Slave}	195	220	300	pF
Total capacitance of the bus including slave and master capacitance	C_{BUS}	0.47	4	10	nF
Network Total Resistance	$R_{Network}$	500		862	Ω
Time constant of overall system	τ	1		5	µs

Table 1 - Bus loading requirements

5.2 Slope time calculation

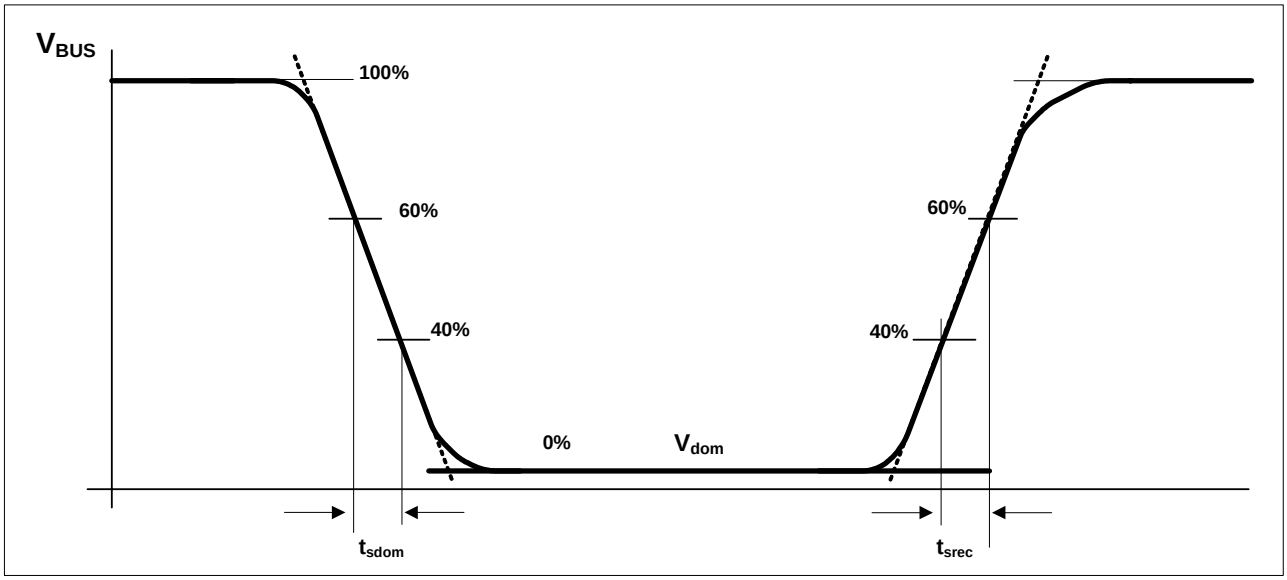


Figure 7 - Slope time and slew rate calculation in accordance to LIN 1.3

The slew rate of the bus voltage is measured between 40% and 60% of the output voltage swing (linear region). The output voltage swing is the difference between dominant and recessive bus voltage.

$$dV/dt = 0.2*V_{swing} / (t_{40\%} - t_{60\%})$$

The slope time is the extension of the slew rate tangent until the upper and lower voltage swing limits:

$$t_{slope} = 5 * (t_{40\%} - t_{60\%})$$

The slope time of the recessive to dominant edge is directly determined by the slew rate control of the transmitter:

$$t_{slope} = V_{swing} / dV/dt$$

The dominant to recessive edge is influenced from the network time constant and the slew rate control, because it's a passive edge. In case of low battery voltages and high bus loads the rising edge is only determined by the network. If the rising edge slew rate exceeds the value of the dominant one, the slew rate control determines the rising edge.

5.3 Duty Cycle Calculation

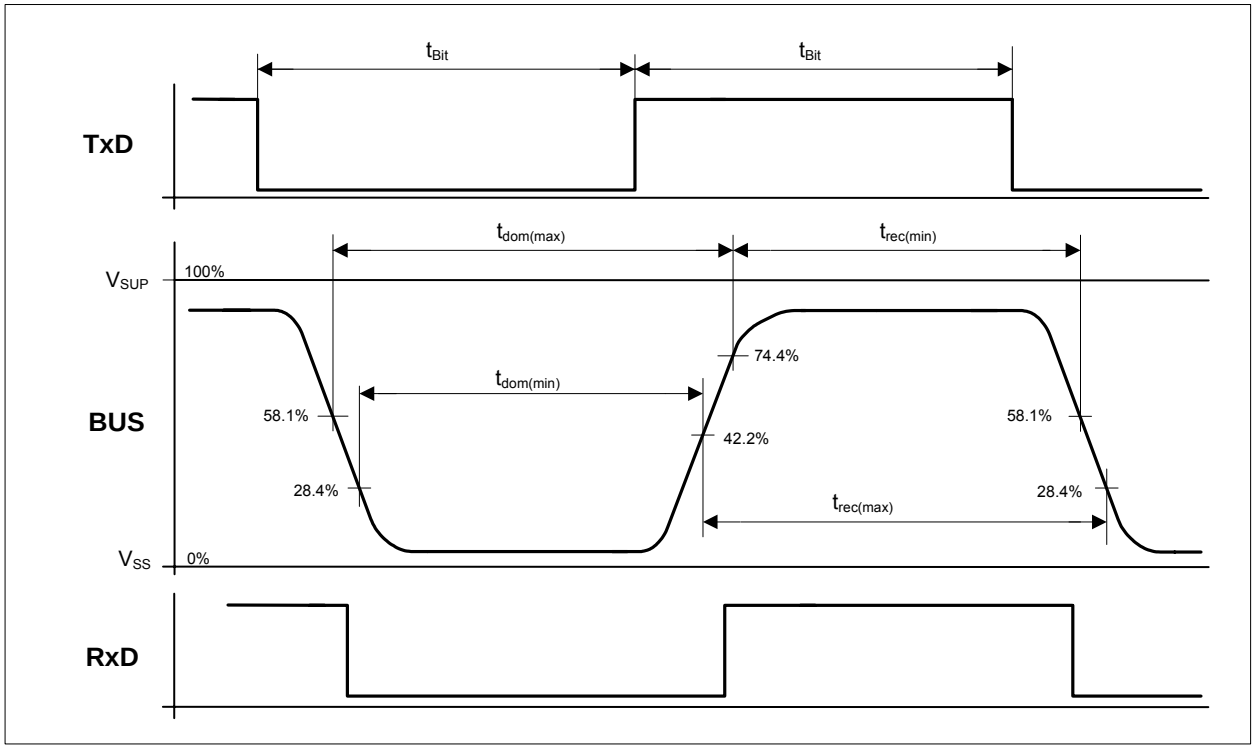


Figure 8 - Duty cycle calculation in accordance to LIN 2.0

With the timing parameters shown in Figure 8 two duty cycles , based on $t_{rec(min)}$ and $t_{rec(max)}$ can be calculated as follows :

$$D1 = t_{rec(min)} / (2 * t_{Bit})$$
$$D2 = t_{rec(max)} / (2 * t_{Bit})$$

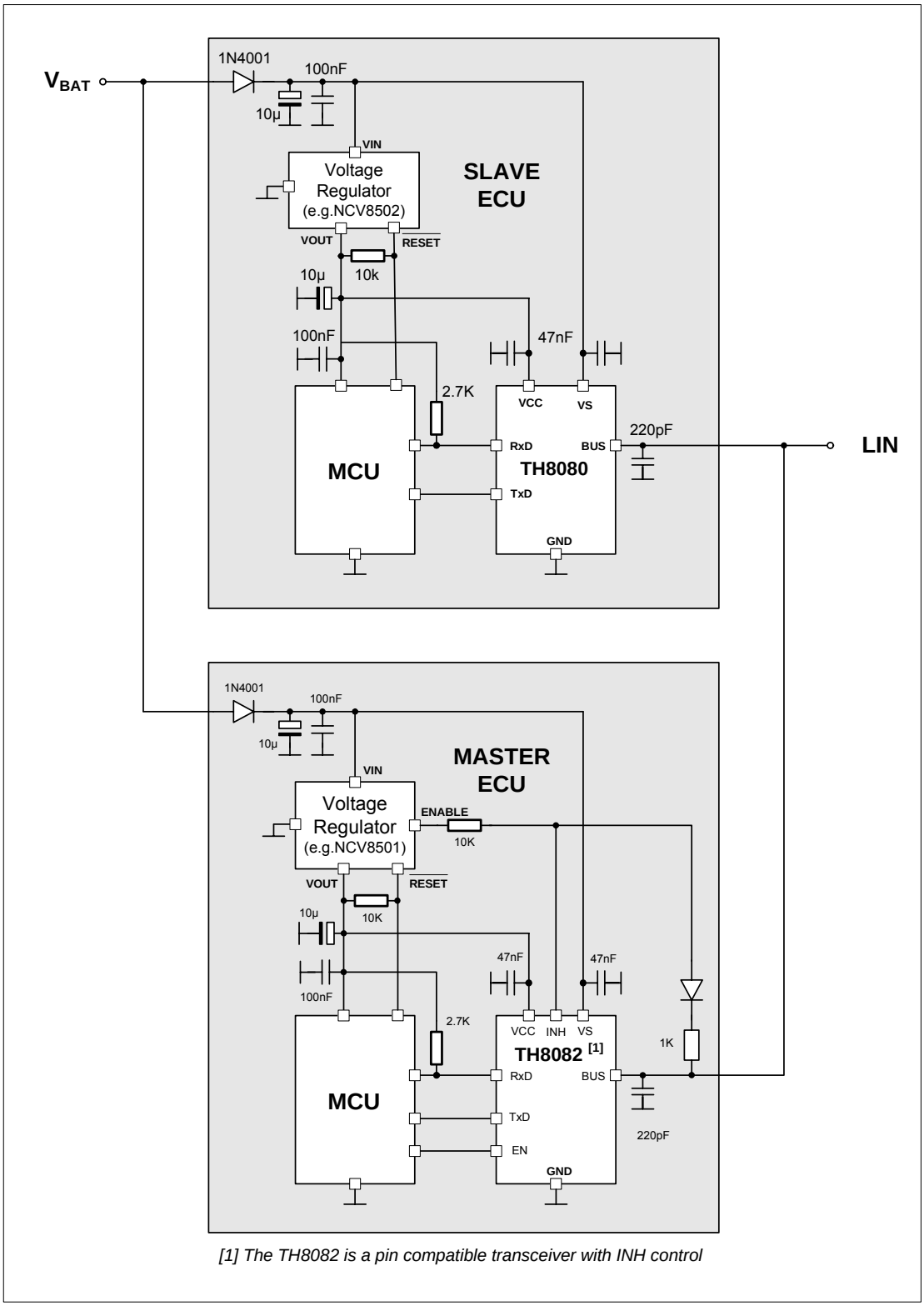
For proper operation at 20KBit/s (t_{Bit} = 50µs) the LIN driver has to fulfil the duty cycles specified in chapter 2.4 Dynamic Characteristics for supply voltages of 7 to 18V and the defined standard loads .

Due to this simplified definition there is no need to measure slew rates, slope times, transmitter delays and dominant voltage levels as specified in the LIN physical layer specification 1.3.

The device within the D1/D2 duty cycle range operates also in applications with reduced bus speed of 10.4KBit/s or below.

In order to minimize EME, the slew rates of the transmitter can be reduced (approximately by 2 times). Such devices have to fulfil the duty cycle definition D3/D4 in the LIN physical layer specification 2.0. Devices within this duty cycle range cannot operate in 20KBit/s applications.

5.4 Application Circuitry



[1] The TH8082 is a pin compatible transceiver with INH control

Figure 9 - Application Circuitry

6. Pin Description

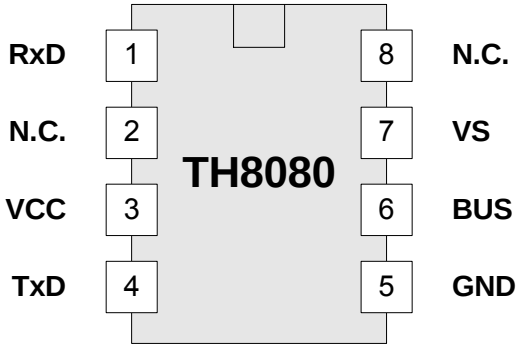
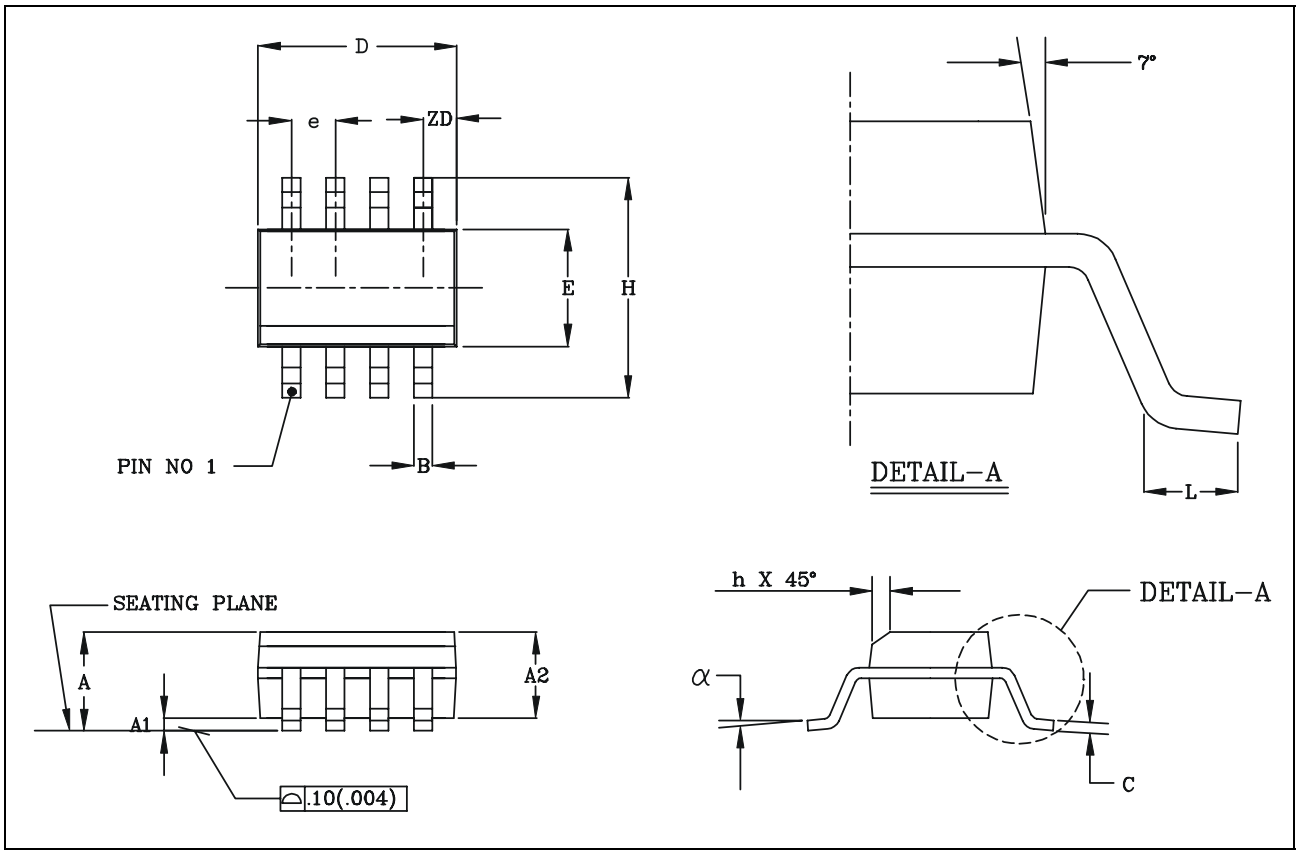


Figure 10 - Pin description SOIC8 package

Pin	Name	IO-Typ	Description
1	RXD	O	Receive data from BUS to core, LOW in dominant state
2	N.C.		
3	VCC	P	5V supply input
4	TXD	I	Transmit data from core to BUS, LOW in dominant state
5	GND	G	Ground
6	BUS	I/O	LIN bus pin, LOW in dominant state
7	VS	P	Battery input voltage
8	N.C.		

7. Mechanical Specification SOIC8

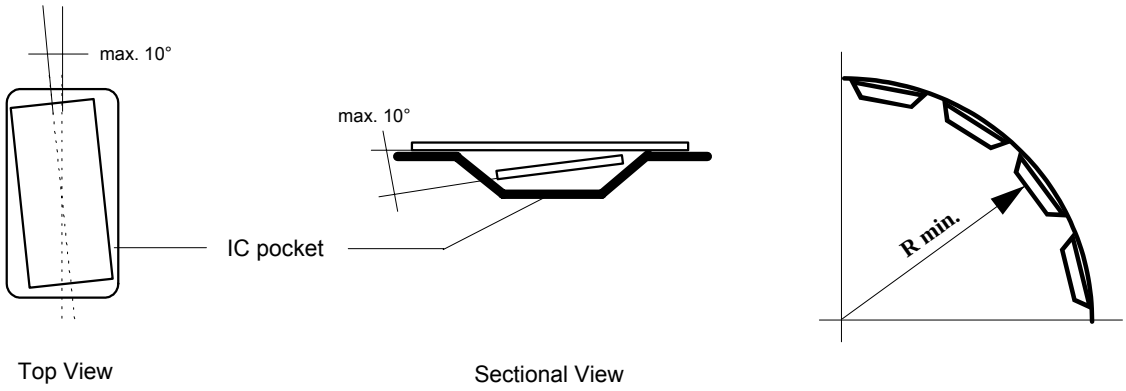


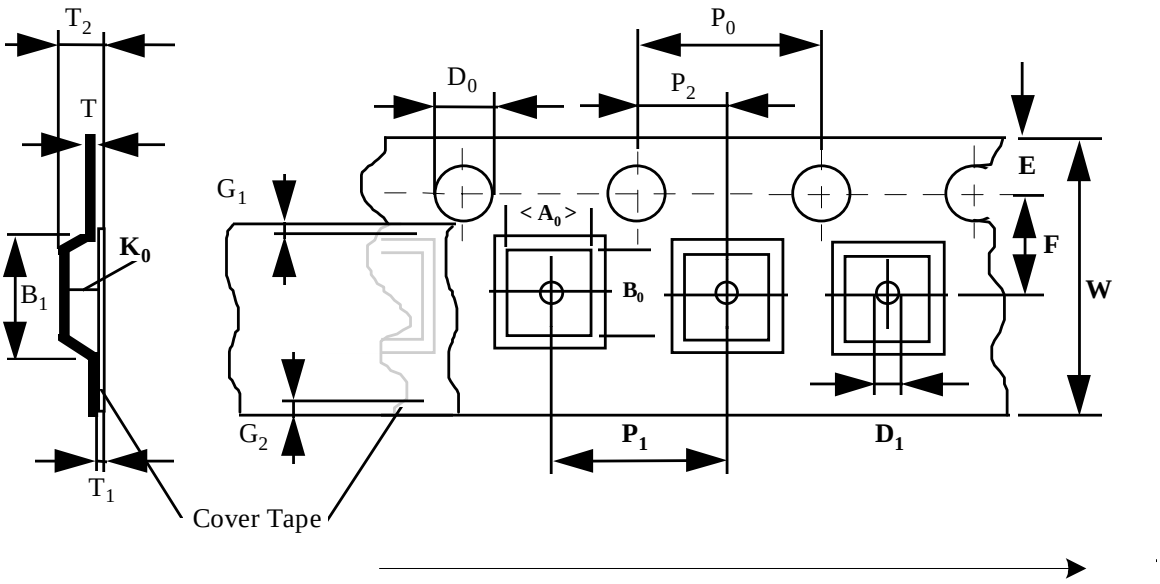
Small Outline Integrated Circiut (SOIC), SOIC 8, 150 mil

	A1	B	C	D	E	e	H	h	L	A	α	ZD	A2
All Dimension in mm, coplanarity < 0.1 mm													
min max	0.10 0.25	0.36 0.46	0.19 0.25	4.80 4.98	3.81 3.99	1.27	5.80 6.20	0.25 0.50	0.41 1.27	1.52 1.72	0° 8°	0.53	1.37 1.57
All Dimension in inch, coplanarity < 0.004”													
min max	0.004 0.0098	0.014 0.018	0.0075 0.0098	0.189 0.196	0.150 0.157	0.050	0.2284 0.244	0.0099 0.0198	0.016 0.050	0.060 0.068	0° 8°	0.021	0.054 0.062

8. Tape and Reel Specification

8.1 Tape Specification





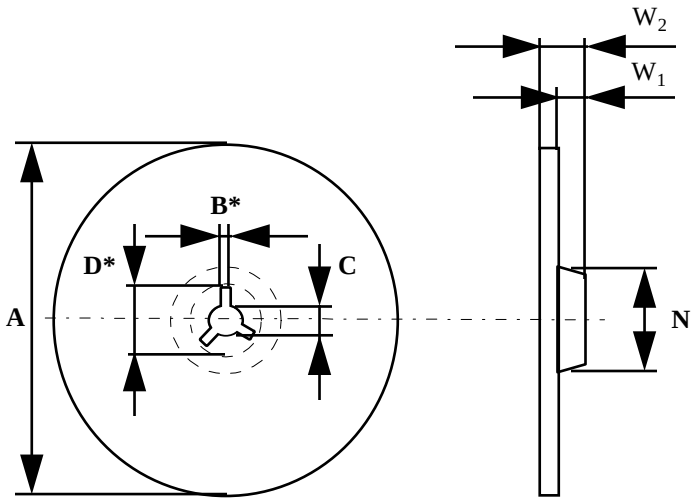
Standard Reel with diameter of 13“

Package	Parts per Reel	Width	Pitch
SOIC8	2500	12 mm	8 mm

D_0	E	P_0	P_2	T_{max}	$T_{1\,max}$	$G_{1\,min}$	$G_{2\,min}$	$B_{1\,max}$	$D_{1\,min}$	F	P_1	R_{min}	$T_{2\,max}$	W
1.5 +0.1	1.75 ±0.1	4.0 ±0.1	2.0 ±0.05	0.6	0.1	0.75	0.75	8.2	1.5	5.5 ±0.05	4.0 ±0.1	30	6.5	12.0 ±0.3

A_0, B_0, K_0 can be calculated with package specification.
Cover Tape width 9.2 mm.

8.2 Reel Specification



A_{max}	B*	C	D^*_{min}
330	2.0 ±0.5	13.0 +0,5/-0,2	20.2

Width of half reel	N_{min}	W_1	$W_{2\ max}$
4 mm	100,0	4,4	7,1
8 mm	100,0	8,4	11,1

9. ESD/EMC Remarks

9.1 General Remarks

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

9.2 ESD-Test

The TH8080 is tested according MIL883D (human body model).

9.3 EMC

The test on EMC impacts is done according to ISO 7637-1 for power supply pins and ISO 7637-3 for data- and signal pins.

Power Supply pin VS:

Testpulse	Condition	Duration
1	t_1 = 5 s / U_S = -100 V / t_D = 2 ms	5000 pulses
2	t_1 = 0.5 s / U_S = 100 V / t_D = 0.05 ms	5000 pulses
3a/b	U_S = -150 V/ U_S = 100 V burst 100ns / 10 ms / 90 ms break	1h
5	R_i = 0.5 Ω, t_D = 400 ms t_r = 0.1 ms / U_P+U_S = 40 V	10 pulses every 1min

Signal pin BUS:

Testpulse	Condition	Duration
1	t_1 = 5 s / U_S = -100 V / t_D = 2 ms	1000 pulses
2	t_1 = 0.5 s / U_S = 100 V / t_D = 0.05 ms	1000 pulses
3a/b	U_S = -150 V/ U_S = 100 V burst 100ns / 10 ms / 90 ms break	1000 burst

10. Assembly Information

This Melexis device is classified and qualified regarding soldering technology, solderability and moisture sensitivity level, as defined in this specification, according to following test methods:

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)
- CECC00802
  Standard Method For The Specification of Surface Mounting Components (SMDs) of Assessed Quality
- EIA/JEDEC JESD22-B106
  Resistance to soldering temperature for through-hole mounted devices
- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices
- MIL 883 Method 2003 / EIA/JEDEC JESD22-B102
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Based on Melexis commitment to environmental responsibility, European legislation (Directive on the Restriction of the Use of Certain Hazardous substances, RoHS) and customer requests, Melexis has installed a roadmap to qualify their package families for lead free processes also.
Various lead free generic qualifications are running, current results on request.

For more information on Melexis lead free statement see quality page at our website: http://www.melexis.com/html/pdf/MLXleadfree-statement.pdf

11. Disclaimer

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