

## ESDA6V1Q6-18RL

## Application Specific Discretes A.S.D.™

# ESD PROTECTION MONOLITHIC 9-BIT WIDE TRANSIL™ ARRAY

## **MAIN APPLICATIONS**

Where protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems

## **DESCRIPTION**

The ESDA6V1Q6-18RL is a monolithic TRANSIL array designed to provide a 9-bit wide undershoot and overshoot clamping function in association with ESD protection level of up to 25 kV.

The ESDA6V1Q6-18RL provides best efficiency when using separated inputs and outputs, in the so called 4-point structure.

## **FEATURES**

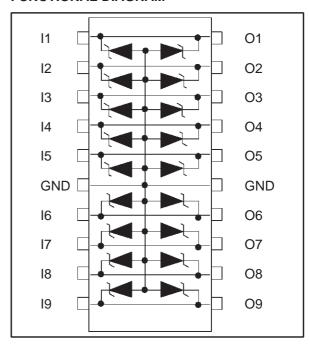
- 9-bit wide undershoot and overshoot clamping functions.
- Breakdown voltage: V<sub>BR</sub> = 6.1V min.
- Forward voltage V<sub>F</sub> = 1.25V max. @ I<sub>F</sub> = 200mA
- Low capacitance : C = 130pF @ V<sub>RM</sub> = 5.25V.
- Low clamping voltage.
- 200W peak pulse power (8/20µs).

## **BENEFITS**

- ESD protection of 25 kV, according to MIL STD- Method 3015-7.
- High integration.
- Four points structure, efficient for minimizingl ESD effects at the outputs.



## **FUNCTIONAL DIAGRAM**



## **COMPLIES WITH THE FOLLOWING STANDARDS:**

ESD Standard	IEC61000-4-2: level 4	15kV (air discharge) 8kV (contact discharge)	
MIL STD 883E-Method 3015-7 (Human body model)	Class 3	25kV F = 1Hz C = 100pF R = 1500Ω	3 positive / 3 negative strikes

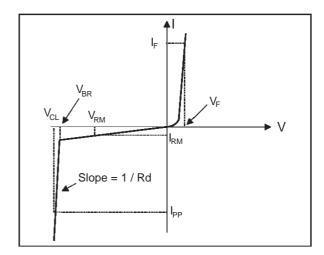
ASD and TRANSIL are trademarks of STMicroelectronics

August 2002 - Ed: 4A 1/6

## ABSOLUTE MAXIMUM RATINGS $(T_{amb} = 25^{\circ}C)$

Symbol	Parameter	Value	Unit
V <sub>PP</sub>	Maximum electrostatic discharge in following measurement conditions:  MIL STD 883E - METHOD 3015-7 IEC1000-4-2 - air discharge IEC1000-4-2 - contact discharge	25 15 8	kV
P <sub>PP</sub>	Peak pulse power (8/20μs)	200	W
T <sub>stg</sub> T <sub>j</sub>	Storage temperature Maximum junction temperature	- 55 to + 150 125	°C

Symbol	Parameter		
$V_{RM}$	Stand-off voltage		
$V_{BR}$	Breakdown voltage		
V <sub>CL</sub>	Clamping voltage		
V <sub>F</sub>	Forward voltage drop		
С	Capacitance		
Rd	Dynamic impedance		
I <sub>RM</sub>	Leakage current		
IPP	Peak pulse current		



Symbol	Test conditions	Min.	Тур.	Max.	Unit
I <sub>RM</sub>	$V_{RM}$ = 5.25 V, between any I/O pin and GND			20	μΑ
$V_{BR}$	I <sub>R</sub> = 1 mA, between any I/O pin and GND	6.1		7.2	V
V <sub>F</sub>	IF = 200 mA, between any I/O pin and GND			1.25	V
Rd	$I_{PP} = 15 \text{ A}, t_p = 2.5 \mu s \text{ (note 1)}$		0.2		Ω
С	Between any I/O pin and GND at 0 V bias Between any I/O pin and GND at $V_{RM} = 5.25 \text{ V}$		260 130		pF

Note 1 : see the calculation of the clamping voltage.

2/6

### **CALCULATION OF THE CLAMPING VOLTAGE**

## **USE OF THE DYNAMIC RESISTANCE**

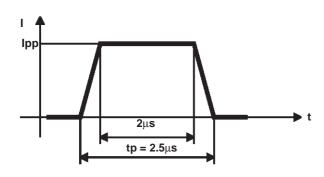
The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage  $V_{\text{CL}}$ . This is why we give the dynamic resistance in addition to the classical parameters. The voltage across the protection cell can be calculated with the following formula:

$$V_{CL} = V_{BR} + Rd I_{PP}$$

Where Ipp is the peak current through the ESDA cell.

#### DYNAMIC RESISTANCE MEASUREMENT

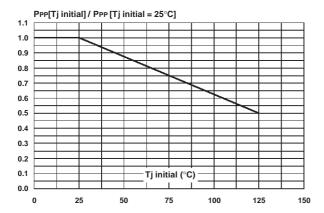
The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical  $8/20\mu s$  and  $10/1000\mu s$  surges.



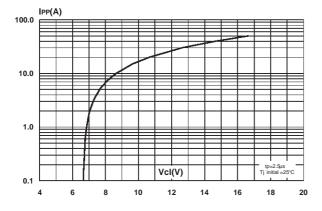
2.5µs duration measurement wave.

As the value of the dynamic resistance remains stable for a surge duration lower than  $20\mu s$ , the  $2.5\mu s$  rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of Rd.

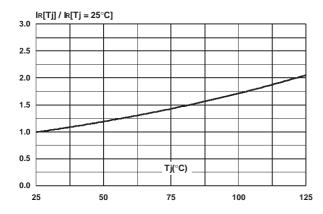
**Fig. 1:** Relative variation of peak pulse power versus initial junction temperature.



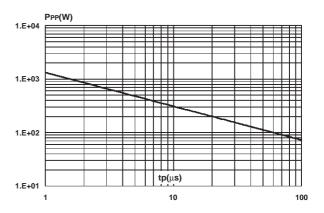
**Fig. 3:** Clamping voltage versus peak pulse current (maximum values, rectangular waveform).



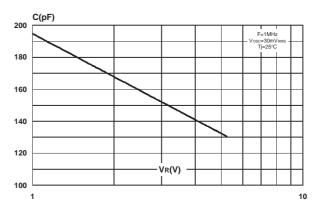
**Fig. 5:** Relative variation of leakage current versus junction temperature (typical values).



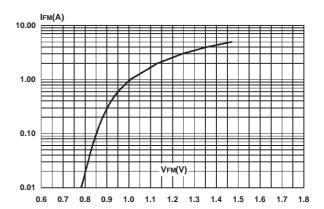
**Fig. 2:** Peak pulse power versus exponential pulse duration.



**Fig. 4:** Junction capacitance versus reverse applied voltage (typical values).



**Fig. 6:** Peak forward voltage drop versus peak forward current (typical values).



5

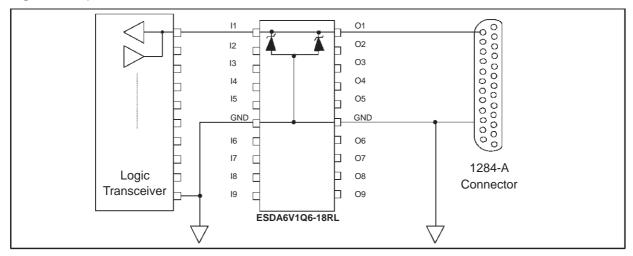
## ESD protection by the ESDA6VQ6-18RL

Electrostatic discharge (ESD) is a major cause of failure in electronic systems.

Transient Voltage Suppressors (TVS) are an ideal choice for ESD protection. They are capable of clamping the incoming transient to a low enough level such that damage to the protected semiconductor is prevented. Surface mount TVS arrays offer the best choice for minimal lead inductance.

They serve as parallel protection elements, connected between the signal line to ground. As the transient rises above the operating voltage of the device, the TVS array becomes a low impedance path diverting the

Fig. 7: Example of connection for one cell of the ESDA6V1Q6-18RL.



transient current to ground.

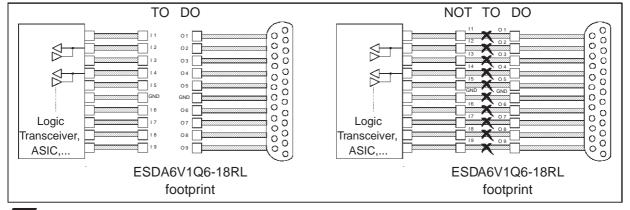
The ESDA6V1Q6-18RL array is the ideal board level protection of ESD sensitive semiconductor components. The first TRANSIL<sup>TM</sup> diode suppresses coarsely the ESD transient, while the second stage finally clamps the remaining overvoltage. It provides best efficiency when using separated inputs and outputs, in the so called 4-points structure.

## **Circuit Board Layout**

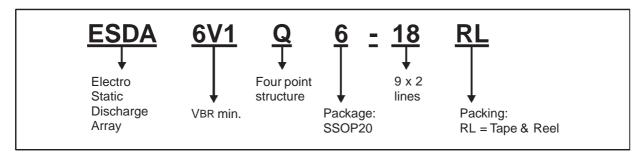
Circuit board layout is a critical design step in the suppression of ESD induced transients. The following guidelines are recommended:

- The ESDA6V1Q6-18RL should be placed as near as possible to the input terminals or connectors.
- The path length between the ESD suppressor and the protected line should be minimized.
- All conductive loops, including power and ground loops should be minimized.
- The ESD transient return path to ground should be kept as short as possible.

Fig. 8: Recommended PCB layout to benefit from 4 point structure.

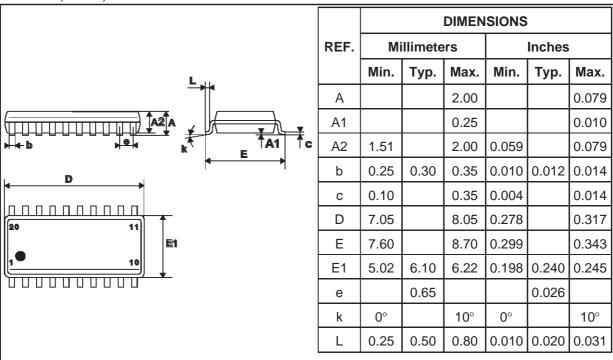


## PART NUMBERING AND ORDERING INFORMATION



## PACKAGE MECHANICAL DATA

SSOP20 (Plastic)



### **ORDERING CODE**

Order code	Marking	Package	Weight	Delivery mode	Base qty (pcs)
ESDA6V1Q6-18RL	ESDA6V1FU6	SSOP20	0.18g	Tape & reel	2000

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied.

STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All rights reserved.

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore Spain - Sweden - Switzerland - United Kingdom - United States.

http://www.st.com

6/6