

Description

- Compact footprint for high density, high current/low voltage applications
- Foil technology that adds higher reliability factor over the traditional magnet wire used for higher frequency circuit designs
- Frequency Range up to 1MHz

Applications

- Next generation microprocessors
- Energy storage applications
- DC-DC converters
- Computers

Environmental Data

- Storage temperature range: -40°C to +125°C
- Operating ambient temperature range: -40°C to +85°C (range is application specific).
- Solder reflow temperature: +260°C for 10 seconds maximum



Packaging

- 45 parts per tray bulk packaging.
- Tape and reel packaging also available, 44mm width, 110 parts per 13" reel.
- Add -TR after part number for tape and reel packaging.

Part Number	Rated Inductance μH	OCL (1) μH ± 20%	I _{rms} (2) Amperes (Typ.)	I _{sat} (3) Amperes (Typ.)	DCR (4) Ohms (Max.)	Volts (5) μSec
HC2-R47-R	.47	.52	52.9	63.75	.0006	6.87
HC2-R68-R	.68	.63	52.9	50.00	.0006	6.87
HC2-1R0-R	1.0	1.15	33.0	42.50	.0013	10.31
HC2-2R2-R	2.2	2.00	24.3	31.90	.0023	13.75
HC2-4R7-R	4.7	4.55	17.0	21.25	.0046	20.62
HC2-6R0-R	6.0	6.00	17.0	16.50	.0046	20.62

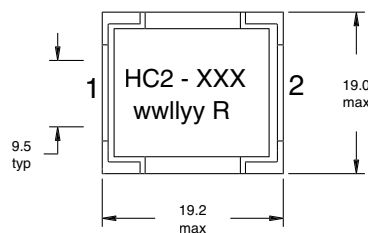
1) Open Circuit Inductance Test Parameters: 300kHz, 0.250 Vrms, 0.0 Adc.
 2) DC current for an approximate temperature change of 40°C without core loss.
 Derating is necessary for AC currents.
 PCB layout, trace thickness and width, air-flow and proximity of other heat generating components will affect the temperature rise.
 It is recommended that the temperature of the part not exceed 125°C under worst case operating conditions verified in the end application.

3) Peak current for approximately 30% roll-off
 4) Values @ 20°C

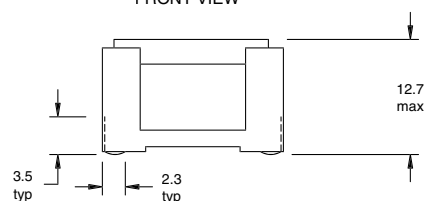
5) Applied Volt-Time product (V-μS) across the inductor. This value represents the applied V-μS at 300kHz necessary to generate a core loss equal to 10% of the total losses for 40°C temperature rise.

Mechanical Diagrams

TOP VIEW

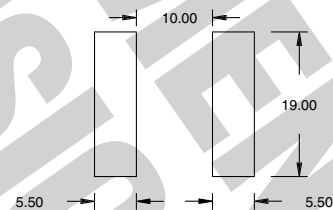


FRONT VIEW

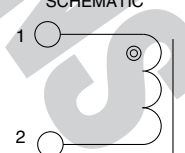


Dimensions in Millimeters

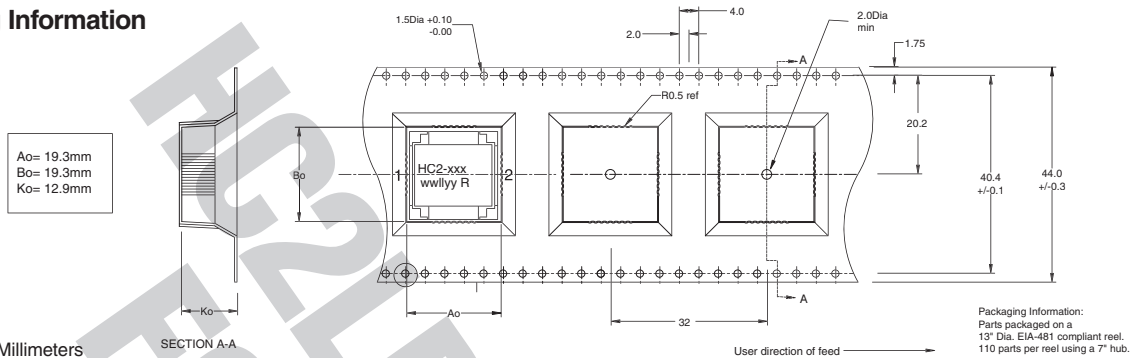
RECOMMENDED PCB PAD LAYOUT



SCHEMATIC

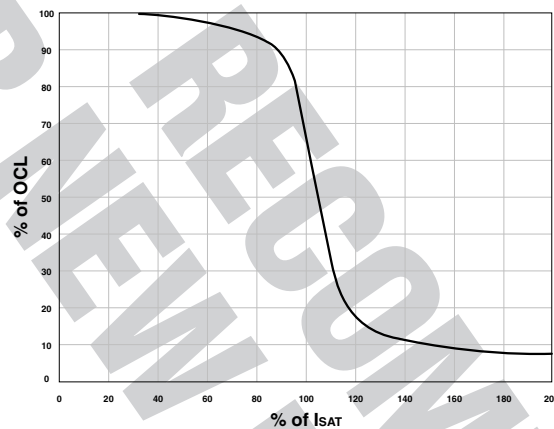


Packaging Information



Rolloff

INDUCTANCE VERSUS SATURATION CURRENT



Core Loss

IRMS DERATING WITH CORE LOSS

