



Low Noise, Matched Dual Monolithic Transistor

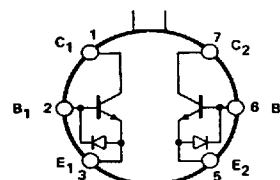
MAT02

FEATURES

Low Offset Voltage: 50 μV max
Low Noise Voltage at 100 Hz, 1 mA: 1.0 nV/ $\sqrt{\text{Hz}}$ max
High Gain (h_{FE}): 500 min at $I_C = 1$ mA
300 min at $I_C = 1$ μA
Excellent Log Conformance: $r_{BE} = 0.3 \Omega$
Low Offset Voltage Drift: 0.1 $\mu\text{V}/^\circ\text{C}$ max
Improved Direct Replacement for LM194/394
Available in Die Form

PIN CONNECTION

TO-78
(H Suffix)



NOTE

Substrate is connected to case on TO-78 package. Substrate is normally connected to the most negative circuit potential, but can be floated.

PRODUCT DESCRIPTION

The design of the MAT02 series of NPN dual monolithic transistors is optimized for very low noise, low drift, and low r_{BE} . Precision Monolithics' exclusive Silicon Nitride "Triple-Passivation" process stabilizes the critical device parameters over wide ranges of temperature and elapsed time. Also, the high current gain (h_{FE}) of the MAT02 is maintained over a wide range of collector current. Exceptional characteristics of the MAT02 include offset voltage of 50 μV max (A/E grades) and 150 μV max F grade. Device performance is specified over the full military temperature range as well as at 25°C.

Input protection diodes are provided across the emitter-base junctions to prevent degradation of the device characteristics due to reverse-biased emitter current. The substrate is clamped to the most negative emitter by the parasitic isolation junction created by the protection diodes. This results in complete isolation between the transistors.

The MAT02 should be used in any application where low noise is a priority. The MAT02 can be used as an input stage to make an amplifier with noise voltage of less than 1.0 nV/ $\sqrt{\text{Hz}}$ at 100 Hz. Other applications, such as log/antilog circuits, may use the excellent logging conformity of the MAT02. Typical bulk resistance is only 0.3 Ω to 0.4 Ω . The MAT02 electrical characteristics approach those of an ideal transistor when operated over a collector current range of 1 μA to 10 mA. For applications requiring multiple devices see MAT04 Quad Matched Transistor data sheet.

ABSOLUTE MAXIMUM RATINGS¹

Collector-Base Voltage (BV_{CBO})	40 V
Collector-Emitter Voltage (BV_{CEO})	40 V
Collector-Collector Voltage (BV_{CC})	40 V
Emitter-Emitter Voltage (BV_{EE})	40 V
Collector Current (I_C)	20 mA
Emitter Current (I_E)	20 mA
Total Power Dissipation	
Case Temperature $\leq 40^\circ\text{C}$ ²	1.8 W
Ambient Temperature $\leq 70^\circ\text{C}$ ³	500 mW
Operating Temperature Range	
MAT02A	-55°C to +125°C
MAT02E, F	-25°C to +85°C
Operating Junction Temperature	-55°C to +150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C
Junction Temperature	-65°C to +150°C

NOTES

¹Absolute maximum ratings apply to both DICE and packaged devices.

²Rating applies to applications using heat sinking to control case temperature. Derate linearly at 16.4 mW/ $^\circ\text{C}$ for case temperature above 40°C.

³Rating applies to applications not using a heat sinking; devices in free air only. Derate linearly at 6.3 mW/ $^\circ\text{C}$ for ambient temperature above 70°C.

ORDERING GUIDE¹

Model	V_{OS} max ($T_A = +25^\circ\text{C}$)	Temperature Range	Package Option
MAT02AH ²	50 μV	-55°C to +125°C	TO-78
MAT02EH	50 μV	-55°C to +125°C	TO-78
MAT02FH	150 μV	-55°C to +125°C	TO-78

NOTES

¹Burn-In is available on commercial and industrial temperature range parts in TO-can packages.

²For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

REV. C

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MAT02—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_{CB} = 15\text{ V}$, $I_C = 10\text{ }\mu\text{A}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT02A/E			MAT02F			Units
			Min	Typ	Max	Min	Typ	Max	
Current Gain	h_{FE}	$I_C = 1\text{ mA}^1$ $I_C = 100\text{ }\mu\text{A}$ $I_C = 10\text{ }\mu\text{A}$ $I_C = 1\text{ }\mu\text{A}$	500	605		400	605		
Current Gain Match	Δh_{FE}	$10\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}^2$		0.5	2		0.5	4	%
Offset Voltage	V_{OS}	$V_{CB} = 0$, $1\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}^3$		10	50		80	150	μV
Offset Voltage	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq V_{MAX}^4$		10	25		10	50	μV
Change vs. V_{CB}		$1\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}^3$		10	25		10	50	μV
Offset Voltage Change	$\Delta V_{OS}/\Delta I_C$	$V_{CB} = 0\text{ V}$		5	25		5	50	μV
vs. Collector Current		$1\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}^3$		5	25		5	50	μV
Offset Current									
Change vs. V_{CB}	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq V_{MAX}$		30	70		30	70	pA/V
Bulk Resistance	r_{BE}	$10\text{ }\mu\text{A} \leq I_C \leq 10\text{ mA}^5$		0.3	0.5		0.3	0.5	Ω
Collector-Base									
Leakage Current	I_{CBO}	$V_{CB} = V_{MAX}$		25	200		25	400	pA
Collector-Collector									
Leakage Current	I_{CC}	$V_{CC} = V_{MAX}^{5,6}$ $V_{CE} = V_{MAX}^{5,6}$		35	200		35	400	pA
Collector-Emitter									
Leakage Current	I_{CES}	$V_{BE} = 0$		35	200		35	400	pA
Noise Voltage Density	e_n	$I_C = 1\text{ mA}$, $V_{CB} = 0^7$ $f_O = 10\text{ Hz}$ $f_O = 100\text{ Hz}$ $f_O = 1\text{ kHz}$ $f_O = 10\text{ kHz}$		1.6	2		1.6	3	$\text{nV}/\sqrt{\text{Hz}}$
				0.9	1		0.9	2	$\text{nV}/\sqrt{\text{Hz}}$
				0.85	1		0.85	2	$\text{nV}/\sqrt{\text{Hz}}$
				0.85	1		0.85	2	$\text{nV}/\sqrt{\text{Hz}}$
Collector Saturation									
Voltage	$V_{CE(SAT)}$	$I_C = 1\text{ mA}$, $I_B = 100\text{ }\mu\text{A}$		0.05	0.1		0.05	0.2	V
Input Bias Current	I_B	$I_C = 10\text{ }\mu\text{A}$			25			34	nA
Input Offset Current	I_{OS}	$I_C = 10\text{ }\mu\text{A}$			0.6			1.3	nA
Breakdown Voltage	BV_{CEO}		40			40			V
Gain-Bandwidth Product	f_T	$I_C = 10\text{ mA}$, $V_{CE} = 10\text{ V}$		200			200		MHz
Output Capacitance	C_{OB}	$V_{CB} = 15\text{ V}$, $I_E = 0$		23			23		pF
Collector-Collector									
Capacitance	C_{CC}	$V_{CC} = 0$		35			35		pF

NOTES

¹Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector currents.

²Current gain match (Δh_{FE}) is defined as: $\Delta h_{FE} = \frac{100 (\Delta I_B) (h_{FE} \text{ min})}{I_C}$

³Measured at $I_C = 10\text{ }\mu\text{A}$ and guaranteed by design over the specified range of I_C .

⁴This is the maximum change in V_{OS} as V_{CB} is swept from 0 V to 40 V.

⁵Guaranteed by design.

⁶ I_{CC} and I_{CES} are verified by measurement of I_{CBO} .

⁷Sample tested.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS ($V_{CB} = 15\text{ V}$, $-25^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT02E			MAT02F			Units
			Min	Typ	Max	Min	Typ	Max	
Offset Voltage	V_{OS}	$V_{CB} = 0$ $1\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}^1$			70			220	μV
Average Offset Voltage Drift	TCV_{OS}	$10\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}$, $0 \leq V_{CB} \leq V_{MAX}^2$ V_{OS} Trimmed to Zero ³		0.08	0.3		0.08	1	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current	I_{OS}	$I_C = 10\text{ }\mu\text{A}$		0.03	0.1		0.03	0.3	nA
Input Offset Current Drift	TCI_{OS}	$I_C = 10\text{ }\mu\text{A}^4$			8			13	nA
Input Bias Current	I_B	$I_C = 10\text{ }\mu\text{A}$			45			50	nA
Current Gain	h_{FE}	$I_C = 1\text{ mA}^5$	325			300			
		$I_C = 100\text{ }\mu\text{A}$	275			250			
		$I_C = 10\text{ }\mu\text{A}$	225			200			
		$I_C = 1\text{ }\mu\text{A}$	200			150			
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = V_{MAX}$		2			3		nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = V_{MAX}$, $V_{BE} = 0$		3			4		nA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = V_{MAX}$		3			4		nA

ELECTRICAL CHARACTERISTICS ($V_{CB} = 15\text{ V}$, $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	MAT02A		Units
				Typ	Max	
Offset Voltage	V_{OS}	$V_{CB} = 0$ $1\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}^1$			80	μV
Average Offset Voltage Drift	TCV_{OS}	$10\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}$, $0 \leq V_{CB} \leq V_{MAX}^2$ V_{OS} Trimmed to Zero ³		0.08	0.3	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current	I_{OS}	$I_C = 10\text{ }\mu\text{A}$		0.03	0.1	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current Drift	TCI_{OS}	$I_C = 10\text{ }\mu\text{A}^4$			9	nA
Input Bias Current	I_B	$I_C = 10\text{ }\mu\text{A}$			60	nA
Current Gain	h_{FE}	$I_C = 1\text{ mA}^5$	275			
		$I_C = 100\text{ }\mu\text{A}$	225			
		$I_C = 10\text{ }\mu\text{A}$	125			
		$I_C = 1\text{ }\mu\text{A}$	150			
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = V_{MAX}$ $T_A = 125^{\circ}\text{C}$		15		nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = V_{MAX}$, $V_{BE} = 0$ $T_A = 125^{\circ}\text{C}$		50		nA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = V_{MAX}$ $T_A = 125^{\circ}\text{C}$		30		nA

NOTES

¹Measured at $I_C = 10\text{ }\mu\text{A}$ and guaranteed by design over the specified range of I_C .

²Guaranteed by V_{OS} test ($TCV_{OS} \equiv \frac{V_{OS}}{T}$ for $V_{OS} \ll V_{BE}$) $T = 298^{\circ}\text{K}$ for $T_A = 25^{\circ}\text{C}$.

³The initial zero offset voltage is established by adjusting the ratio of IC1 to IC2 at $T_A = 25^{\circ}\text{C}$. This ratio must be held to 0.003% over the entire temperature range. Measurements are taken at the temperature extremes and 25°C .

⁴Guaranteed by design.

⁵Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector current.

Specifications subject to change without notice.

MAT02

WAFER TEST LIMITS (@ 25°C for $V_{CB} = 15\text{ V}$ and $I_C = 10\text{ }\mu\text{A}$, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT02N Limits	Units
Breakdown Voltage	BV_{CEO}		40	V min
Offset Voltage	V_{OS}	$10\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}^1$	150	$\mu\text{V max}$
Input Offset Current	I_{OS}		1.2	nA max
Input Bias Current	I_B	$V_{CB} = 0\text{ V}$	34	nA max
Current Gain	h_{FE}	$I_C = 1\text{ mA}, V_{CB} = 0\text{ V}$	400	min
		$I_C = 10\text{ }\mu\text{A}, V_{CB} = 0\text{ V}$	300	
Current Gain Match	Δh_{FE}	$10\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}, V_{CB} = 0\text{ V}$	4	% max
Offset Voltage Change vs. V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	$0\text{ V} \leq V_{CB} \leq 40\text{ V}$	50	$\mu\text{V max}$
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	$10\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}^1$	50	$\mu\text{V max}$
Bulk Resistance	r_{BE}	$V_{CB} = 0$		
Collector Saturation Voltage	$V_{CE(SAT)}$	$10\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}^1$	0.5	$\Omega\text{ max}$
		$I_C = 1\text{ mA}$	0.2	V max
		$I_B = 100\text{ }\mu\text{A}$		

NOTES

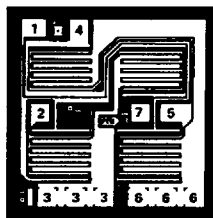
¹Measured at $I_C = 10\text{ }\mu\text{A}$ and guaranteed by design over the specified range of I_C .

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS ($V_{CB} = 15\text{ V}$, $I_C = 10\text{ }\mu\text{A}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT02N Limits	Units
Average Offset Voltage Drift	TCV_{OS}	$10\text{ }\mu\text{A} \leq I_C \leq 1\text{ mA}$	0.08	$\mu\text{V}/^\circ\text{C}$
Average Offset Current Drift	TCI_{OS}	$0 \leq V_{CB} \leq V_{MAX}$ $I_C = 10\text{ }\mu\text{A}$	40	$\text{pA}/^\circ\text{C}$
Gain-Bandwidth Product	f_T	$V_{CE} = 10\text{ V}, I_C = 10\text{ mA}$	200	MHz
Offset Current Change vs. V_{CB}	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 40\text{ V}$	70	pA/V

DICE CHARACTERISTICS



1. COLLECTOR (1)
2. BASE (1)
3. EMITTER (1)
4. COLLECTOR (2)
5. BASE (2)
6. EMITTER (2)
7. SUBSTRATE

Die Size $0.061 \times 0.057\text{ inch}$, 3,477 sq. mils
($1.549 \times 1.448\text{ mm}$, 224 sq. mm)

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the MAT02 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



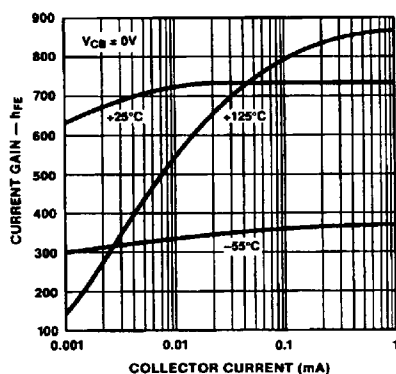


Figure 1. Current Gain vs. Collector Current

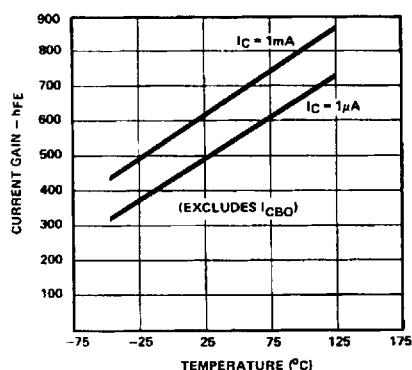


Figure 2. Current Gain vs. Temperature

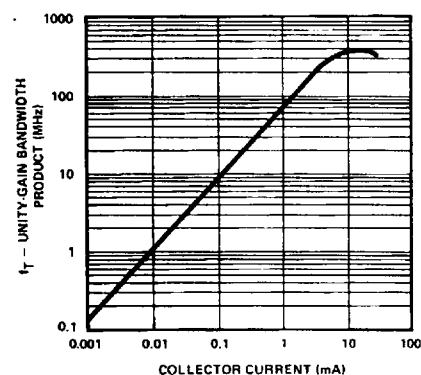


Figure 3. Gain Bandwidth vs. Collector Current

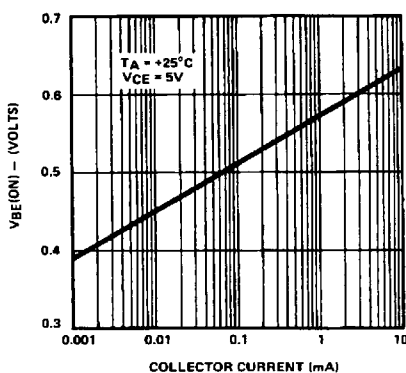


Figure 4. Base-Emitter-On Voltage vs. Collector Current

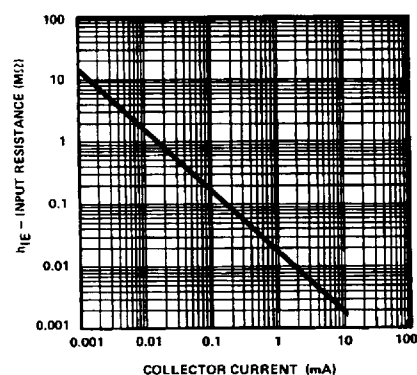


Figure 5. Small Signal Input Resistance vs. Collector Current

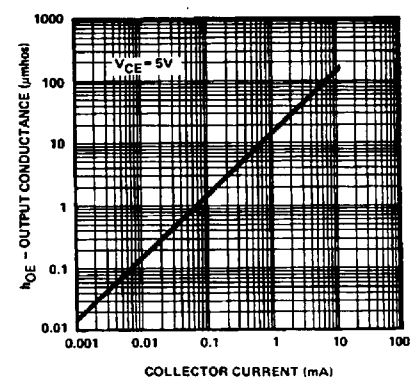


Figure 6. Small-Signal Output Conductance vs. Collector Current

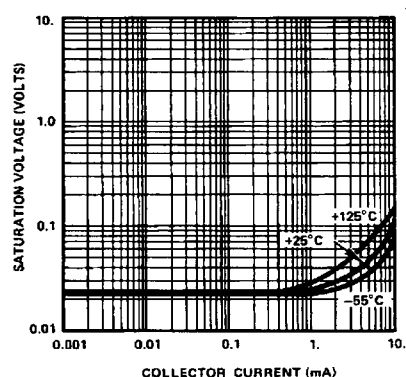


Figure 7. Saturation Voltage vs. Collector Current

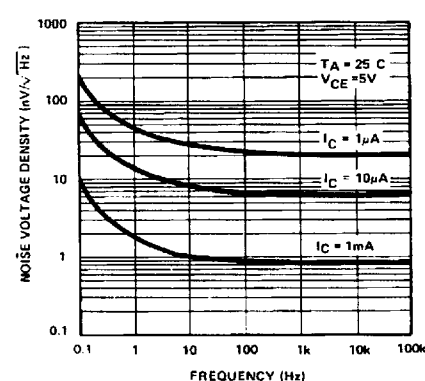


Figure 8. Noise Voltage Density vs. Frequency

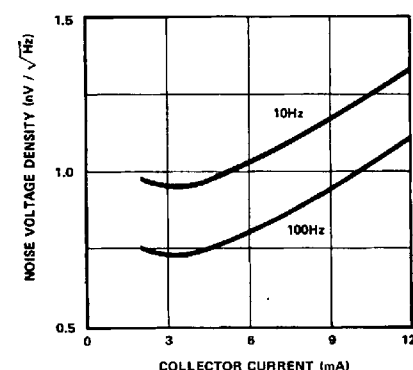


Figure 9. Noise Voltage Density vs. Collector Current

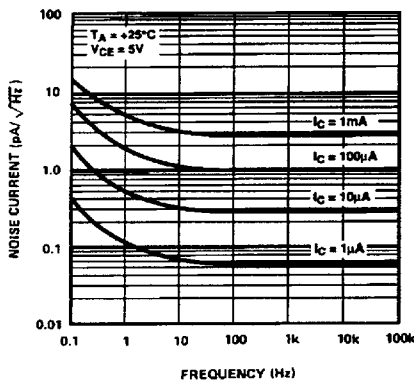


Figure 10. Noise Current Density vs. Frequency

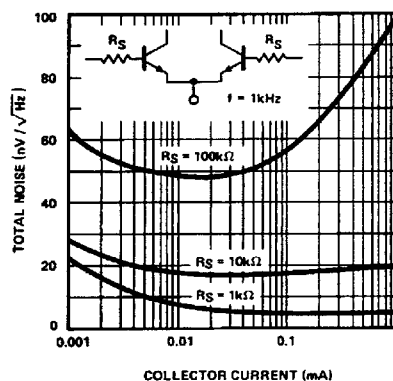


Figure 11. Total Noise vs. Collector Current

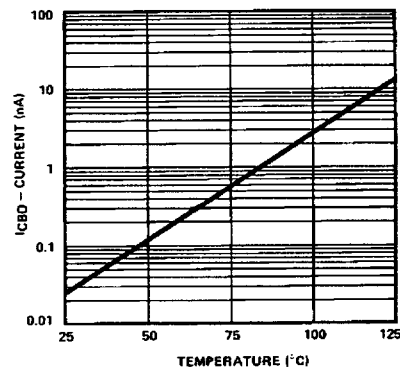


Figure 12. Collector-to-Base Leakage vs. Temperature

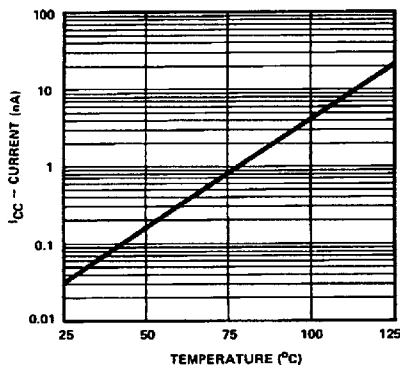


Figure 13. Collector-to-Collector Leakage vs. Temperature

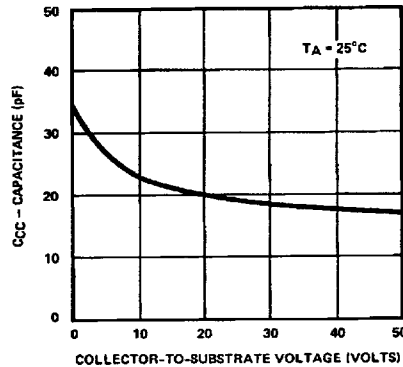


Figure 14. Collector-to-Collector Capacitance vs. Collector-to-Substrate Voltage

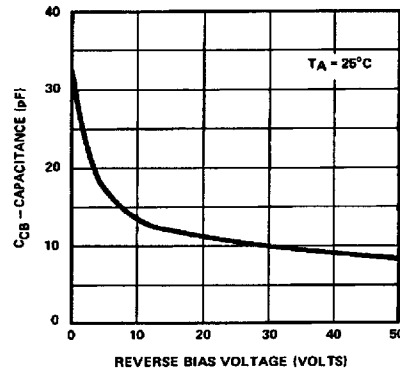


Figure 15. Collector-Base Capacitance vs. Reverse Bias Voltage

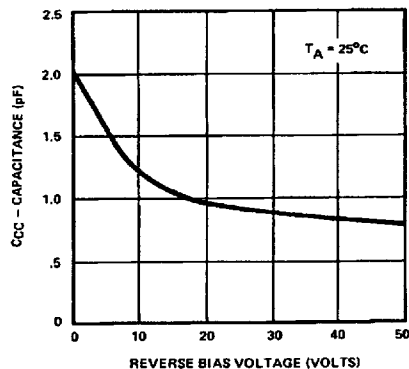


Figure 16. Collector-to-Collector Capacitance vs. Reverse Bias Voltage

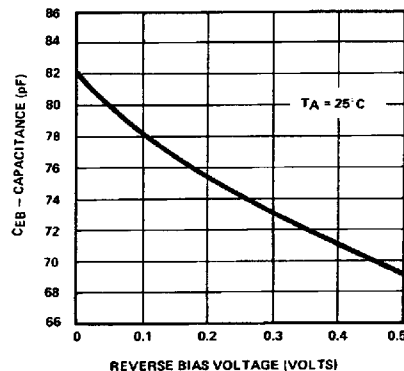


Figure 17. Emitter-Base Capacitance vs. Reverse Bias Voltage

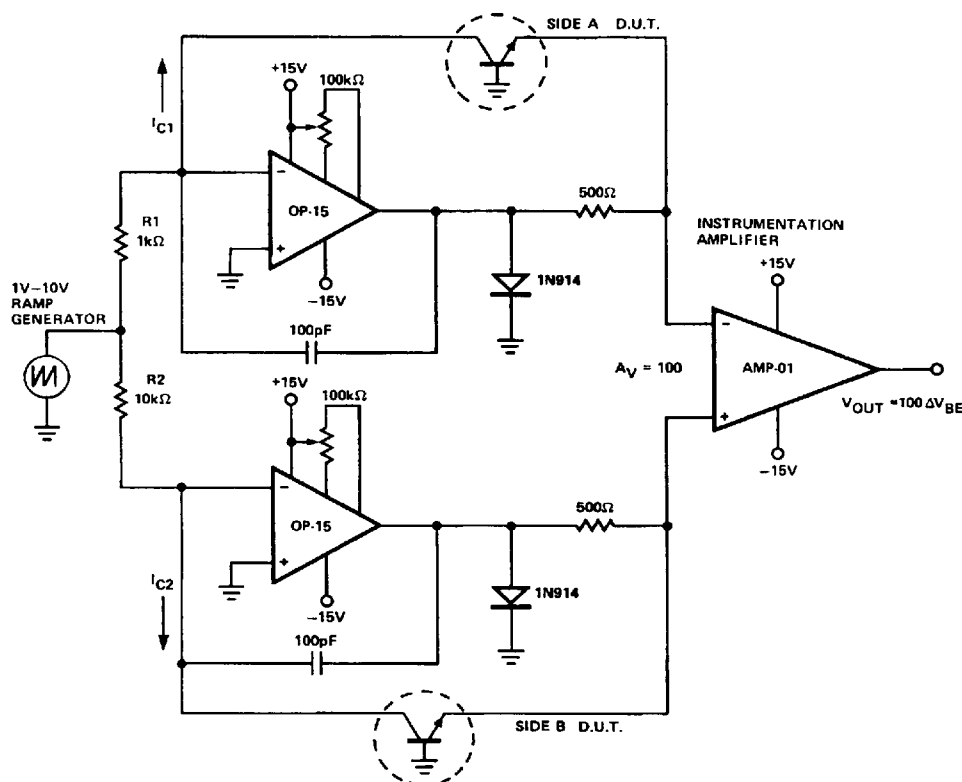


Figure 18. Log Conformance Test Circuit

LOG CONFORMANCE TESTING

The log conformance of the MAT02 is tested using the circuit shown above. The circuit employs a dual transdiode logarithmic converter operating at a fixed ratio of collector currents that are swept over a 10:1 range. The output of each transdiode converter is the V_{BE} of the transistor plus an error term which is the product of the collector current and r_{BE} , the bulk emitter resistance. The difference of the V_{BE} is amplified at a gain of $\times 100$ by the AMP01 instrumentation amplifier. The differential emitter-base voltage (ΔV_{BE}) consists of a temperature-dependent dc level plus an ac error voltage which is the deviation from true log conformity as the collector currents vary.

The output of the transdiode logarithmic converter comes from the idealized intrinsic transistor equation (for silicon):

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S} \text{ where} \quad (1)$$

k = Boltzmann's Constant ($1.38062 \times 10^{-23} \text{ J/}^\circ\text{K}$)

q = Unit Electron Charge ($1.60219 \times 10^{-19} \text{ }^\circ\text{C}$)

T = Absolute Temperature, $^\circ\text{K}$ ($= ^\circ\text{C} + 273.2$)

I_S = Extrapolated Current for $V_{BE} \rightarrow 0$

I_C = Collector Current

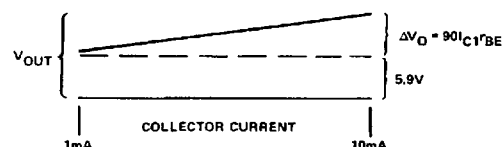
An error term must be added to this equation to allow for the bulk resistance (r_{BE}) of the transistor. Error due to the op amp input current is limited by use of the OP15 BiFET-input op amp. The resulting AMP01 input is:

$$\Delta V_{BE} = \frac{kT}{q} \ln \frac{I_{C1}}{I_{C2}} + I_{C1} r_{BE1} - I_{C2} r_{BE2} \quad (2)$$

A ramp function which sweeps from 1 V to 10 V is converted by the op amps to a collector current ramp through each transistor. Because I_{C1} is made equal to 10 I_{C2} , and assuming $T_A = 25^\circ\text{C}$, the previous equation becomes:

$$\Delta V_{BE} = 59 \text{ mV} + 0.9 I_{C1} r_{BE} (\Delta r_{BE} \sim 0)$$

As viewed on an oscilloscope, the change in ΔV_{BE} for a 10:1 change in I_C is then displayed as shown below:



MAT02

With the oscilloscope ac coupled, the temperature dependent term becomes a dc offset and the trace represents the deviation from true log conformity. The bulk resistance can be calculated from the voltage deviation ΔV_O and the change in collector current (9 mA):

$$r_{BE} = \frac{\Delta V_O}{9 \text{ mA}} \times \frac{1}{100} \quad (3)$$

This procedure finds r_{BE} for Side A. Switching R_1 and R_2 will provide the r_{BE} for Side B. Differential r_{BE} is found by making $R_1 = R_2$.

APPLICATIONS: NONLINEAR FUNCTIONS MULTIPLIER/DIVIDER CIRCUIT

The excellent log conformity of the MAT02 over a very wide range of collector current makes it ideal for use in log-antilog circuits. Such nonlinear functions as multiplying, dividing, squaring, and square-rooting are accurately and easily implemented with a log-antilog circuit using two MAT02 pairs (see Figure 19). The transistor circuit accepts three input currents (I_1 , I_2 , and I_3) and provides an output current I_O according to $I_O = I_1 I_2 / I_3$. All four currents must be positive in the log-antilog circuit, but negative input voltages can be easily accommodated

by various offsetting techniques. Protective diodes across each base-to-emitter junction would normally be needed, but these diodes are built into the MAT02. External protection diodes are therefore not needed.

For the circuit shown in Figure 19, the operational amplifiers make $I_1 = V_X / R_1$, $I_2 = V_Y / R_2$, $I_3 = V_Z / R_3$, and $I_O = V_O / R_O$. The output voltage for this one-quadrant, log-antilog multiplier/divider is ideally:

$$V_O = \frac{R_3 R_O}{R_1 R_2} \frac{V_X V_Y}{V_Z} \quad (V_X, V_Y, V_Z > 0) \quad (4)$$

If all the resistors (R_O , R_1 , R_2 , R_3) are made equal, then $V_O = V_X V_Y / V_Z$. Resistor values of 50 k Ω to 100 k Ω are recommended assuming an input range of 0.1 V to +10 V.

ERROR ANALYSIS

The base-to-emitter voltage of the MAT02 in its forward active operation is:

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S} + r_{BE} I_C, \quad V_{CB} \sim 0 \quad (5)$$

The first term comes from the idealized intrinsic transistor equation previously discussed (see equation (1)).

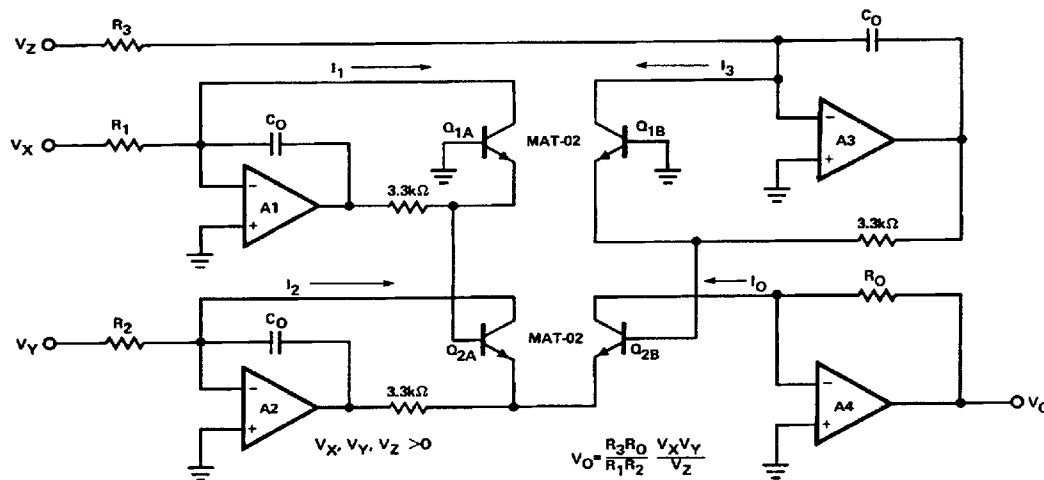


Figure 19. One-Quadrant Multiplier/Divider

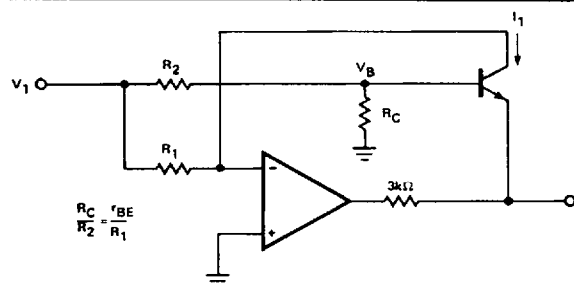


Figure 20. Compensation of Bulk Resistance Error

Extrinsic resistive terms and the early effect cause departure from the ideal logarithmic relationship. For small V_{CB} , all of these effects can be lumped together as a total effective bulk resistance r_{BE} . The $r_{BE}I_C$ term causes departure from the desired logarithmic relationship. The r_{BE} term for the MAT02 is less than 0.5Ω and Δr_{BE} between the two sides is negligible.

Returning to the multiplier/divider circuit of Figure 1 and using Equation (4):

$$V_{BE1A} + V_{BE2A} - V_{BE2B} - V_{BE1B} + (I_1 + I_2 - I_O - I_3) r_{BE} = 0$$

If the transistor pairs are held to the same temperature, then:

$$\frac{kT}{q} \ln \frac{I_1 I_2}{I_3 I_O} = \frac{kT}{q} \ln \frac{I_{SA} I_{S2A}}{I_{SB} I_{S2B}} + (I_1 + I_2 - I_O - I_3) r_{BE} \quad (6)$$

If all the terms on the right-hand side were zero, then we would have $\ln(I_1 I_2 / I_3 I_O)$ equal to zero which would lead directly to the desired result:

$$I_O = \frac{I_1 I_2}{I_3}, \text{ where } I_1, I_2, I_3, I_O > 0 \quad (7)$$

Note that this relationship is temperature independent. The right-hand side of Equation (6) is near zero and the output current I_O will be approximately $I_1 I_2 / I_3$. To estimate error, define ϕ as the right-hand side terms of Equation (6):

$$\phi = \ln \frac{I_{SA} I_{S2A}}{I_{SB} I_{S2B}} + \frac{q}{kT} (I_1 + I_2 - I_O - I_3) r_{BE} \quad (8)$$

For the MAT02, $\ln(I_{SA}/I_{SB})$ and $I_C r_{BE}$ are very small. For small ϕ , $e^\phi \sim 1 + \phi$ and therefore:

$$\frac{I_1 I_2}{I_3 I_O} = 1 + \phi \quad (9)$$

$$I_O = \frac{I_1 I_2}{I_3} (1 - \phi)$$

The $\ln(I_{SA}/I_{SB})$ terms in ϕ cause a fixed gain error of less than $\pm 0.6\%$ from each pair when using the MAT02, and this gain error is easily trimmed out by varying R_O . The $I_C r_{BE}$ terms are more troublesome because they vary with signal levels and are multiplied by absolute temperature. At 25°C , kT/q is

approximately 26 mV and the error due to an $r_{BE}I_C$ term will be $r_{BE}I_C/26 \text{ mV}$. Using an r_{BE} of 0.4Ω for the MAT02 and assuming a collector current range of up to $200 \mu\text{A}$, then a peak error of 0.3% could be expected for an $r_{BE}I_C$ error term when using the MAT02. Total error is dependent on the specific application configuration (multiply, divide, square, etc.) and the required dynamic range. An obvious way to reduce $I_C r_{BE}$ error is to reduce the maximum collector current, but then op amp offsets and leakage currents become a limiting factor at low input levels. A design range of no greater than $10 \mu\text{A}$ to 1 mA is generally recommended for most nonlinear function circuits.

A powerful technique for reducing error due to $I_C r_{BE}$ is shown in Figure 20. A small voltage equal to $I_C r_{BE}$ is applied to the transistor base. For this circuit:

$$V_B = \frac{R_C}{R_2} V_I \text{ and } I_C r_{BE} = \frac{r_{BE}}{R_1} V_I \quad (10)$$

The error from $r_{BE}I_C$ is cancelled if R_C/R_2 is made equal to r_{BE}/R_1 . Since the MAT02 bulk resistance is approximately 0.39Ω , an R_C of 3.9Ω and R_2 of $10 R_1$ will give good error cancellation.

In more complex circuits, such as the circuit in Figure 19, it may be inconvenient to apply a compensation voltage to each individual base. A better approach is to sum all compensation to the bases of Q1. The "A" side needs a base voltage of $(V_O/R_O + V_Z/R_3) r_{BE}$ and the "B" side needs a base voltage of $(V_X/R_1 + V_Y/R_2) r_{BE}$. Linearity of better than $\pm 0.1\%$ is readily achievable with this compensation technique.

Operational amplifier offsets are another source of error. In Figure 20, the input offset voltage and input bias current will cause an error in collector current of $(V_{OS}/R_1) + I_B$. A low offset op amp, such as the OP07 with less than $75 \mu\text{V}$ of V_{OS} and I_B of less than $\pm 3 \text{ nA}$, is recommended. The OP22/OP32, a programmable micropower op amp, should be considered if low power consumption or single-supply operation is needed. The value of frequency-compensating capacitor (C_O) is dependent on the op amp frequency response and peak collector current. Typical values for C_O range from 30 pF to 300 pF .

FOUR-QUADRANT MULTIPLIER

A simplified schematic for a four-quadrant log/antilog multiplier is shown in Figure 21. As with the previously discussed one-quadrant multiplier, the circuit makes $I_O = I_1 I_2 / I_3$. The two input currents, I_1 and I_2 , are each offset in the positive direction. This positive offset is then subtracted out at the output stage. Assuming ideal op amps, the currents are:

$$I_1 = \frac{V_X}{R_1} + \frac{V_R}{R_2}, I_2 = \frac{V_Y}{R_1} + \frac{V_R}{R_2} \quad (11)$$

$$I_O = \frac{V_X}{R_1} + \frac{V_Y}{R_1} + \frac{V_R}{R_2} + \frac{V_O}{R_O}, I_3 = \frac{V_R}{R_2}$$

From $I_O = I_1 I_2 / I_3$, the output voltage will be:

$$V_O = \frac{R_O R_2}{R_1^2} \frac{V_X V_Y}{V_R} \quad (12)$$

MAT02

Collector-current range is the key design decision. The inherently low r_{BE} of the MAT02 allows the use of a relatively high collector current. For input scaling of ± 10 V full-scale and using a 10 V reference, we have a collector-current range for I_1 and I_2 of:

$$\left(\frac{-10}{R_1} + \frac{10}{R_2}\right) \leq I_C \leq \left(\frac{10}{R_1} + \frac{10}{R_2}\right) \quad (13)$$

Practical values for R_1 and R_2 would range from 50 k Ω to 100 k Ω . Choosing an R_1 of 82 k Ω and R_2 of 62 k Ω provides a collector-current range of approximately 39 μ A to 283 μ A. An R_O of 108 k Ω will then make the output scale factor 1/10 and $V_O = V_X V_Y / 10$. The output, as well as both inputs, are scaled for ± 10 V full scale.

Linear error for this circuit is substantially improved by the small correction voltage applied to the base of Q1 as shown in Figure 21. Assuming an equal bulk emitter resistance for each MAT02 transistor, then the error is nulled if:

$$(I_1 + I_2 - I_3 - I_O) r_{BE} + \rho V_O = 0$$

The currents are known from the previous discussion, and the relationship needed is simply:

$$V_O = \frac{r_{BE}}{R_O} V_O \quad (14)$$

The output voltage is attenuated by a factor of r_{BE}/R_O and applied to the base of Q1 to cancel the summation of voltage drops due to $r_{BE}I_C$ terms. This will make $\ln(I_1 I_2 / I_3 I_O)$ more nearly zero which will thereby make $I_O = I_1 I_2 / I_3$ a more accurate relationship. Linearity of better than 0.1% is readily achievable with this circuit if the MAT02 pairs are carefully kept at the same temperature.

MULTIFUNCTION CONVERTER

The multifunction converter circuit provides an accurate means of squaring, square rooting, and of raising ratios to arbitrary powers. The excellent log conformity of the MAT02 allows a wide range of exponents. The general transfer function is:

$$V_O = V_Y \left(\frac{V_Z}{V_X} \right)^m \quad (15)$$

V_X , V_Y , and V_Z are input voltages and the exponent "m" has a practical range of approximately 0.2 to 5. Inputs V_X and V_Y are often taken from a fixed reference voltage. With a REF01 providing a precision +10 V to both V_X and V_Y , the transfer function would simplify to:

$$V_O = 10 \left(\frac{V_Z}{10} \right)^m \quad (16)$$

As with the multiplier/divider circuits, assume that the transistor pairs have excellent matching and are at the same temperature. The $\ln I_{SA}/I_{SB}$ will then be zero. In the circuit of Figure 22, the voltage drops across the base-emitter junctions of Q1 provide:

$$\frac{R_B}{R_B + KR_A} V_A = \frac{kT}{q} \ln \frac{I_Z}{I_X} \quad (17)$$

I_Z is V_Z/R_1 and I_X is V_X/R_1 . Similarly, the relationship for Q2 is:

$$\frac{R_B}{R_B + (1-K)R_A} V_A = \frac{kT}{q} \ln \frac{I_O}{I_Y} \quad (18)$$

I_O is V_O/R_O and I_Y is V_Y/R_1 . These equations for Q1 and Q2 can then be combined.

$$\frac{R_B + KR_A}{R_B + (1-K)R_A} \ln \frac{I_Z}{I_X} = \ln \frac{I_O}{I_Y} \quad (19)$$

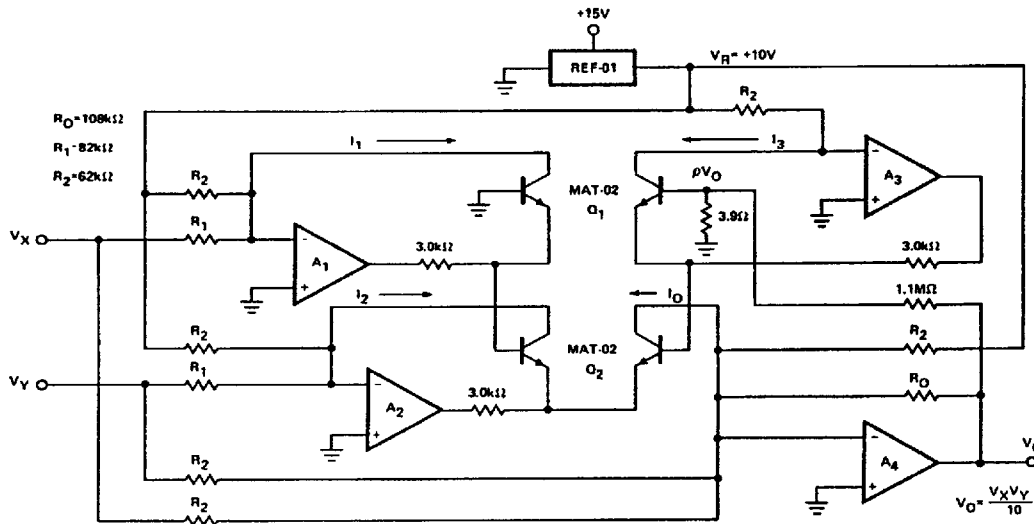


Figure 21. Four-Quadrant Multiplier

MAT02

Transistors Q2 and Q3 form a 2 mA current source (0.65 V/330 Ω ~ 2 mA). Each collector of Q1 operates at 1 mA. The OP32 inputs are 3 V below the positive supply voltage ($R_L I_C$ ~ 3 V). The OP32's low input offset current, typically less than 1 nA, and low offset voltage of 1 mV cause negligible error when referred to the amplifier input. Input stage gain is $g_m R_L$, which is approximately 100 when operating at I_C of 1 mA with R_L of 3 k Ω . Since the OP32 has a minimum open-loop gain of 500,000, total open-loop gain for the composite amplifier is over 50 million. Even at closed-loop gain of 1000, the gain error due to finite open-loop gain will be negligible. The OP32 features excellent symmetry of slew-rate and very linear gain. Signal distortion is minimal.

Frequency compensation is very easy with this circuit; just vary the set-resistor R_S for the desired frequency response. Gain-bandwidth of the OP32 varies directly with the supply

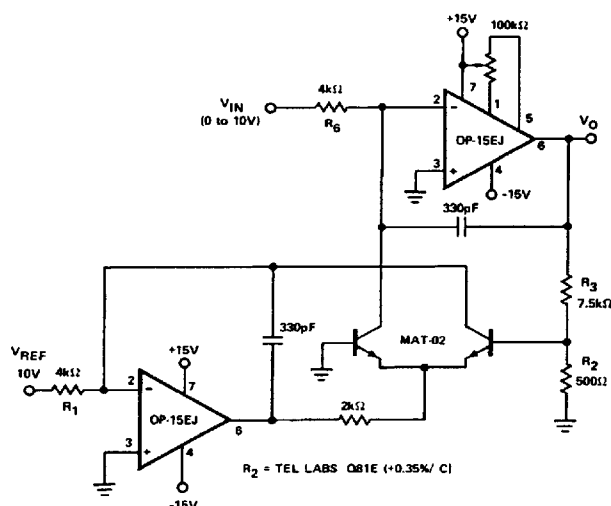


Figure 23. Fast Logarithmic Amplifier

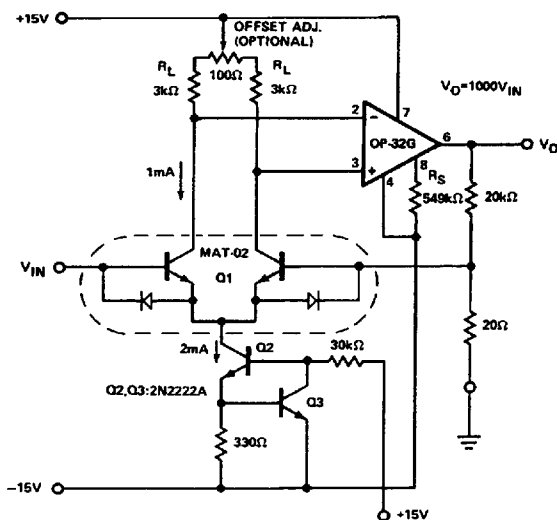


Figure 24. Low-Noise, Single-Ended X1000 Amplifier

current. A set resistor of 549 k Ω was found to provide the best step response for this circuit. The resultant supply current is found from:

$$R_{SET} = \frac{(V_+) - (V_-) - (2V_{BE})}{I_{SET}}, I_{SY} = 15 I_{SET} \quad (22)$$

The I_{SET} , using ± 15 V supplies and an R_{SET} of 549 k Ω , is approximately 52 μ A which will result in supply current of 784 μ A. Dynamic range of this amplifier is excellent; the OP32 has an output voltage swing of ± 14 V with a ± 15 V supply.

Input characteristics are outstanding. The MAT02F has offset voltage of less than 150 μ V at 25°C and a maximum offset drift of 1 μ V/°C. Nulling the offset will further reduce offset drift. This can be accomplished by slightly unbalancing the collector load resistors. This adjustment will reduce the drift to less than 0.1 μ V/°C.

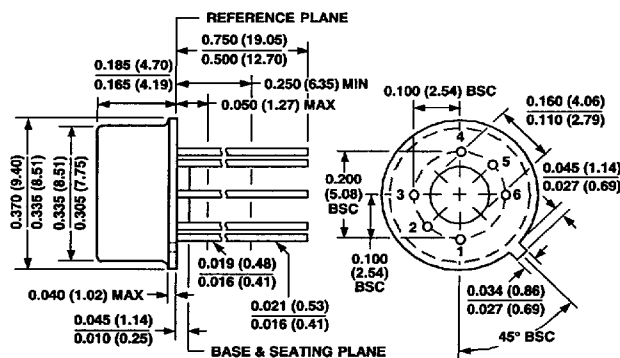
Input bias current is relatively low due to the high current gain of the MAT02. The minimum β of 400 at 1 mA for the MAT02F implies an input bias current of approximately 2.5 μ A. This circuit should be used with signals having relatively low source impedance. A high source impedance will degrade offset and noise performance.

This circuit configuration provides exceptionally low input noise voltage and low drift. Noise can be reduced even further by raising the collector currents from 1 mA to 3 mA, but power consumption is then increased.

OUTLINE DIMENSION

Dimensions shown in inches and (mm).

6-Lead Metal Can (TO-78)



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