CY62157ESL MoBL®

8-Mbit (512K x 16) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
  - Typical Standby current: 2 µA
  - Maximum Standby current: 8 µA
- Ultra low active power
  - Typical active current: 1.8 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package

Functional Description

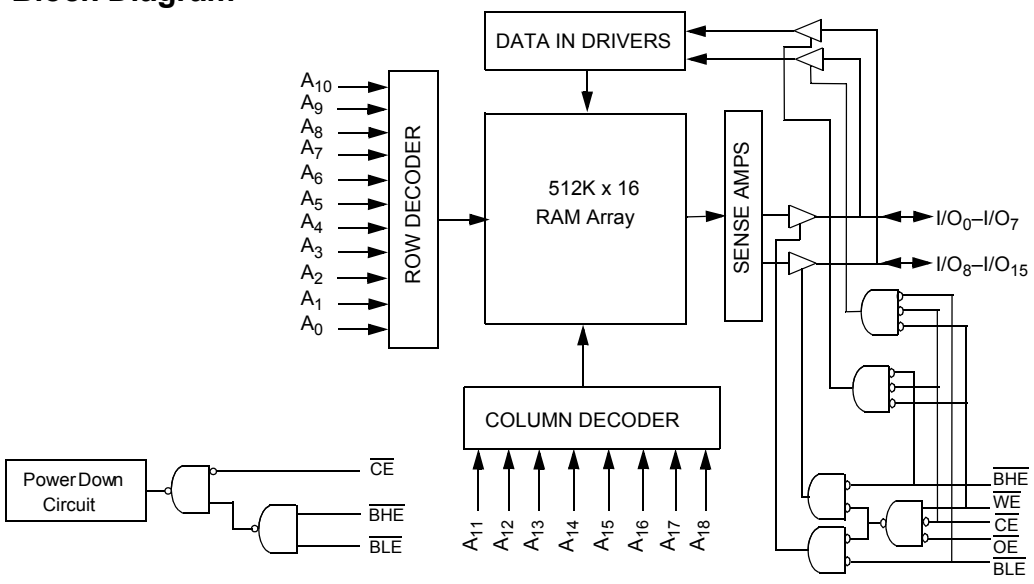
The CY62157ESL is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device into standby mode when deselected ($\overline{CE}$ HIGH or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input or output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), both the Byte High Enable and the Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during an active write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Logic Block Diagram



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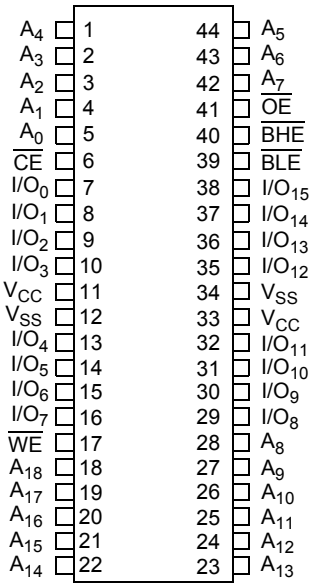
Pin Configuration

Figure 1. 44-Pin TSOP II (Top View)



Product Portfolio

Product	Range	V_{CC} Range (V) [1]	Speed (ns)	Power Dissipation					
				Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
				f = 1MHz		f = f_{max}			
				Typ[2]	Max	Typ [2]	Max	Typ [2]	Max
CY62157ESL	Industrial	2.2 V–3.6 V and 4.5 V–5.5 V	45	1.8	3	18	25	2	8

Notes
1. Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3V, and V_{CC} = 5V, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage to Ground Potential ..... –0.5 V to 6.0 V

DC Voltage Applied to Outputs in High-Z State[3, 4] ..... –0.5 V to 6.0 V

DC Input Voltage[3, 4] ..... –0.5 V to 6.0 V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001 V (MIL-STD-883, Method 3015)

Latch up Current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[5]
CY62157ESL	Industrial	–40°C to +85°C	2.2 V–3.6 V, and 4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ[6]	Max	
V_{OH}	Output high voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0			V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4			
		$4.5 \le V_{CC} \le 5.5$	I_{OH} = –1.0 mA	2.4			
V_{OL}	Output low voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA			0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OL} = 2.1 mA			0.4	
		$4.5 \le V_{CC} \le 5.5$	I_{OL} = 2.1 mA			0.4	
V_{IH}	Input high voltage	$2.2 \le V_{CC} \le 2.7$		1.8		V_{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2		V_{CC} + 0.3	
		$4.5 \le V_{CC} \le 5.5$		2.2		V_{CC} + 0.5	
V_{IL}	Input low voltage	$2.2 \le V_{CC} \le 2.7$		–0.3		0.6	V
		$2.7 \le V_{CC} \le 3.6$		–0.3		0.8	
		$4.5 \le V_{CC} \le 5.5$		–0.5		0.8	
I_{IX}	Input leakage current	$GND \le V_I \le V_{CC}$		–1		+1	µA
I_{OZ}	Output leakage current	$GND \le V_O \le V_{CC}$, Output Disabled		–1		+1	µA
I_{CC}	V_{CC} operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$, I_{OUT} = 0 mA, CMOS levels		18	25	mA
		f = 1 MHz			1.8	3	
I_{SB1}	Automatic CE power down current — CMOS inputs	$\overline{CE} \ge V_{CC}$ – 0.2 V, $V_{IN} \ge V_{CC}$ – 0.2 V or $V_{IN} \le$ 0.2 V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), $V_{CC} = V_{CC(max)}$			2	8	µA
I_{SB2}[7]	Automatic CE power down current — CMOS inputs	$\overline{CE} \ge V_{CC}$ – 0.2 V, $V_{IN} \ge V_{CC}$ – 0.2 V or $V_{IN} \le$ 0.2 V, f = 0, $V_{CC} = V_{CC(max)}$			2	8	µA

Notes

3. VIL (min) = –2.0V for pulse durations less than 20 ns.
4. VIH (max) = VCC + 0.75 V for pulse durations less than 20 ns.
5. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3V, and V_{CC} = 5V, T_A = 25 °C.
7. Chip enable ($\overline{CE}$) needs to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

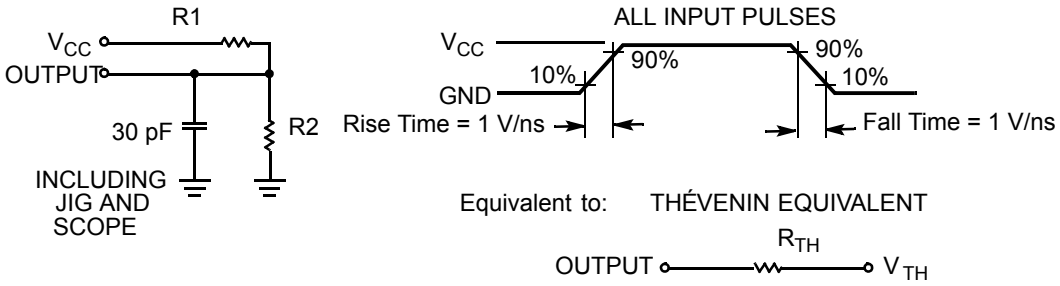
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	77	°C/W
Θ_{JC}	Thermal resistance (Junction to case)		13	°C/W

Figure 2. AC Test Loads and Waveforms



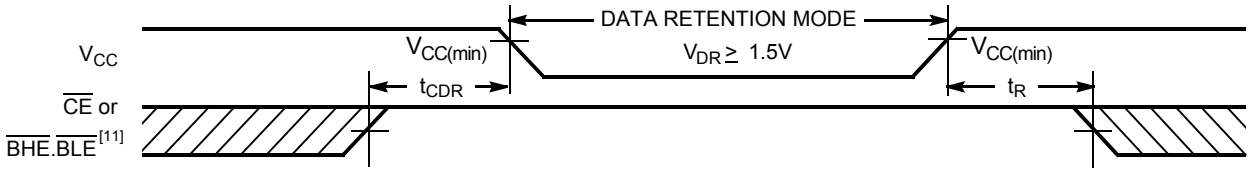
Parameters	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R_{TH}	8000	645	639	Ω
V_{TH}	1.20	1.75	1.77	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ[8]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5			V
I_{CCDR}	Data retention current	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	V_{CC} = 1.5 V		2	5	µA
			V_{CC} = 2.0 V		2	8	
t_{CDR} [9]	Chip deselect to data retention time			0			ns
t_R [10]	Operation recovery time			45			ns

Figure 3. Data Retention Waveform



Notes

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3V, and V_{CC} = 5V, T_A = 25°C.
9. Tested initially and after any design or process changes that may affect these parameters.
10. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
11. BHE.BLE is the AND of both BHE and BLE. Deselect the chip by either disabling chip enable signals or by disabling both BHE and BLE.

Switching Characteristics

Over the Operating Range [12]

Parameter	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45		ns
t_{AA}	Address to data valid		45	ns
t_{OHA}	Data hold from address change	10		ns
t_{ACE}	$\overline{CE}$ LOW to data valid		45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid		22	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW-Z[13]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[13, 14]		18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[13]	10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[13, 14]		18	ns
t_{PU}	$\overline{CE}$ LOW to power up	0		ns
t_{PD}	$\overline{CE}$ HIGH to power down		45	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid		45	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low-Z[13, 15]	5		ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to HIGH-Z[13, 14]		18	ns
Write Cycle[16]				
t_{WC}	Write cycle time	45		ns
t_{SCE}	$\overline{CE}$ LOW to write end	35		ns
t_{AW}	Address setup to write end	35		ns
t_{HA}	Address hold from write end	0		ns
t_{SA}	Address setup to write start	0		ns
t_{PWE}	$\overline{WE}$ pulse width	35		ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	35		ns
t_{SD}	Data setup to write end	25		ns
t_{HD}	Data hold from write end	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[13, 14]		18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[13]	10		ns

Notes

12. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3V, and output loading of the specified IOL/IOH as shown in the AC Test Loads and Waveforms on page 5.
13. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
14. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
15. If both byte enables are toggled together, this value is 10 ns.
16. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle No.1: Address Transition Controlled. [17, 18]

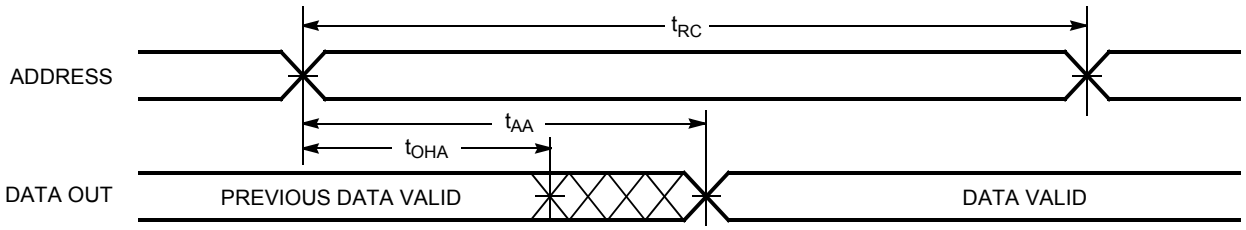
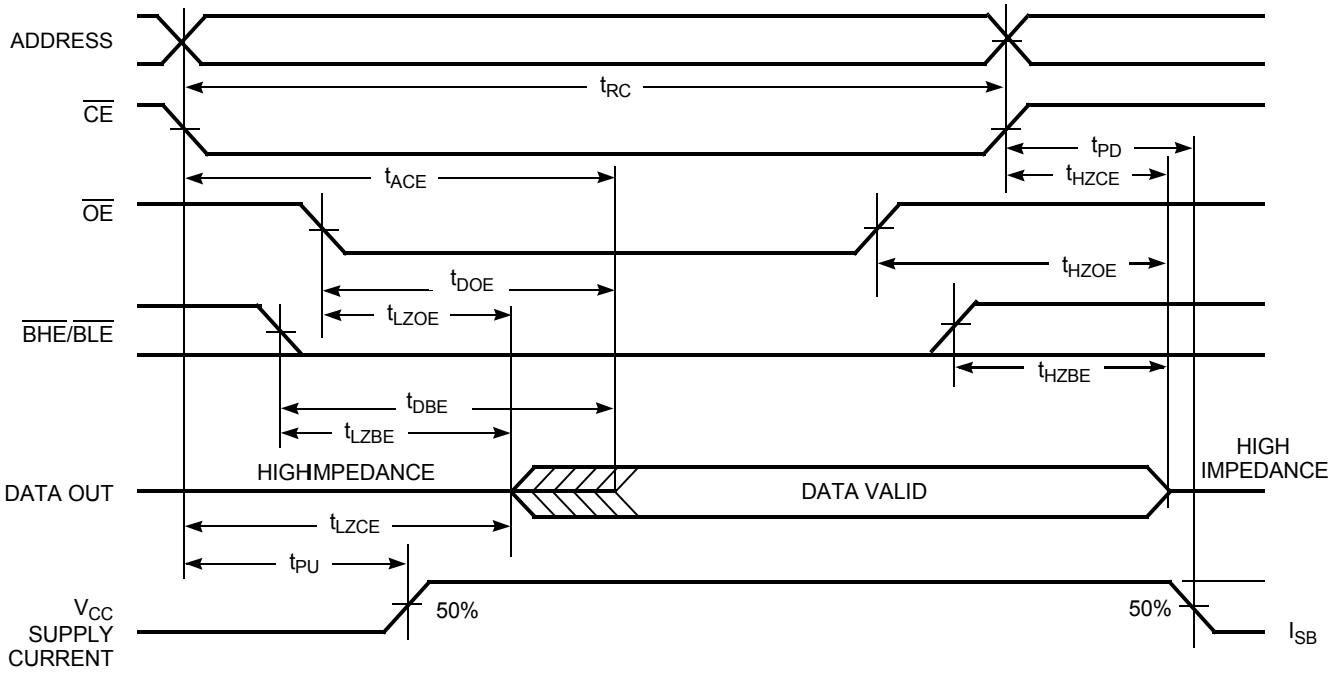


Figure 5. Read Cycle No. 2: $\overline{OE}$ Controlled [18, 19]



Notes
17. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}.
18. $\overline{WE}$ is HIGH for read cycle.
19. Address valid before or similar to $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No 1: $\overline{WE}$ Controlled [20, 21, 22]

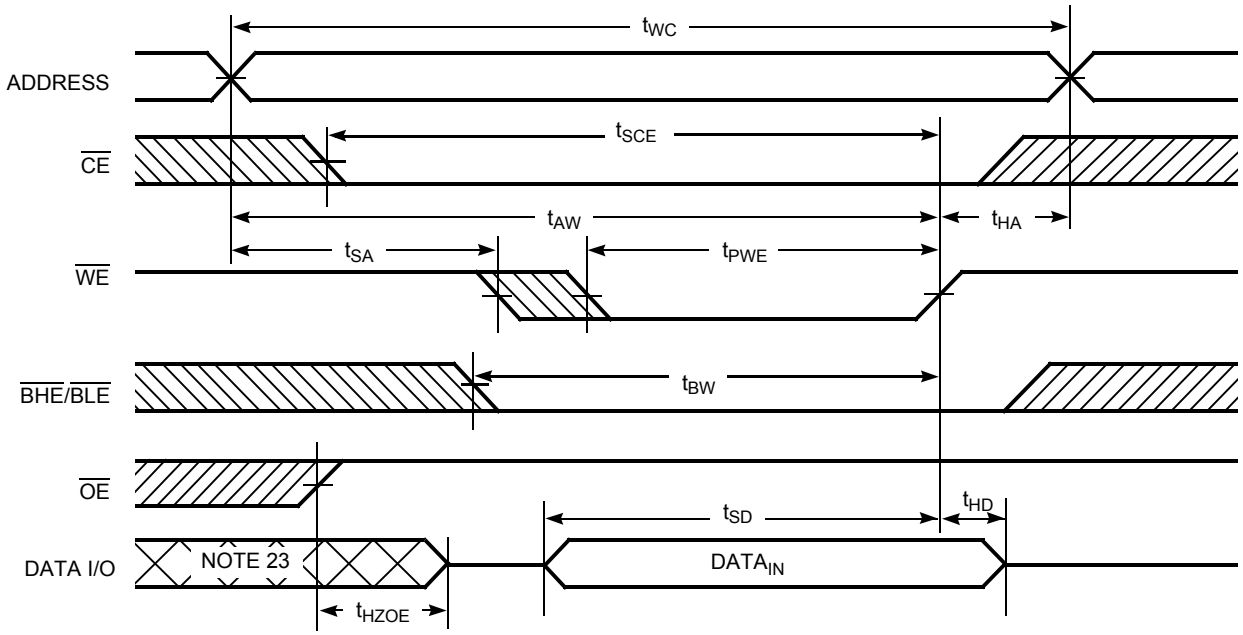
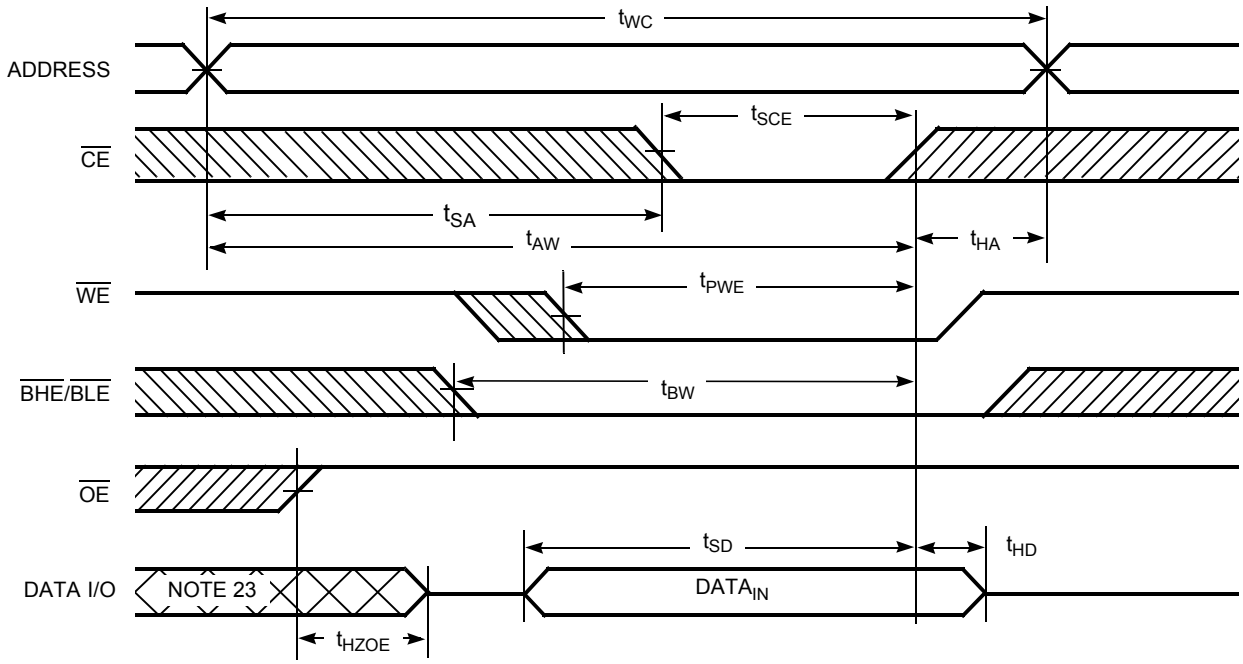


Figure 7. Write Cycle 2: $\overline{CE}$ Controlled [20, 21, 22]



Notes

20. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
21. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
22. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
23. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle 3: $\overline{WE}$ controlled, $\overline{OE}$ LOW [24, 25, 26]

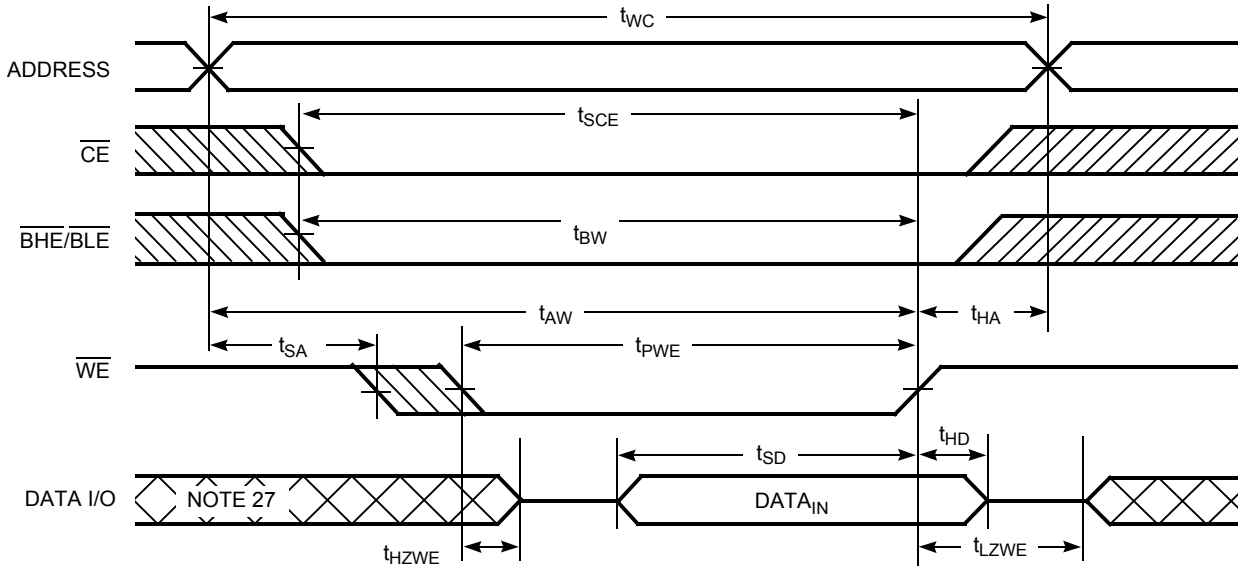
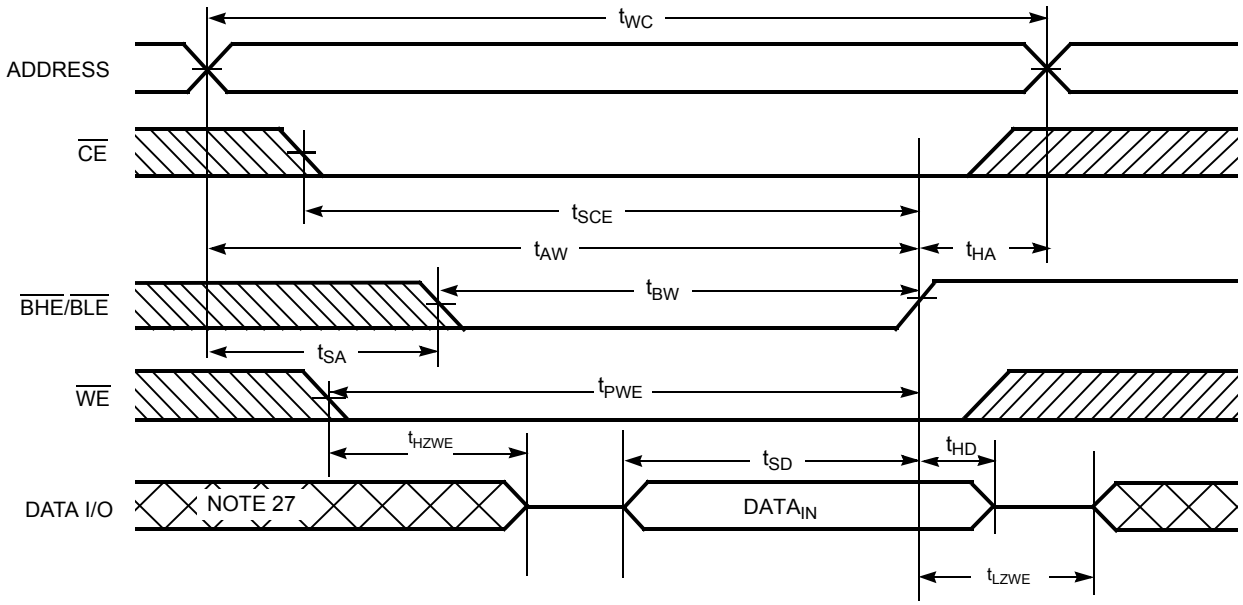


Figure 9. Write Cycle 4: $\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW [24, 25, 26]



Notes

24. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
25. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
26. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
27. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

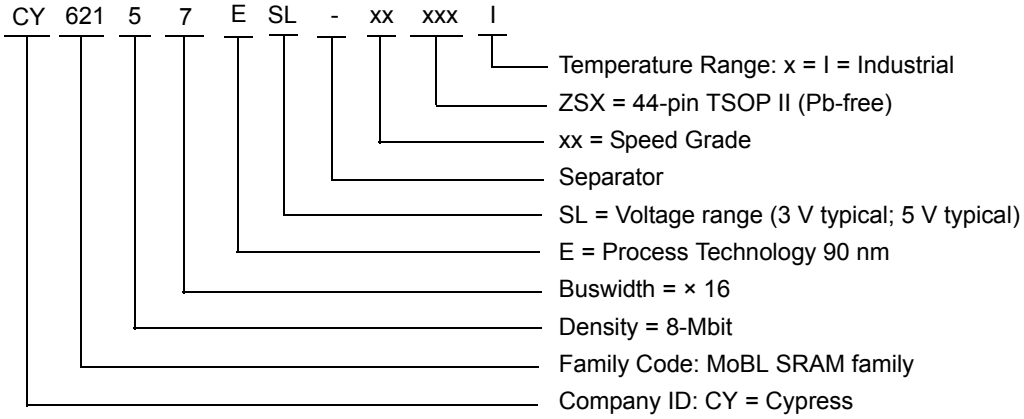
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/power down	Standby (I_{SB})
X[28]	X	X	H	H	High-Z	Deselect/power down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Write	Active (I_{CC})

Note
28. The 'X' (Don't care) state for the Chip enable in the truth table refers to the logic state (either HIGH or LOW). Intermediate voltage levels on this pin is not permitted.

Ordering Information

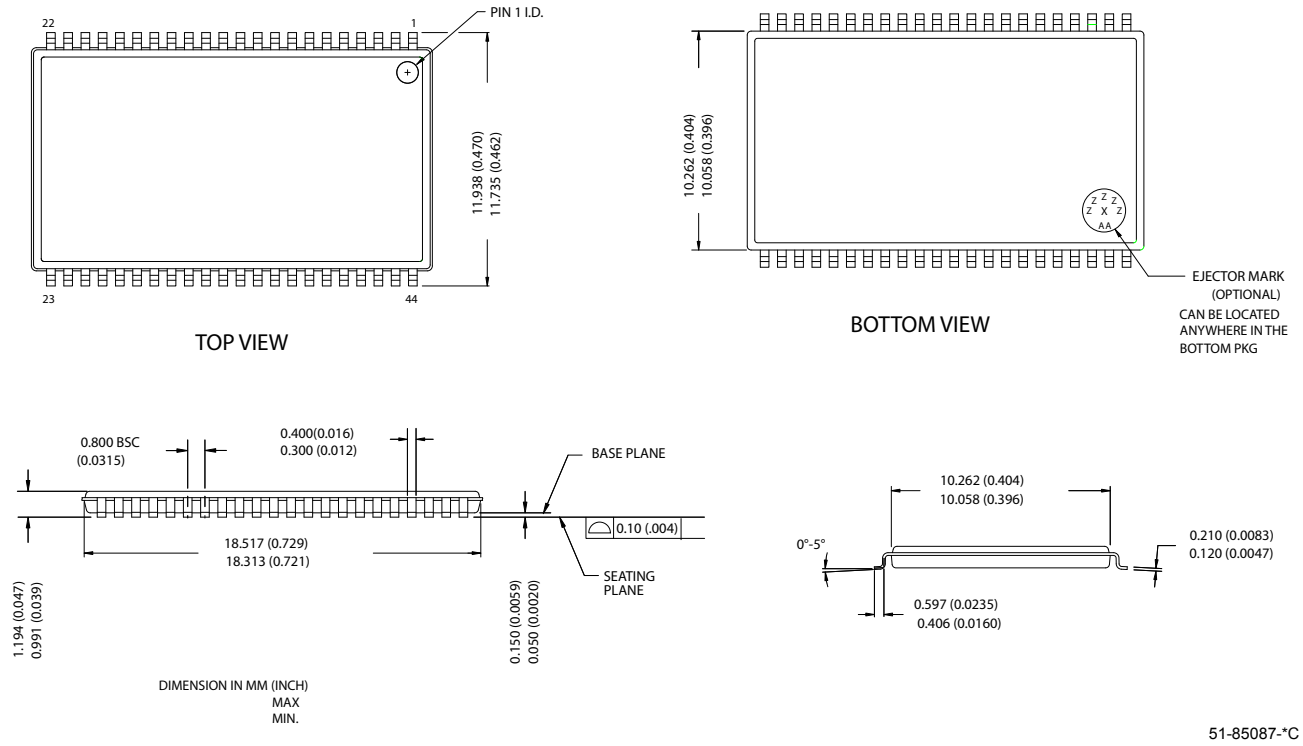
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157ESL-45ZSXI	51-85087	44-pin thin small outline package type II (Pb-free)	Industrial

Ordering Code Definitions



Package Diagram

Figure 10. 44-Pin TSOP II, 51-85087



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
VFBGA	very fine ball gird array
TSOP	thin small outline package

Document History Page

Document Title: CY62157ESL MoBL® 8-Mbit (512K x 16) Static RAM Document Number: 001-43141				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	1875228	See ECN	VKN/AESA	New Data Sheet
*A	2943752	06/03/2010	VKN	Added Contents Added footnote for the ISB2 parameter in Electrical Characteristics Added footnote related to chip enable in Truth Table Updated Package Diagram Added Sales, Solutions, and Legal Information
*B	3109266	12/13/2010	PRAS	Changed Table Footnotes to Footnotes. Added Ordering Code Definitions.

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