Final COM'L MIL

T-46-19-07

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# PAL22V10-10/15
# AmPAL22V10/A
# PALCE22V10H-15/25/Q-25

**24-pin TTL/CMOS Versatile PAL® Device**

**Advanced Micro Devices**

## DISTINCTIVE CHARACTERISTICS

- As fast as 10 ns propagation delay and 71 MHz $f_{MAX}$
- Low-power EE CMOS versions
- 10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs
- Varied product term distribution allows up to 16 product terms per output for complex functions
- Global asynchronous reset and synchronous preset for initialization
- Power-up reset for initialization and register preload for testability
- Easy design with PALASM® software
- Programmable on standard PAL device programmers
- 24-pin SKINNYDIP® and 28-pin PLCC packages save space

## GENERAL DESCRIPTION

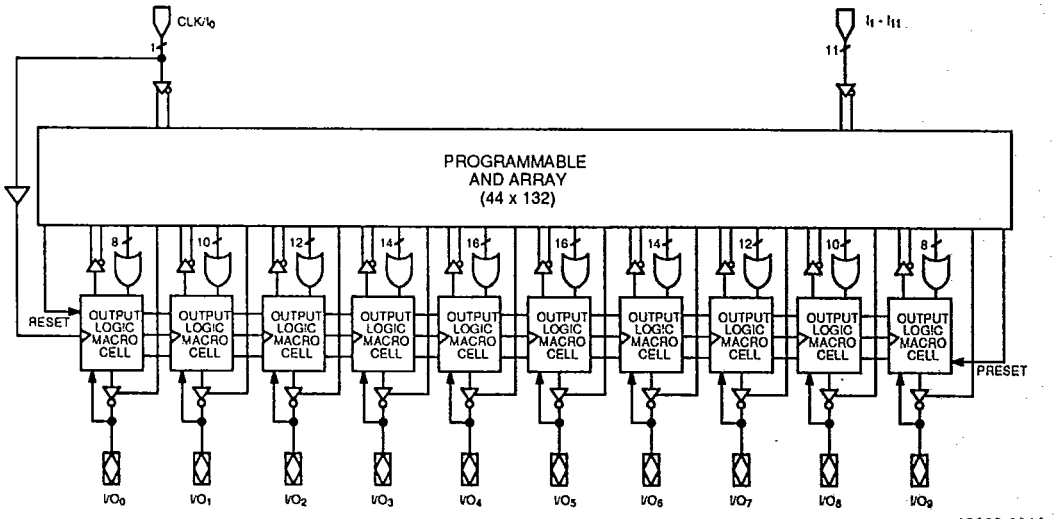
The PAL22V10 provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two fuses controlling two multiplexers in each macrocell.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers.

## BLOCK DIAGRAM

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Publication # 14004 Rev. A Amendment /0
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## PERFORMANCE OPTIONS
### Commercial

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| Speed ($t_{PD}$, ns) | Power ($I_{CC}$, mA) | | |
|---|---|---|---|
| | 55 | 90 | 180 |
| 35 | | | Std |
| 25 | CMOS Q-25 | CMOS H-25 | A |
| 15 | | CMOS H-15 | -15 |
| 10 | | | -10 |

## OPERATING RANGES

| Commercial | Military |
|---|---|
| -10 | -15 |
| -15 | -20 |
| A (25 ns) | A (30 ns) |
| Std (35 ns) | Std (40 ns) |
| H-15 | H-25 |
| H-25 | H-30 |
| Q-25 | |

## CONNECTION DIAGRAMS
**Top View**

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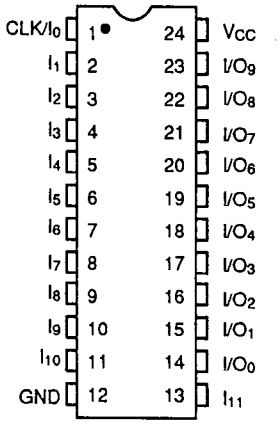
### SKINNYDIP/FLATPACK

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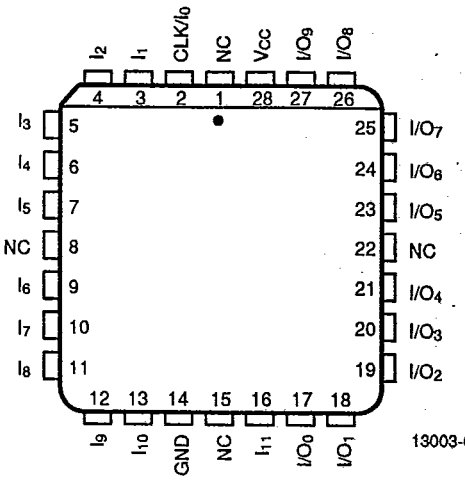
### PLCC/LCC

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**Note:**
Pin 1 is marked for orientation.

## PIN DESIGNATIONS

| | |
|---|---|
| CLK | Clock |
| GND | Ground |
| I | Input |
| I/O | Input/Output |
| NC | No Connect |
| Vcc | Supply Voltage |

## ORDERING INFORMATION
## Commercial Products

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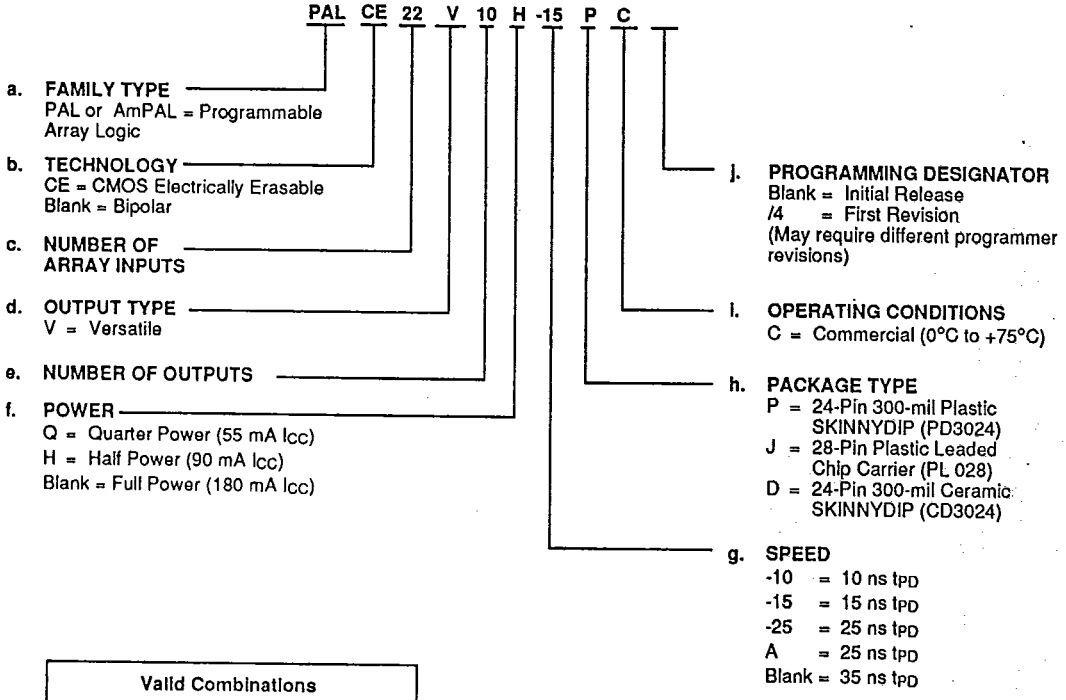
AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Number of Array Inputs
d. Output Type
e. Number of Outputs
f. Power
g. Speed
h. Package Type
i. Operating Conditions
j. Programming Designator




| Valid Combinations | | |
|---|---|---|
| PAL22V10-10 | PC, JC, DC | |
| PAL22V10-15 | | |
| AmPAL22V10A | | |
| AmPAL22V10 | | |
| PALCE22V10H-15 | | blank, |
| PALCE22V10H-25 | | /4 |
| PALCE22V10Q-25 | | |

### Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

## ORDERING INFORMATION
## APL Products

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AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Technology**
c. **Number of Array Inputs**
d. **Output Type**
e. **Number of Outputs**
f. **Power**
g. **Speed**
h. **Programming Designator**
i. **Device Class**
j. **Package Type**
k. **Lead Finish**

**PAL CE 22 V 10 H -25 /B L A**

a. **FAMILY TYPE**
PAL or AmPAL = Programmable Array Logic

b. **TECHNOLOGY**
CE = CMOS Electrically Erasable
Blank = Bipolar

c. **NUMBER OF ARRAY INPUTS**

d. **OUTPUT TYPE**
V = Versatile

e. **NUMBER OF OUTPUTS**

f. **POWER**
H = Half Power (100 mA $I_{CC}$)
Blank = Full Power (180–200 mA $I_{CC}$)

k. **LEAD FINISH**
A = Hot Solder Dip

j. **PACKAGE TYPE**
L = 24-Pin 300-mil Ceramic SKINNYDIP (CD3024)
K = 24-Pin Ceramic Flatpack (CFL024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL028)

i. **DEVICE CLASS**
/B = Class B

h. **PROGRAMMING DESIGNATOR**
Blank = Initial Release
E4 = First Revision
(May require different programmer revisions)

g. **SPEED**
-15 = 15 ns $t_{PD}$
-20 = 20 ns $t_{PD}$
-25 = 25 ns $t_{PD}$
-30 = 30 ns $t_{PD}$
A = 30 ns $t_{PD}$
Blank = 40 ns $t_{PD}$

| Valid Combinations | |
|---|---|
| PAL22V10-15 | /BLA, /BKA, /B3A |
| PAL22V10-20 | |
| AmPAL22V10A | |
| AmPAL22V10 | |
| PALCE22V10H-25 | blank, E4 |
| PALCE22V10H-30 | |

**Valid Combinations**

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

**Group A Tests**
Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

**Military Burn-In**
Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

## FUNCTIONAL DESCRIPTION

The PAL22V10 allows the systems engineer to implement the design on-chip, by opening fuse links (or programming EE cells) to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PAL22V10 has 12 inputs and 10 I/O macrocells (Figure 1). The macrocell allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits $S_0$ - $S_1$. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Programming the fuse or erasing the bit disconnects the control line from GND and it floats to $V_{CC}$ (1), selecting the "1" path.

The device is produced with a fuse or EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

### Variable Input/Output Pin Ratio

The PAL22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to $V_{CC}$ or GND.

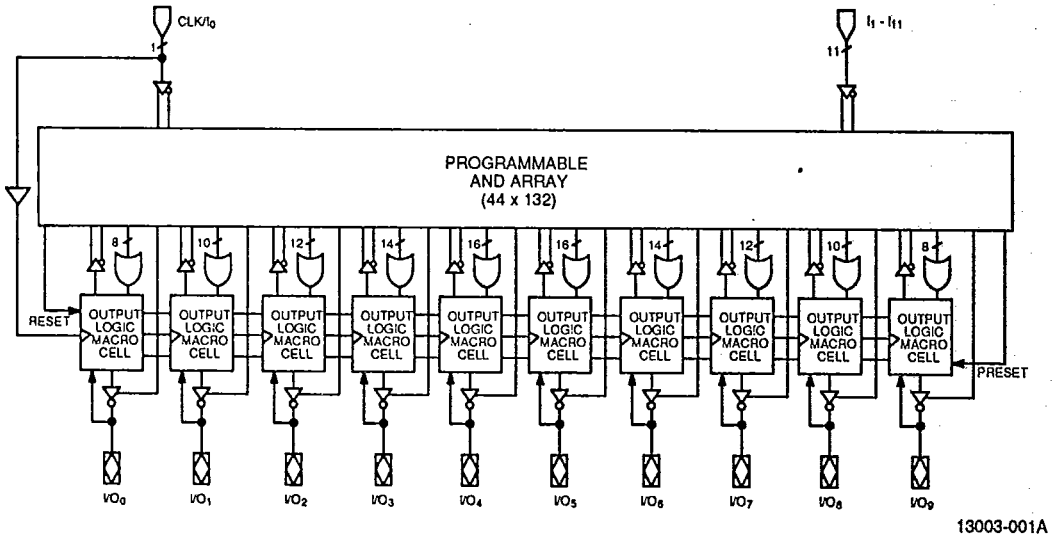


**Figure 1. Block Diagram**

## Registered Output Configuration

Each macrocell of the PAL22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

## Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.

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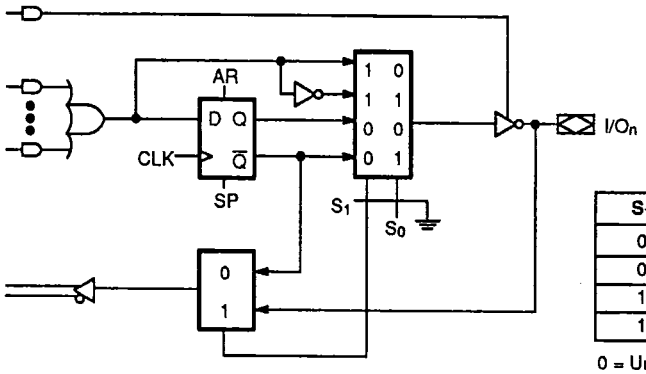


| $S_1$ | $S_0$ | Output Configuration |
|---|---|---|
| 0 | 0 | Registered/Active Low |
| 0 | 1 | Registered/Active High |
| 1 | 0 | Combinatorial/Active Low |
| 1 | 1 | Combinatorial/Active High |

0 = Unprogrammed fuse or programmed EE bit
1 = Programmed fuse or erased (charged) EE bit

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**Figure 2. Output Logic Macrocell Diagram**

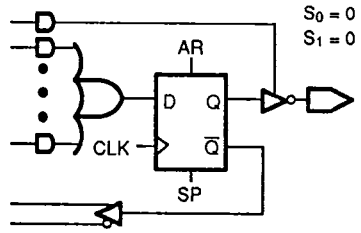


Figure 3a. Registered/Active Low

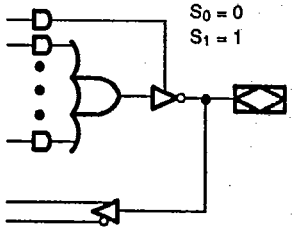


Figure 3c. Combinatorial/Active Low

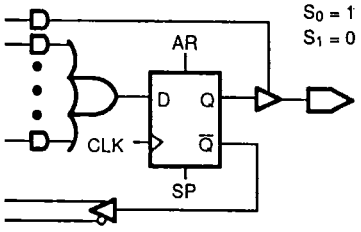


Figure 3b. Registered/Active High

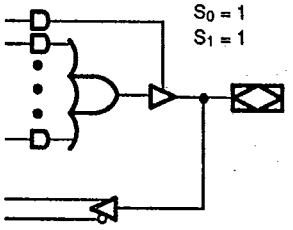


Figure 3d. Combinatorial/Active High

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## Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

## Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit $S_0$ in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

## Preset/Reset

For initialization, the PAL22V10 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

## Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL22V10 will depend on the programmed output polarity. The $V_{CC}$ rise must be monotonic and the reset delay time is 1–10 µs maximum.

## Register Preload

The register on the PAL22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

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## Security Fuse

After programming and verification, a PAL22V10 design can be secured by programming the security fuse or EE bit. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed, and preload will be disabled.

For the CMOS PALCE22V10, a floating gate is used as the security bit. The bit can only be erased in conjunction with erasure of the entire pattern.

## Quality and Testability

The PAL22V10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

The erasability of the CMOS PALCE22V10 allows direct testing of the device array to guarantee 100% programming and functional yields.

## Technology

The bipolar PAL22V10 is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for reliable operation. The PAL22V10-10 uses TiW fuses.

The CMOS PALCE22V10 is fabricated with AMD's advanced EE CMOS process. The array connections are formed by electrically-erasable floating gates similar to those found in EEPROMs.

## Programming and Erasing

The PAL22V10 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

The CMOS PALCE22V10 may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

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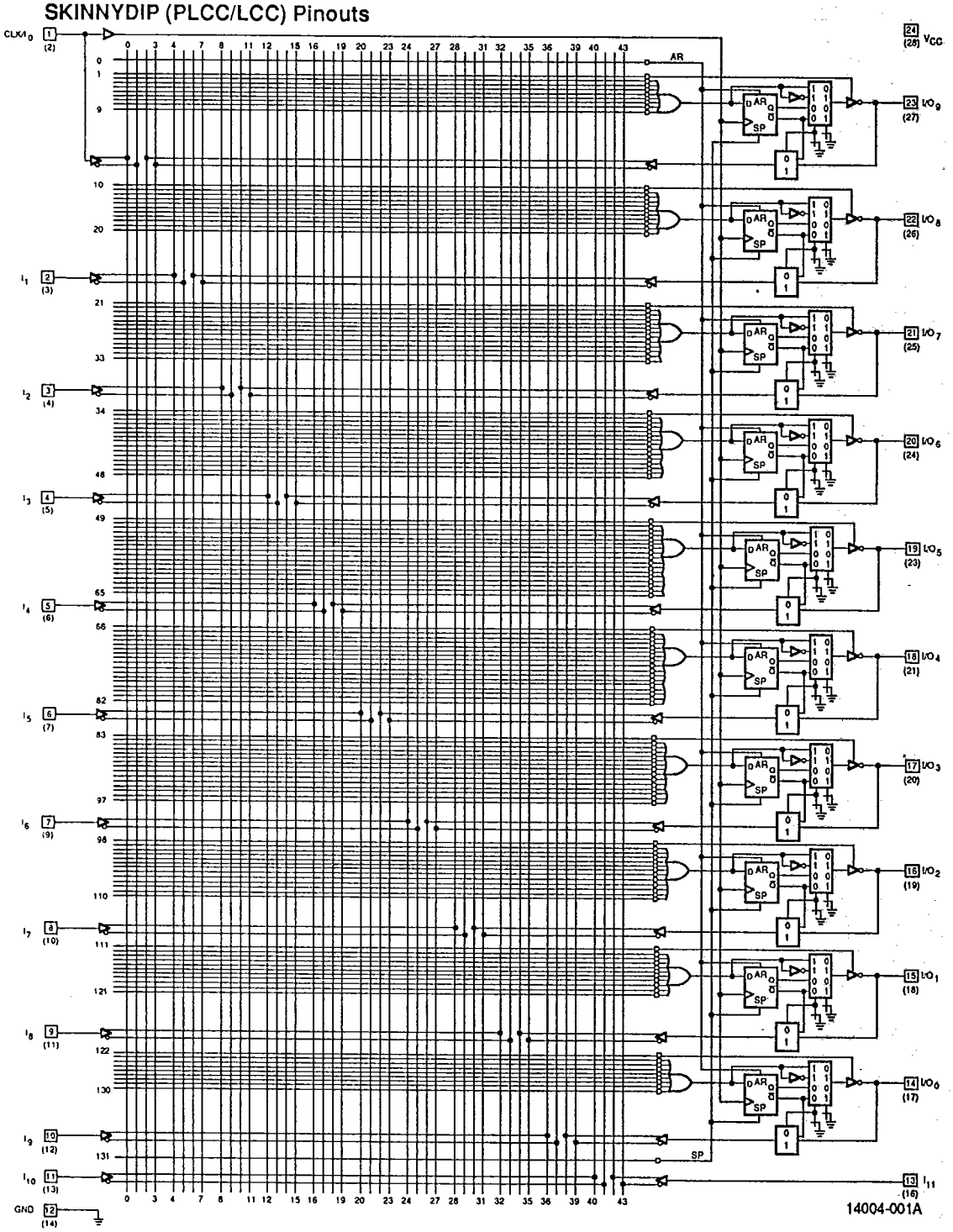
## LOGIC DIAGRAM
## SKINNYDIP (PLCC/LCC) Pinouts

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature with Power Applied | −55°C to +125°C |
| Supply Voltage with Respect to Ground | −0.5 V to +7.0 V |
| DC Input Voltage (-10) | −1.2 V to $V_{CC}$ + 0.5 V |
| DC Input Voltage (-15) | −0.5 V to $V_{CC}$ + 0.5 V |
| DC Input Current (-15) | −30 mA to + 5 mA |
| DC Output or I/O Pin Voltage | −0.5 V to $V_{CC}$ + 0.5 V |
| Static Discharge Voltage | 2001 V |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

| | |
|---|---|
| Ambient Temperature ($T_A$) Operating in Free Air | 0°C to +75°C |
| Supply Voltage ($V_{CC}$) with Respect to Ground | +4.75 V to +5.25 V |

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −3.2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min. | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 16 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min. | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −18 mA, $V_{CC}$ = Min. | | −1.2 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.7 V, $V_{CC}$ = Max. (Note 2) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max. (Note 2) | | −100 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max. | | 1 | mA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.7 V, $V_{CC}$ = Max. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max. (Note 3) | −30 | −90 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA) $V_{CC}$ = Max. | | 180 | mA |

**Notes:**

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | | Test Conditions | | -10 Typ. | -15 Typ. | Unit |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | Pins 1, 13 | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V | 6 | 9 | pF |
| | | Others | | $T_A$ = 25°C | | 6 | |
| $C_{OUT}$ | Output Capacitance | | $V_{OUT}$ = 2.0 V | f = 1 MHz | 8 | 9 | |

**Note:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

**PRELIMINARY**

| Parameter Symbol | Parameter Description | | | -10 Min. (Note 3) | -10 Max. | -15 Min. | -15 Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 3 | 10 | | 15 | ns |
| $t_S$ | Setup Time from Input, Feedback or SP to Clock | | | 8 | | 10 | | ns |
| $t_H$ | Hold Time | | | 0 | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | 3 | 6 | | 10 | ns |
| $t_{CF}$ | Clock to Feedback (Note 4) | | | | 2.5 | | 2.5 | ns |
| $t_{AR}$ | Asynchronous Reset to Registered Output | | | | 15 | | 20 | ns |
| $t_{ARW}$ | Asynchronous Reset Width | | | 10 | | 15 | | ns |
| $t_{ARR}$ | Asynchronous Reset Recovery Time | | | 8 | | 10 | | ns |
| $t_{SPR}$ | Synchronous Preset Recovery Time | | | 8 | | 10 | | ns |
| $t_{WL}$ | Clock Width | LOW | | 5 | | 6 | | ns |
| $t_{WH}$ | | HIGH | | 5 | | 6 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 5) | External Feedback | $1/(t_S + t_{CO})$ | 71 | | 50 | | MHz |
| | | Internal Feedback | $1/(t_S + t_{CF})$ | 95 | | 80 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | 100 | | 83 | | MHz |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | 3 | 10 | | 15 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | 3 | 10 | | 15 | ns |

**Notes:**

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured $f_{MAX}$ internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Supply Voltage with Respect to Ground | −0.5 V to +7.0 V |
| DC Input Voltage (-15) | −1.2 V to +7.0 V |
| DC Input Voltage (-20) | −0.5 V to +5.5 V |
| DC Output or I/O Pin Voltage | −0.5 V to +7.0 V |
| DC Input Current (-20) | −30 mA to +5 mA |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.*

## OPERATING RANGES

**Military (M) Devices (Note 1)**

| | |
|---|---|
| Ambient Temperature ($T_A$) Operating in Free Air | −55°C Min. |
| Operating Case ($T_C$) Temperature | 125°C Max. |
| Supply Voltage ($V_{CC}$) with Respect to Ground | +4.50 V to +5.50 V |

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

**Note:**

1. Military products are tested at $T_C$ = +25°C, +125°C, and −55°C, per MIL-STD-883.

## DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min. | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 12 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min. | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 3) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −18 mA, $V_{CC}$ = Min. | | −1.2 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.7 V, $V_{CC}$ = Max. (Note 4) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max. (Note 4) | | −100 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max. | | 1 | mA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.7 V, $V_{CC}$ = Max. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | −100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max. (Note 5) | −30 | −90 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA) $V_{CC}$ = Max. | | 200 | mA |

**Notes:**

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. $V_{IL}$ and $V_{IH}$ are input conditions of output tests and are not themselves directly tested. $V_{IL}$ and $V_{IH}$ are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | | Test Conditions | | -15 Typ. | -20 Typ. | Unit |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | Pins 1, 13 | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V | 6 | 9 | pF |
| | | Others | | $T_A$ = 25°C | | 6 | |
| $C_{OUT}$ | Output Capacitance | | $V_{OUT}$ = 2.0 V | f = 1 MHz | 8 | 9 | |

**Note:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

**PRELIMINARY**

| Parameter Symbol | Parameter Description | | | -15 Min. | -15 Max. | -20 Min. | -20 Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | | 15 | | 20 | ns |
| $t_S$ | Setup Time from Input, or Feedback to Clock | | | 10 | | 17 | | ns |
| $t_H$ | Hold Time | | | 0 | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | | 10 | | 15 | ns |
| $t_{CF}$ | Clock to Feedback (Note 3 and 4) | | | | 2.5 | | 13 | ns |
| $t_{AR}$ | Asynchronous Reset to Registered Output | | | | 20 | | 25 | ns |
| $t_{ARW}$ | Asynchronous Reset Width (Note 5) | | | 15 | | 20 | | ns |
| $t_{ARR}$ | Asynchronous Reset Recovery Time (Note 5) | | | 10 | | 20 | | ns |
| $t_{SPR}$ | Synchronous Preset Recovery Time (Note 4) | | | 10 | | 20 | | ns |
| $t_{WL}$ | Clock Width | LOW | | 6 | | 15 | | ns |
| $t_{WH}$ | | HIGH | | 6 | | 15 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 6) | External Feedback | $1/(t_S + t_{CO})$ | 50 | | 31.2 | | MHz |
| | | Internal Feedback | $1/(t_S + t_{CF})$ | 80 | | 33.3 | | MHz |
| $t_{EA}$ | Input to Output Enable Using Product Term Control (Note 4) | | | | 15 | | 20 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control (Note 4) | | | | 15 | | 20 | ns |

**Notes:**

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Calculated from measured $f_{MAX}$ internal.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.
5. $t_{ARW}$ and $t_{ARR}$ are not directly tested, but are guaranteed by the testing of $t_S$ and $t_{AR}$.
6. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Ambient Temperature with Power Applied | –55°C to +125°C |
| Supply Voltage with Respect to Ground | –0.5 V to +7.0 V |
| DC Input Voltage | –0.5 V to +5.5 V |
| DC Input Current | –30 mA to +5 mA |
| DC Output or I/O Pin Voltage | –0.5 V to $V_{CC}$ Max. |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

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**Commercial (C) Devices**

| | |
|---|---|
| Ambient Temperature ($T_A$) Operating in Free Air | 0°C to +75°C |
| Supply Voltage ($V_{CC}$) with Respect to Ground | +4.75 V to +5.25 V |

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –3.2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min. | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 16 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min. | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = –18 mA, $V_{CC}$ = Min. | | –1.2 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.7 V, $V_{CC}$ = Max. (Note 2) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max. (Note 2) | | –100 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max. | | 1 | mA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.7 V, $V_{CC}$ = Max. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | –100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max. (Note 3) | –30 | –90 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA) $V_{CC}$ = Max. | | 180 | mA |

**Notes:**

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

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## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | | Test Conditions | | Typ. | Unit |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | Pins 1, 13 | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V | 11 | pF |
| | | Others | | $T_A$ = 25°C | 6 | |
| $C_{OUT}$ | Output Capacitance | | $V_{OUT}$ = 2.0 V | f = 1 MHz | 9 | |

**Note:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | A | | Std | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | | 25 | | 35 | ns |
| $t_S$ | Setup Time from Input, Feedback or SP to Clock | | | 20 | | 30 | | ns |
| $t_H$ | Hold Time | | | 0 | | 0 | | ns |
| $t_{CO}$ | Clock to Output or Feedback | | | | 15 | | 25 | ns |
| $t_{AR}$ | Asynchronous Reset to Registered Output | | | | 30 | | 40 | ns |
| $t_{ARW}$ | Asynchronous Reset Width | | | 25 | | 35 | | ns |
| $t_{ARR}$ | Asynchronous Reset Recovery Time | | | 25 | | 35 | | ns |
| $t_{SPR}$ | Synchronous Preset Recovery Time | | | 20 | | 30 | | ns |
| $t_{WL}$ | Clock Width | LOW | | 15 | | 25 | | ns |
| $t_{WH}$ | | HIGH | | 15 | | 25 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 3) | External Feedback | $1/(t_S + t_{CO})$ | 28.5 | | 18 | | MHz |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | | 25 | | 35 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | | 25 | | 35 | ns |

**Notes:**

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Supply Voltage with Respect to Ground | –0.5 V to +7.0 V |
| DC Input Voltage | –0.5 V to +5.5 V |
| DC Output or I/O Pin Voltage | –0.5 V to $V_{CC}$ Max. |
| DC Input Current | –30 mA to +5 mA |
| Output Sink Current | 100 mA (Note 6) |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.*

## OPERATING RANGES

**Military (M) Devices (Note 1)**

| | |
|---|---|
| Ambient Temperature ($T_A$) Operating in Free Air | –55°C Min. |
| Operating Case ($T_C$) Temperature | +125°C Max. |
| Supply Voltage ($V_{CC}$) with Respect to Ground | +4.50 V to +5.50 V |

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

**Note:**

1. Military products are tested at $T_C$ = +25°C, +125°C, and –55°C per MIL-STD-883.

## DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –2 mA $V_{IN} = V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min. | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 12 mA $V_{IN} = V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min. | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 3) | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = –18 mA, $V_{CC}$ = Min. | | –1.2 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = 2.7 V, $V_{CC}$ = Max. (Note 4) | | 25 | µA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4 V, $V_{CC}$ = Max. (Note 4) | | –100 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max. | | 1 | mA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 2.7 V, $V_{CC}$ = Max. $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 4) | | 100 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0.4 V, $V_{CC}$ = Max. $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 4) | | –100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max. (Note 5) | –30 | –90 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA) $V_{CC}$ = Max. | | 180 | mA |

**Notes:**

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. $V_{IL}$ and $V_{IH}$ are input conditions of output tests and are not themselves directly tested. $V_{IL}$ and $V_{IH}$ are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
6. Not more than one output should sink 100 mA at a time. Duration should not exceed one second.

## CAPACITANCE (Note 1)

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| Parameter Symbol | Parameter Description | | Test Conditions | | Typ. | Unit |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | Pins 1, 13 | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V | 11 | pF |
| | | Others | | $T_A$ = 25°C | 6 | |
| $C_{OUT}$ | Output Capacitance | | $V_{OUT}$ = 2.0 V | f = 1 MHz | 9 | |

**Note:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | A | | Std. | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | | 30 | | 40 | ns |
| $t_S$ | Setup Time from Input, or Feedback to Clock | | | 25 | | 35 | | ns |
| $t_H$ | Hold Time | | | 0 | | 0 | | ns |
| $t_{CO}$ | Clock to Output or Feedback | | | | 20 | | 25 | ns |
| $t_{AR}$ | Asynchronous Reset to Registered Output | | | | 35 | | 45 | ns |
| $t_{ARW}$ | Asynchronous Reset Width (Note 3) | | | 30 | | 40 | | ns |
| $t_{ARR}$ | Asynchronous Reset Recovery Time (Note 3) | | | 30 | | 40 | | ns |
| $t_{WL}$ | Clock Width | LOW | | 20 | | 30 | | ns |
| $t_{WH}$ | | HIGH | | 20 | | 30 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 4) | External Feedback | $1/(t_S + t_{CO})$ | 22 | | 16.5 | | MHz |
| $t_{EA}$ | Input to Output Enable Using Product Term Control (Note 5) | | | | 30 | | 40 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control (Note 5) | | | | 30 | | 40 | ns |

**Notes:**

2. See Switching Test Circuit for test conditions.
3. $t_{ARW}$ and $t_{ARR}$ are not directly tested, but are guaranteed by the testing of $t_S$ and $t_{AR}$.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature with Power Applied | −55°C to +125°C |
| Supply Voltage with Respect to Ground | −0.5 V to +7.0 V |
| DC Input Voltage (Except Pin 5) | −0.5 V to $V_{CC}$ + 0.5 V |
| DC Input Voltage (Pin 5) | −0.6 V to +11.0 V |
| DC Output or I/O Pin Voltage | −0.5 V to $V_{CC}$ + 0.5 V |
| Static Discharge Voltage | 2001 V |
| Latchup Current ($T_A$ = 0°C to +75°C) | 100 mA |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

| | |
|---|---|
| Ambient Temperature ($T_A$) Operating in Free Air | 0°C to +75°C |
| Supply Voltage ($V_{CC}$) with Respect to Ground (Except H-25) | +4.75 V to +5.25 V |
| Supply Voltage ($V_{CC}$) with Respect to Ground (H-25) | +4.5 V to +5.5 V |

*Operating Ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −3.2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min. | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 16 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min. | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max. (Note 2) | | | 10 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0 V, $V_{CC}$ = Max. (Note 2) | | | −10 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 5.5 V, $V_{CC}$ = Max., $V_{IN}$ = $V_{IL}$ or $V_{IH}$ (Note 2) | | | 10 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0 V, $V_{CC}$ = Max. $V_{IN}$ = $V_{IL}$ or $V_{IH}$ (Note 2) | | | −10 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max. (Note 3) | | −30 | −150 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA), $V_{CC}$ = Max. | H | | 90 | mA |
| | | | Q | | 55 | |

**Notes:**

1. These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).
3. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions | | Typ. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V, $T_A$ = 25°C, f = 1 MHz | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | | 8 | |

**Note:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | -15 Min. | -15 Max. | -25 Min. | -25 Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | | 15 | | 25 | ns |
| $t_S$ | Setup Time from Input, Feedback or SP to Clock | | | 10 | | 15 | | ns |
| $t_H$ | Hold Time | | | 0 | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | | 10 | | 15 | ns |
| $t_{CF}$ | Clock to Feedback (Note 3) | | | | 7 | | 13 | ns |
| $t_{AR}$ | Asynchronous Reset to Registered Output | | | | 20 | | 25 | ns |
| $t_{ARW}$ | Asynchronous Reset Width | | | 15 | | 25 | | ns |
| $t_{ARR}$ | Asynchronous Reset Recovery Time | | | 10 | | 25 | | ns |
| $t_{SPR}$ | Synchronous Preset Recovery Time | | | 10 | | 25 | | ns |
| $t_{WL}$ | Clock Width | LOW | | 8 | | 13 | | ns |
| $t_{WH}$ | | HIGH | | 8 | | 13 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 4) | External Feedback | $1/(t_S + t_{CO})$ | 50 | | 33.3 | | MHz |
| | | Internal Feedback | $1/(t_S + t_{CF})$ | 58.8 | | 35.7 | | MHz |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | | 15 | | 25 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | | 15 | | 25 | ns |

**Notes:**

2. See Switching Test Circuit for test conditions.
3. Calculated from measured $f_{MAX}$ internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Ambient Temperature with Power Applied | –55°C to +125°C |
| Supply Voltage with Respect to Ground | –0.5 V to +7.0 V |
| DC Input Voltage (Except Pin 5) | –0.5 V to $V_{CC}$ + 0.5 V |
| DC Input Voltage (Pin 5) | –0.6 V to +11.0 V |
| DC Output or I/O Pin Voltage | –0.5 V to $V_{CC}$ + 0.5 V |
| Static Discharge Voltage | 2001 V |
| Latchup Current ($T_A$ = –55°C to +125°C) | 100 mA |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.*

## OPERATING RANGES

**Military (M) Devices (Note 1)**

| | |
|---|---|
| Operating Case Temperature ($T_C$) | –55°C to +125°C |
| Supply Voltage ($V_{CC}$) with Respect to Ground | +4.5 V to +5.5 V |

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

**Note:**

1. Military products are tested at $T_C$ = +25°C, +125°C and –55°C, per MIL-STD-883.

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## DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –2.0 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min. | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 12 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min. | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 3) | | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max. (Note 4) | | 10 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0 V, $V_{CC}$ = Max. (Note 4) | | –10 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 5.5 V, $V_{CC}$ = Max. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | 10 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0 V, $V_{CC}$ = Max. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 4) | | –10 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V $V_{CC}$ = Max. (Note 5) | –30 | –150 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA), $V_{CC}$ = Max. | | 100 | mA |

**Notes:**

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.
3. $V_{IL}$ and $V_{IH}$ are input conditions of output tests and are not themselves directly tested. $V_{IL}$ and $V_{IH}$ are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where $I_{SC}$ may be affected.

## CAPACITANCE (Note 1)

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| Parameter Symbol | Parameter Description | Test Conditions | | Typ. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V, $T_A$ = 25°C, f = 1 MHz | 8 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | | 9 | |

**Note:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | -25 Min. | -25 Max. | -30 Min. | -30 Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | | 25 | | 30 | ns |
| $t_S$ | Setup Time from Input, Feedback or SP to Clock | | | 20 | | 20 | | ns |
| $t_H$ | Hold Time (Note 4) | | | 0 | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | | 20 | | 20 | ns |
| $t_{CF}$ | Clock to Feedback (Note 3) | | | | 18 | | 18 | ns |
| $t_{AR}$ | Asynchronous Reset to Registered Output | | | | 30 | | 35 | ns |
| $t_{ARW}$ | Asynchronous Reset Width (Note 4) | | | 25 | | 30 | | ns |
| $t_{ARR}$ | Asynchronous Reset Recovery Time (Note 4) | | | 25 | | 30 | | ns |
| $t_{SPR}$ | Synchronous Preset Recovery Time | | | 25 | | 30 | | ns |
| $t_{WL}$ | Clock Width | LOW | | 15 | | 15 | | ns |
| $t_{WH}$ | | HIGH | | 15 | | 15 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 5) | External Feedback | $1/(t_S + t_{CO})$ | 25 | | 25 | | MHz |
| | | Internal Feedback | $1/(t_S + t_{CF})$ | 26 | | 26 | | MHz |
| $t_{EA}$ | Input to Output Enable Using Product Term Control (Note 4) | | | | 25 | | 30 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control (Note 4) | | | | 25 | | 30 | ns |

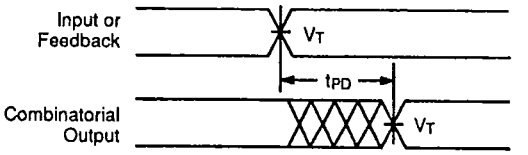
**Notes:**

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 7, 8, 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Calculated from measured $f_{MAX}$ internal.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

## SWITCHING WAVEFORMS

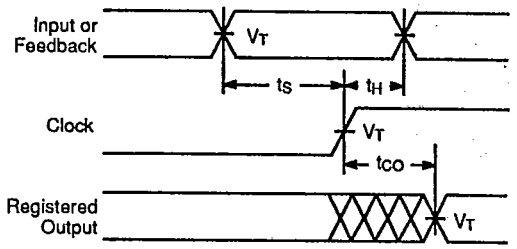
T-46-19-07

T-46-19-13



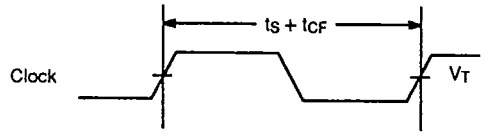

12015-010A

**Combinatorial Output**



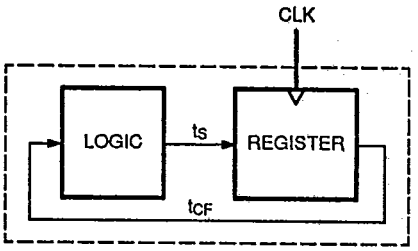

12015-012A

**Registered Output**

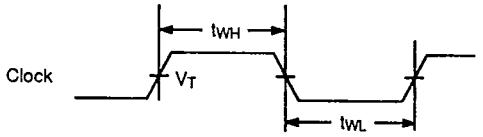



12149-025A

**Clock to Feedback ($f_{MAX}$ Internal)**
**See Path at Right**

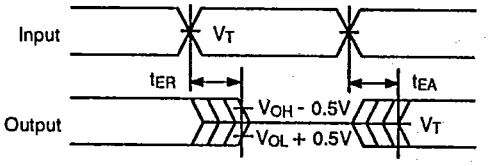



12015-021A



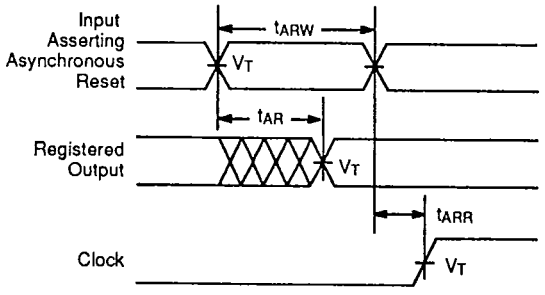

12015-011A

**Clock Width**



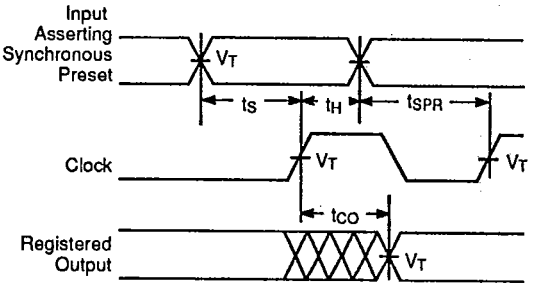

12015-013A

**Input to Output Disable/Enable**




13003-006A

**Asynchronous Reset**




13003-007A

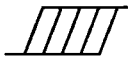
**Synchronous Preset**

**Notes:**

1. $V_T$ = 1.5 V.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical. (2–4 ns for 22V10-10)

## KEY TO SWITCHING WAVEFORMS

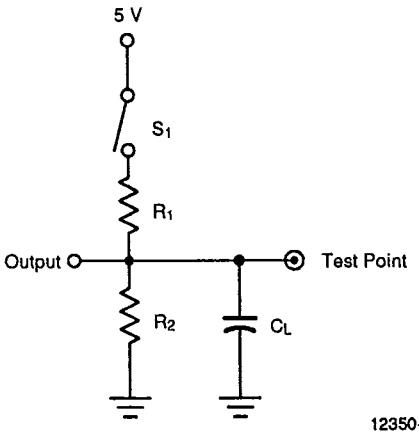
T-46-19-07 T-46-19-13

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| ——— | Must be Steady | Will be Steady |
| ——— | | |
|  | May Change from H to L | Will be Changing from H to L |
|  | May Change from L to H | Will be Changing from L to H |
|  | Don't Care; Any Change Permitted | Changing, State Unknown |
|  | Does Not Apply | Center Line is High-Impedance "Off" State |

KS000010-PAL

2

## SWITCHING TEST CIRCUIT



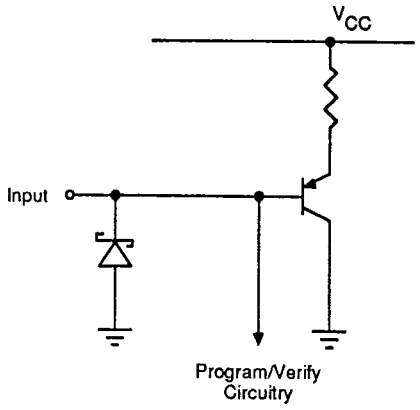

12350-019A

| Specification | $S_1$ | $C_L$ | Commercial | | Military | | Measured Output Value |
|---|---|---|---|---|---|---|---|
| | | | $R_1$ | $R_2$ | $R_1$ | $R_2$ | |
| $t_{PD}$, $t_{CO}$, $t_{CF}$ | Closed | 50 pF | 300 Ω | 390 Ω | 390 Ω CMOS: 338 Ω | 750 Ω CMOS: 248 Ω | 1.5 V |
| $t_{EA}$ | Z → H: Open<br>Z → L: Closed | | | | | | 1.5 V |
| $t_{ER}$ | H → Z: Open<br>L → Z: Closed | 5 pF | | | | | H → Z: $V_{OH}$ – 0.5 V<br>L → Z: $V_{OL}$ + 0.5 V |

## INPUT/OUTPUT EQUIVALENT SCHEMATICS
**Bipolar Devices Only**

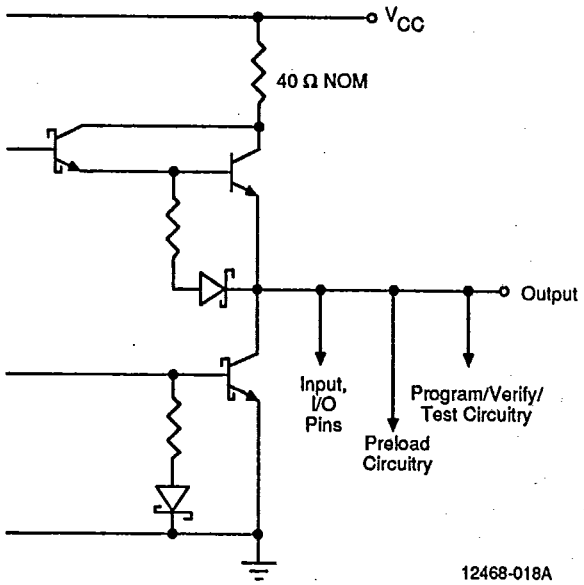
T-46-19-07 T-46-19-13

**Typical Input**




12468-017A

**Typical Output**




12468-018A

## ENDURANCE CHARACTERISTICS

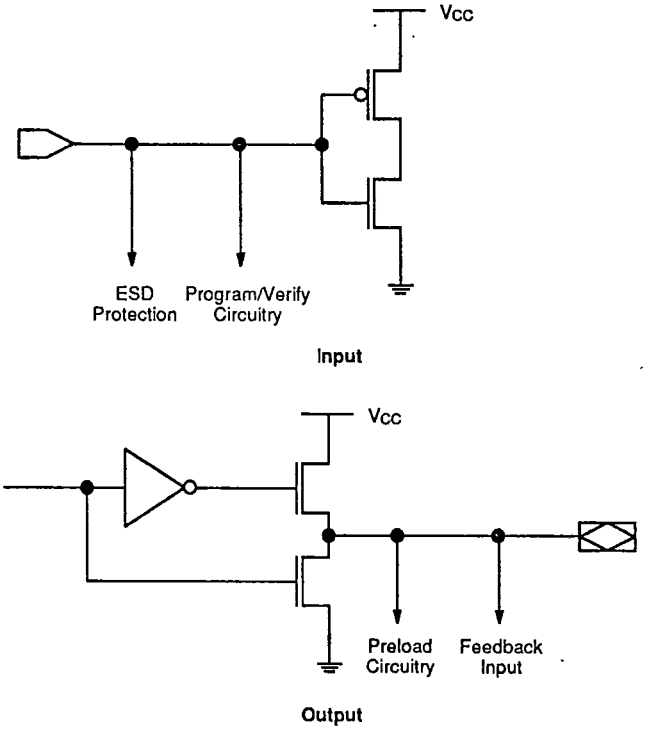
The PALCE22V10 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

### Endurance Characteristics

| Symbol | Parameter | Min. | Units | Test Conditions |
|---|---|---|---|---|
| $t_{DR}$ | Min. Pattern Data Retention Time | 10 | Years | Max. Storage Temperature |
| | | 20 | Years | Max. Operating Temperature (Military) |
| N | Min. Reprogramming Cycles | 100 | Cycles | Normal Programming Conditions |

## INPUT/OUTPUT EQUIVALENT SCHEMATICS

### CMOS Devices Only




12197-013A

T-46-19-07 T-46-19-13

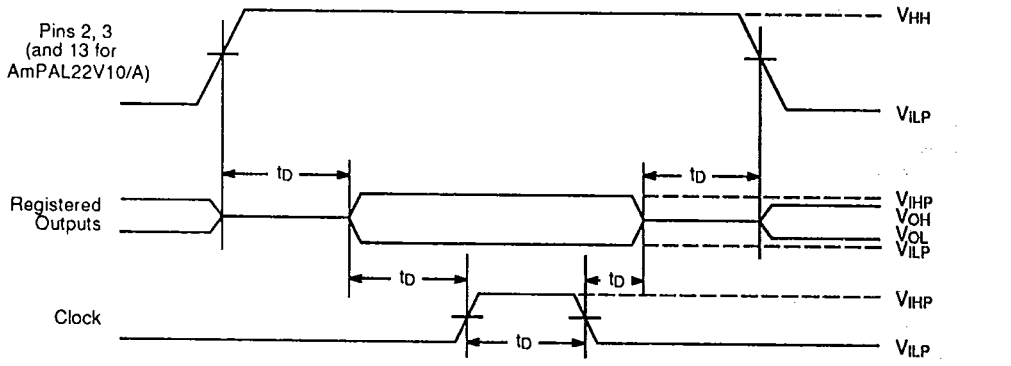
## OUTPUT REGISTER PRELOAD

### Bipolar Devices Only

The preload function allows the registers to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise $V_{CC}$ to 5.0 V ± 0.5 V.
2. Set pins 2 and 3 (and 13 for AmPAL22V10/A) to $V_{HH}$ to disable outputs and enable preload.
3. Apply the desired value ($V_{ILP}/V_{IHP}$) to all registered output pins. Leave combinatorial output pins floating.
4. Clock pin 1 from $V_{ILP}$ to $V_{IHP}$.
5. Remove $V_{ILP}/V_{IHP}$ from all registered output pins.
6. Lower pins 2 and 3 to $V_{ILP}$.
7. Enable the output registers according to the programmed pattern.
8. Verify $V_{OL}/V_{OH}$ at all registered output pins. Note that the output pin signal will depend on the output polarity.

| Parameter Symbol | Parameter Description | Min. | Rec. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{HH}$ | Super-level input voltage | 10 | 11 | 12 | V |
| $V_{ILP}$ | Low-level input voltage | 0 | 0 | 0.5 | V |
| $V_{IHP}$ | High-level input voltage | 2.4 | 5.0 | 5.5 | V |
| $t_D$ | Delay time | 100 | 200 | 1000 | ns |




14004-002A

Output Register Preload Waveform

## OUTPUT REGISTER PRELOAD

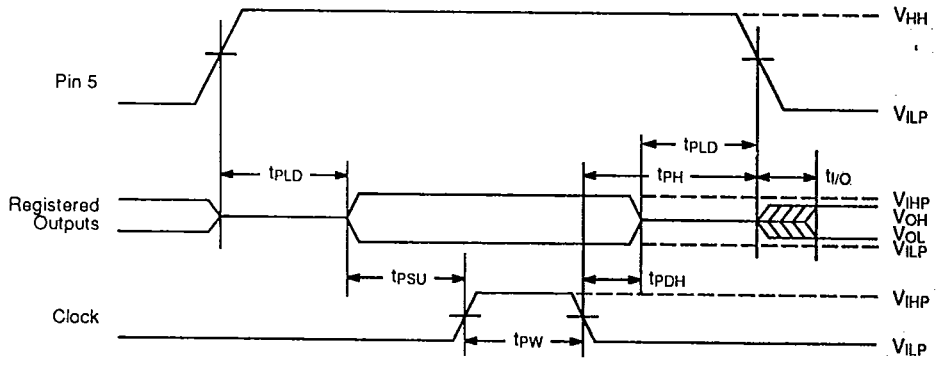
### CMOS Devices Only

The preload function allows the registers to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise $V_{CC}$ to 5.0 V ± 0.5 V.
2. Set pin 5 to $V_{HH}$ to disable outputs and enable preload.
3. Apply the desired value ($V_{ILP}/V_{IHP}$) to all registered output pins. Leave combinatorial output pins floating.
4. Clock pin 1 from $V_{ILP}$ to $V_{IHP}$.
5. Remove $V_{ILP}/V_{IHP}$ from all registered output pins.
6. Lower pin 5 to $V_{ILP}$.
7. Enable the output registers according to the programmed pattern.
8. Verify $V_{OL}/V_{OH}$ at all registered output pins. Note that the output pin signal will depend on the output polarity.

| Parameter Symbol | Parameter Description | Min. | Rec. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{HH}$ | Super-level input voltage | 9.5 | 10 | 10.5 | V |
| $V_{ILP}$ | Low-level input voltage | 0 | 0 | 0.5 | V |
| $V_{IHP}$ | High-level input voltage | 3.0 | 4.0 | $V_{CC}$ | V |
| $t_{PLD}$ | Setup and Hold Data to Preload (Pin 5) | 50 | 50 | | µs |
| $t_{PSU}$ | Data Setup Prior to Applying Preload Latch Pulse | 1.0 | 1.0* | | µs |
| $t_{PDH}$ | Data Hold After Latch Pulse | 1.0 | 1.0* | | µs |
| $t_{PH}$ | Mode Hold After Latch Pulse | 1.0 | 1.0* | | µs |
| $t_{PW}$ | Latch Pulse Width | 1.0 | 1.0* | | µs |
| $t_{IO}$ | I/O Valid After Pin 5 Drops from $V_{HH}$ to TTL Levels | | | 100 | µs |
| $\frac{dVr}{dt}$ | $V_{HH}$ Rising Slew Rate (Pin 5) | 10 | | 100 | V/µs |
| $\frac{dVf}{dt}$ | $V_{HH}$ Falling Slew Rate (Pin 5) | | 2.0 | 3.0 | V/µs |

* Recommended value is as close to 1.0 µs + tolerance as practical, but not less than 1.0 µs.




14004-003A

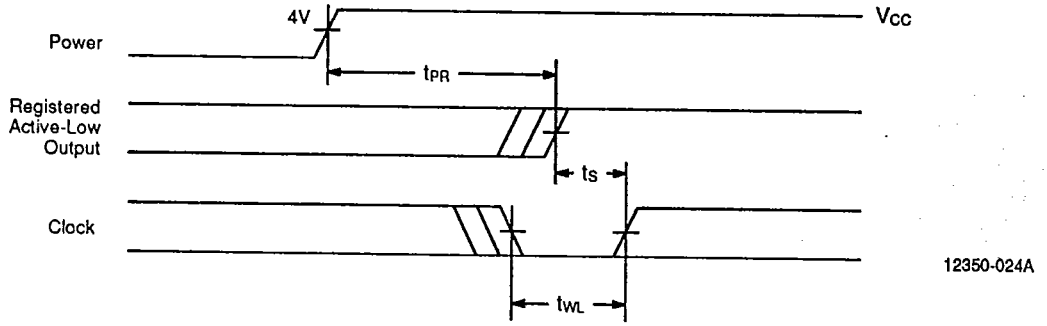
Output Register Preload Waveform

## POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways $V_{CC}$ can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The $V_{CC}$ rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

| Parameter Symbol | Parameter Description | | Max. | Unit |
|---|---|---|---|---|
| $t_{PR}$ | Power-up Reset Time | Bipolar | 1 | µs |
| | | CMOS | 10 | |
| $t_S$ | Input or Feedback Setup Time | | See Switching Characteristics | |
| $t_{WL}$ | Clock Width LOW | | | |




**Power-Up Reset Waveform**