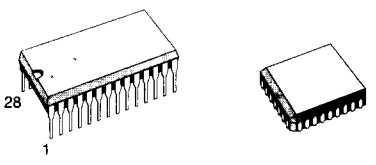
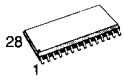
PARALLEL ACCESS CMOS 64K (8K x 8) EEPROM

- FAST ACCESS TIME: 150, 200ns
- SINGLE SUPPLY VOLTAGE: 5V ± 10%
- LOW POWER CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- FAST WRITE CYCLE:
  - 32 Bytes Page Write Operation
  - Byte Or Page Write Cycle: 5ms
- ENHANCED END OF WRITE DETECTION:
  - Ready/Busy Open Drain Output
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABLITY SINGLE POLYSILICON, CMOS:
  - Endurance > 100,000 Erase/Write Cycles
  - Data Retention > 10 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- ADDRESS AND DATA LATCHED ON-CHIP



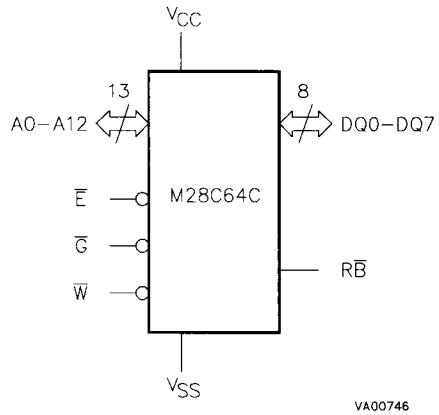
PDIP28

PLCC32



PSO28 (M)
330 mils

Figure 1. Logic Diagram



DESCRIPTION

The M28C64C is an 8K x 8 low power EEPROM fabricated with SGS-THOMSON proprietary single polysilicon CMOS technology. The device offers fast access time (150ns) with low power dissipation and requires a 5V power supply.

Table 1. Signal Names

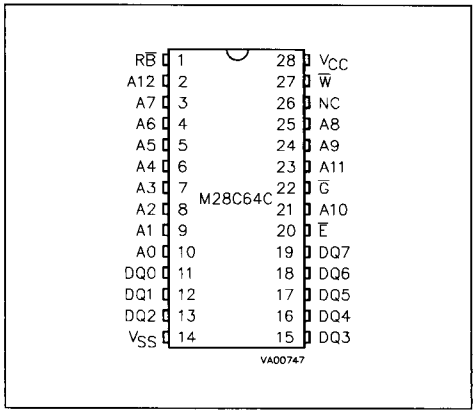
A0 - A12	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$R\overline{B}$	Ready / Busy
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature:	grade 1 grade 6	0 to 70 – 40 to 85	°C
T_{STG}	Storage Temperature Range		– 65 to 150	°C
V_{CC}	Supply Voltage		– 0.3 to 6.5	V
V_{IO}	Input or Output Voltages		– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)		2000	V

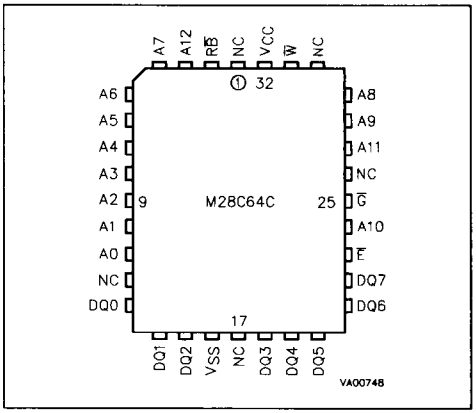
Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2A. DIP Pin Connections



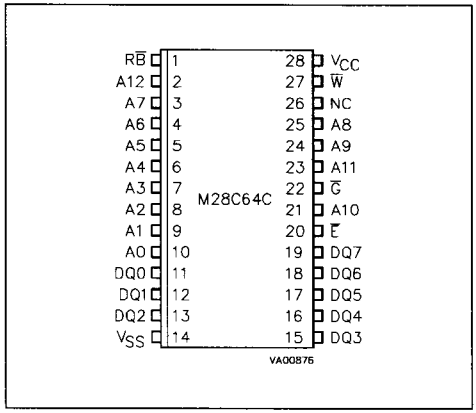
Warning: NC = No Connection

Figure 2B. LCC Pin Connections



Warning: NC = No Connection

Figure 2C. SO Pin Connections



Warning: NC = No Connection

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking with Ready/Busy, Data Polling and Toggle Bit. The M28C64C supports 32 byte page write operation.

PIN DESCRITPION

Addresses (A0-A12). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28C64C through the I/O pins.

Figure 3. Block Diagram

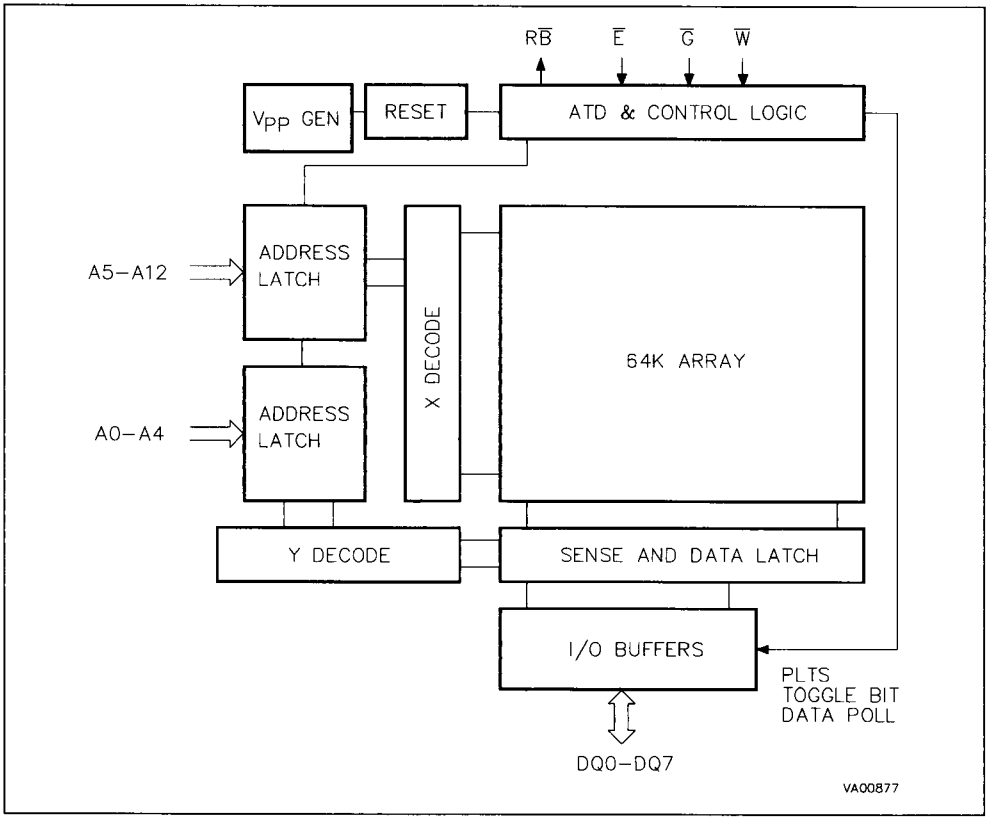


Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	Hi-Z

Note: X = V_{IH} or V_{IL}

PIN DESCRIPTION (cont'd)

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28C64C.

Ready/Busy ($R\overline{B}$). Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle.

OPERATION

Read

The M28C64C is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high. The M28C64C supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion within 5ms.

Page Write

Page write allows up to 32 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A5 - A12 must be the same for all bytes. The page write can be initiated during any byte write operation. Following the first byte write instruction the host may send another address and data up to a maximum of 100µs after the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. If a transition of $\overline{E}$ or $\overline{W}$ is not detected within 100µs, the internal programming cycle will start.

Microcontroller Control Interface

The M28C64C provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the $R\overline{B}$ signal on a separate pin.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
R = Reserved, definition pending
PLTS = Page Load Time Status

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28C64C also offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Input Output Waveforms

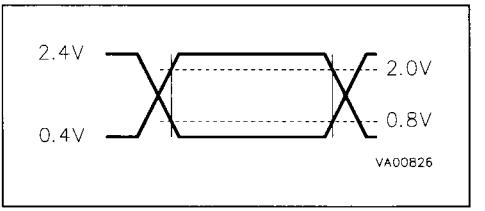


Figure 6. AC Testing Load Circuit

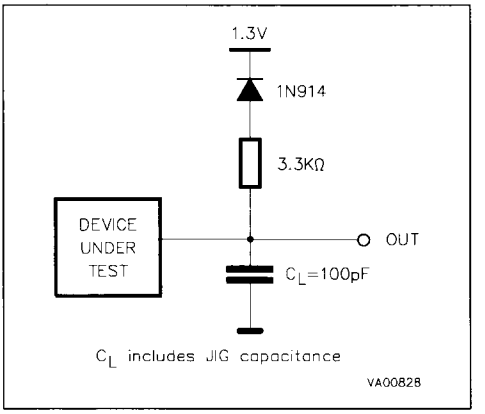


Table 4. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. This parameter is sampled only and not tested 100%.

Table 5. Read Mode DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		2	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} –0.3V		100	µA
V_{IL}	Input Low Voltage		– 0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		V

OPERATION (cont'd)

Page Load Timer Status (DQ5). In the Page Write mode data may be latched by $\overline{E}$ or $\overline{W}$ up to 100µs after the previous byte. Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low. DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

Ready/Busy pin. The $R\overline{B}$ pin provides a signal at its open drain output which is low during the erase/write cycle, but which is relased at the completing of the programming cycle.

Table 6. Read Mode AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C, V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	Test Condition	M28C64C				Unit
				-150		-200		
				min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		75		100	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-z	$\overline{G}$ = V_{IL}	0	50	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Note: 1. Output float is defined as the point where data is no longer driving. The parameter is sampled only and not 100% tested.

Figure 7. Read Mode AC Waveforms

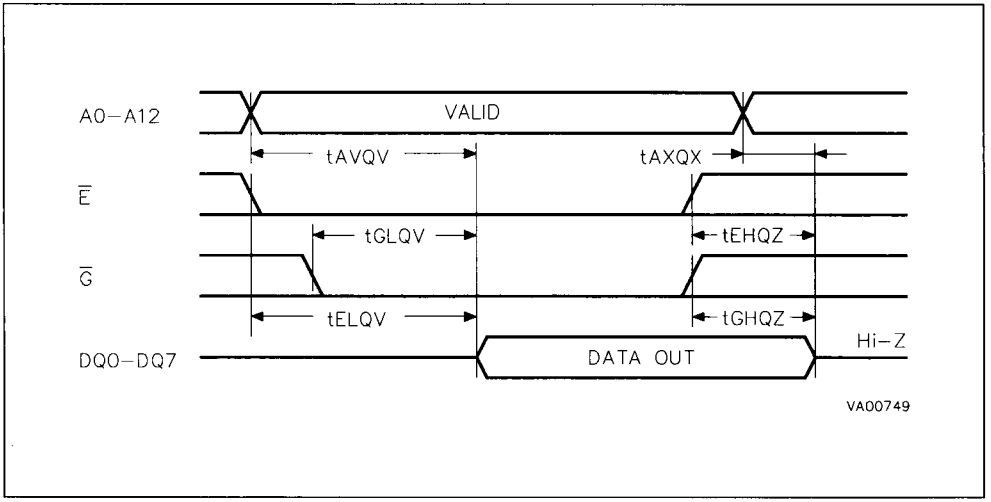


Table 7. Write Mode AC Characteristics
(T_A = 0 to 70 °C or –40 to 85°C, V_{CC} = 5V ±10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E}$ = V_{IL}	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W}$ = V_{IL}	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		150		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		150		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}		1	µs
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		150		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		150		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		200		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time			100	µs
t_{WHRH}	t_{WC}	Write Cycle Time			5	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		50	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		50	ns

Note: 1. With a 3.3kΩ pull-up resistor.

Figure 8. Write Mode AC Waveforms - Write Enable Controlled

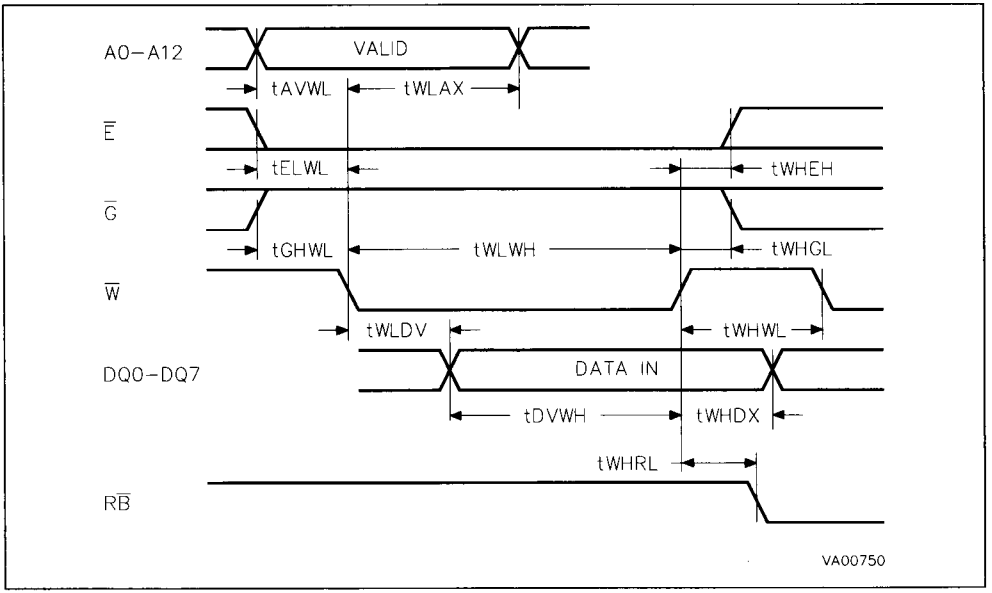


Figure 9. Write Mode AC Waveforms - Chip Enable Controlled

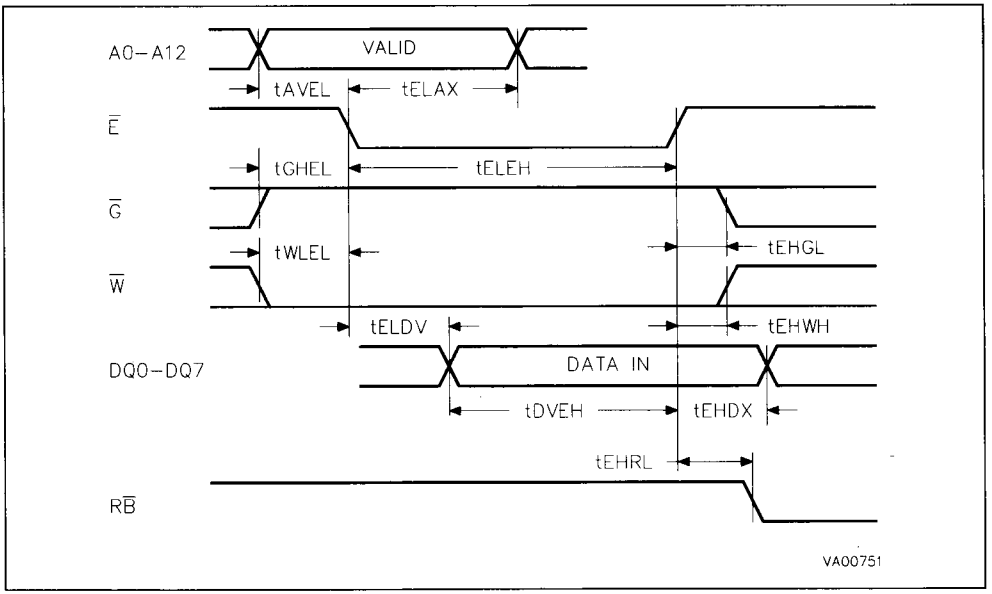


Figure 10. Page Write Mode AC Waveforms

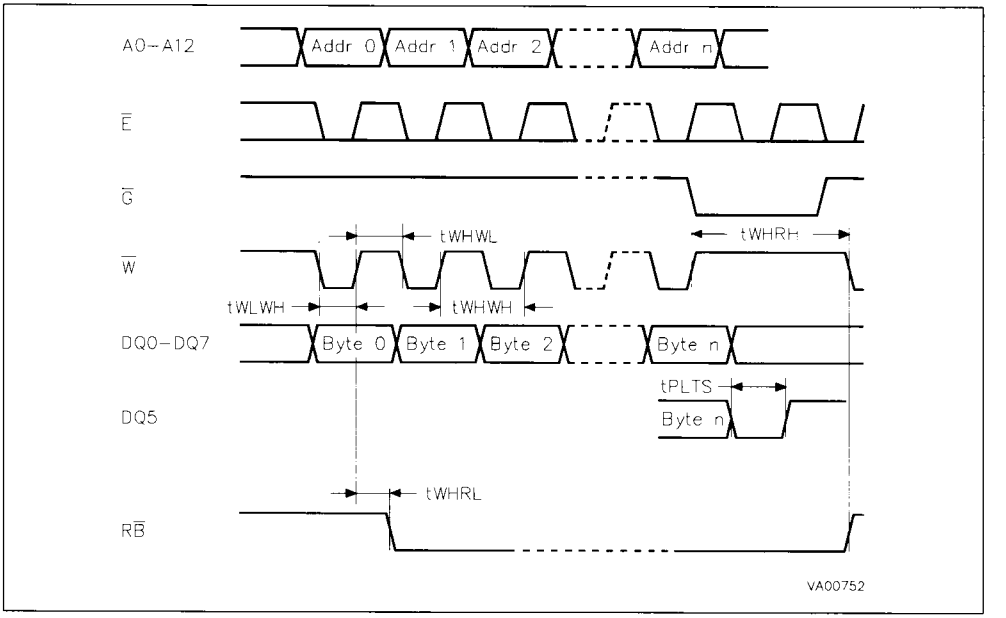


Figure 11. Data Polling Waveforms Sequence

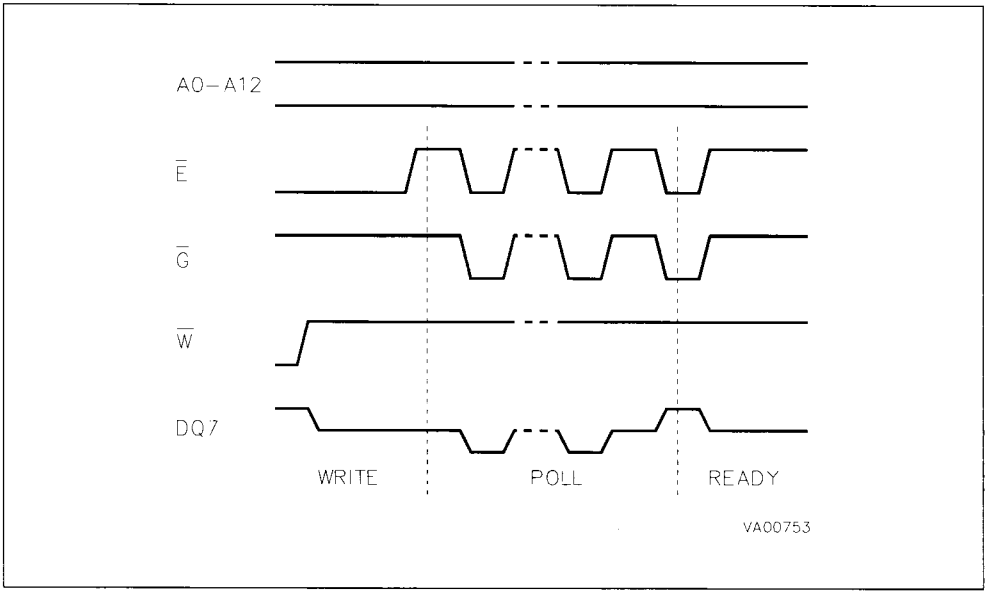
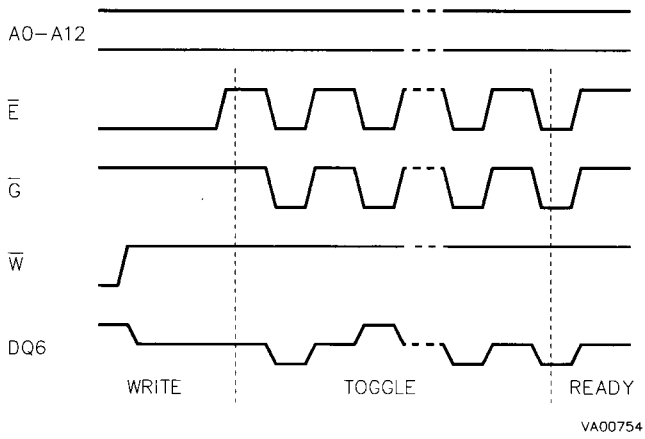


Figure 12. Toggle Bit Waveforms Sequence



ORDERING INFORMATION

Example: M28C64C -150 K 1

Speed		Package		Temperature Range	
-150	150 ns	K	PLCC32	1	0 to 70 °C
-200	200 ns	P	PDIP28	6	–40 to 85 °C
		M	PSO28 330 mils		

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.