



CY7C132/CY7C136 CY7C142/CY7C146

2Kx8 Dual-Port Static RAM

Features

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- 2K x 8 organization
- 0.65-micron CMOS for optimum speed/power
- High-speed access: 15 ns
- Low operating power: $I_{CC} = 110$ mA (max.)
- Fully asynchronous operation
- Automatic power-down
- Master CY7C132/CY7C136 easily expands data bus width to 16 or more bits using slave CY7C142/CY7C146
- BUSY output flag on CY7C132/CY7C136; BUSY input on CY7C142/CY7C146
- INT flag for port-to-port communication (52-pin PLCC/PQFP versions)
- Available in 48-pin DIP (CY7C132/142), 52-pin PLCC and 52-pin TQFP (CY7C136/146)
- Pin-compatible and functionally equivalent to IDT7132/IDT7142

Functional Description

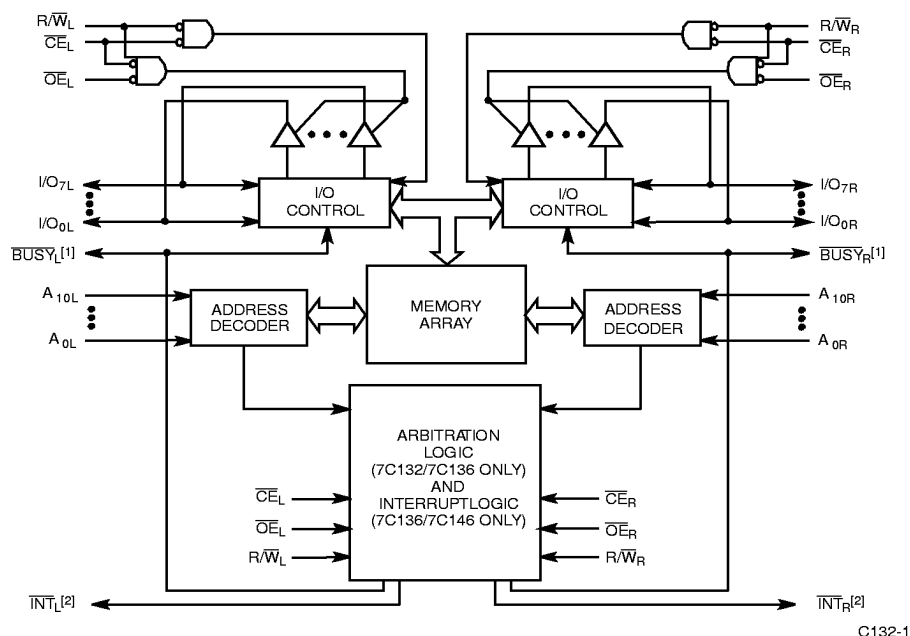
The CY7C132/CY7C136/CY7C142 and CY7C146 are high-speed CMOS 2K by 8 dual-port static RAMs. Two ports are provided to permit independent access to any location in memory. The CY7C132/ CY7C136 can be utilized as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7C142/CY7C146 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable (\overline{CE}), write enable ($\overline{R/W}$), and output enable (\overline{OE}). BUSY flags are provided on each port. In addition, an interrupt flag (INT) is provided on each port of the 52-pin PLCC version. BUSY signals that the port is trying to access the same location currently being accessed by the other port. On the PLCC version, INT is an interrupt flag indicating that data has been placed in a unique location (7FF for the left port and 7FE for the right port).

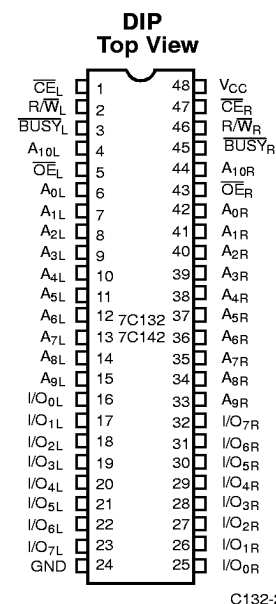
An automatic power-down feature is controlled independently on each port by the chip enable (\overline{CE}) pins.

The CY7C132/CY7C142 are available in 48-pin DIP. The CY7C136/CY7C146 are available in 52-pin PLCC and PQFP.

Logic Block Diagram

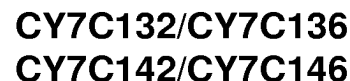


Pin Configuration



Notes:

1. CY7C132/CY7C136 (Master): BUSY is open drain output and requires pull-up resistor. CY7C142/CY7C146 (Slave): BUSY is input.
2. Open drain outputs; pull-up resistor required.





Electrical Characteristics Over the Operating Range^[6]

| Parameter | Description | Test Conditions | 7C136-15 ^[3,4] 7C146-15 | | 7C132-30 ^[3] 7C136-25,30 7C142-30 7C146-25,30 | | 7C132-35,45 7C136-35,45 7C142-35,45 7C146-35,45 | | 7C132-55 7C136-55 7C142-55 7C146-55 | | Unit |
|------------------|---|--|---------------------------------------|------|---|------|--|------|--|------|------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | | 2.4 | | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 4.0 mA | | 0.4 | | 0.4 | | 0.4 | | 0.4 | V |
| | | I _{OL} = 16.0 mA ^[7] | | 0.5 | | 0.5 | | 0.5 | | 0.5 | |
| V _{IH} | Input HIGH Voltage | | 2.2 | | 2.2 | | 2.2 | | 2.2 | | V |
| V _{IL} | Input LOW Voltage | | | 0.8 | | 0.8 | | 0.8 | | 0.8 | V |
| I _{IX} | Input Load Current | GND ≤ V _I ≤ V _{CC} | -5 | +5 | -5 | +5 | -5 | +5 | -5 | +5 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _O ≤ V _{CC} , Output Disabled | -5 | +5 | -5 | +5 | -5 | +5 | -5 | +5 | μA |
| I _{OS} | Output Short Circuit Current ^[8] | V _{CC} = Max., V _{OUT} = GND | | -350 | | -350 | | -350 | | -350 | mA |
| I _{CC} | V _{CC} Operating Supply Current | CE = V _{IL} , Outputs Open, f = f _{MAX} ^[9] | Com'I | 190 | | 170 | | 120 | | 110 | mA |
| | | | Mil | | | | | 170 | | 120 | |
| I _{SB1} | Standby Current Both Ports, TTL Inputs | CE _L and CE _R ≥ V _{IH} , f = f _{MAX} ^[9] | Com'I | 75 | | 65 | | 45 | | 35 | mA |
| | | | Mil | | | | | 65 | | 45 | |
| I _{SB2} | Standby Current One Port, TTL Inputs | CE _L or CE _R ≥ V _{IH} , Active Port Outputs Open, f = f _{MAX} ^[9] | Com'I | 135 | | 115 | | 90 | | 75 | mA |
| | | | Mil | | | | | 115 | | 90 | |
| I _{SB3} | Standby Current Both Ports, CMOS Inputs | Both Ports CE _L and CE _R ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0 | Com'I | 15 | | 15 | | 15 | | 15 | mA |
| | | | Mil | | | | | 15 | | 15 | |
| I _{SB4} | Standby Current One Port, CMOS Inputs | One Port CE _L or CE _R ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, Active Port Outputs Open, f = f _{MAX} ^[9] | Com'I | 125 | | 105 | | 85 | | 70 | mA |
| | | | Mil | | | | | 105 | | 85 | |

Shaded area contains preliminary information.

Capacitance^[10]

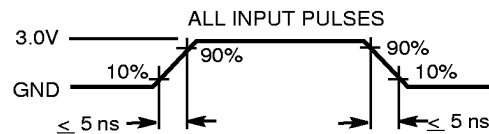
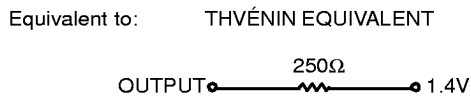
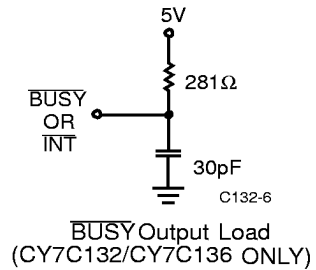
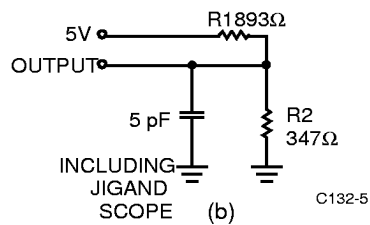
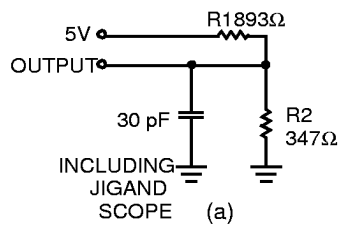
| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|-----------------------------------|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, | 15 | pF |
| C _{OUT} | Output Capacitance | V _{CC} = 5.0V | 10 | pF |

Notes:

6. See the last page of this specification for Group A subgroup testing information.
7. BUSY and INT pins only.
8. Duration of the short circuit should not exceed 30 seconds.
9. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of 1/t_{IC} and using AC Test Waveforms input levels of GND to 3V.
10. This parameter is guaranteed but not tested.



AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range^[6, 11]

| Parameter | Description | 7C136-15 ^[3,4] 7C146-15 | | 7C132-25 ^[3] 7C136-25 7C142-25 7C146-25 | | 7C132-30 7C136-30 7C142-30 7C146-30 | | Unit |
|-----------------------------|---|---------------------------------------|------|---|------|--|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 15 | | 25 | | 30 | | ns |
| t _{AA} | Address to Data Valid ^[12] | | 15 | | 25 | | 30 | ns |
| t _{OHA} | Data Hold from Address Change | 0 | | 0 | | 0 | | ns |
| t _{ACE} | CE LOW to Data Valid ^[12] | | 15 | | 25 | | 30 | ns |
| t _{DOE} | OE LOW to Data Valid ^[12] | | 10 | | 15 | | 20 | ns |
| t _{LZOE} | OE LOW to Low Z ^[10, 13] | 3 | | 3 | | 3 | | ns |
| t _{HZOE} | OE HIGH to High Z ^[10, 13, 14] | | 10 | | 15 | | 15 | ns |
| t _{LZCE} | CE LOW to Low Z ^[10, 13] | 3 | | 5 | | 5 | | ns |
| t _{HZCE} | CE HIGH to High Z ^[10, 13, 14] | | 10 | | 15 | | 15 | ns |
| t _{PU} | CE LOW to Power-Up ^[10] | 0 | | 0 | | 0 | | ns |
| t _{PD} | CE HIGH to Power-Down ^[10] | | 15 | | 25 | | 25 | ns |
| WRITE CYCLE ^[15] | | | | | | | | |
| t _{WC} | Write Cycle Time | 15 | | 25 | | 30 | | ns |
| t _{SCE} | CE LOW to Write End | 12 | | 20 | | 25 | | ns |
| t _{AW} | Address Set-Up to Write End | 12 | | 20 | | 25 | | ns |
| t _{HA} | Address Hold from Write End | 2 | | 2 | | 2 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | 0 | | 0 | | ns |
| t _{PWE} | R/W Pulse Width | 12 | | 15 | | 25 | | ns |
| t _{SD} | Data Set-Up to Write End | 10 | | 15 | | 15 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| t _{HZWE} | R/W LOW to High Z ^[10] | | 10 | | 15 | | 15 | ns |
| t _{LZWE} | R/W HIGH to Low Z ^[10] | 0 | | 0 | | 0 | | ns |



Switching Characteristics Over the Operating Range^[6, 11] (continued)

| Parameter | Description | 7C136-15 ^[3,4] 7C146-15 | | 7C132-25 ^[3] 7C136-25 7C142-25 7C146-25 | | 7C132-30 7C136-30 7C142-30 7C146-30 | | Unit |
|----------------------------------|---|---------------------------------------|---------|---|---------|--|---------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| BUSY/INTERRUPT TIMING | | | | | | | | |
| t _{BLA} | BUSY LOW from Address Match | | 15 | | 20 | | 20 | ns |
| t _{BHA} | BUSY HIGH from Address Mismatch ^[16] | | 15 | | 20 | | 20 | ns |
| t _{BLC} | BUSY LOW from \overline{CE} LOW | | 15 | | 20 | | 20 | ns |
| t _{BHC} | BUSY HIGH from \overline{CE} HIGH ^[16] | | 15 | | 20 | | 20 | ns |
| t _{PS} | Port Set Up for Priority | 5 | | 5 | | 5 | | ns |
| t _{WB} | R/W LOW after BUSY LOW ^[17] | 0 | | 0 | | 0 | | ns |
| t _{WH} | R/W HIGH after BUSY HIGH | 13 | | 20 | | 30 | | ns |
| t _{BDD} | BUSY HIGH to Valid Data | | 15 | | 25 | | 30 | ns |
| t _{DDD} | Write Data Valid to Read Data Valid | | Note 18 | | Note 18 | | Note 18 | ns |
| t _{WDD} | Write Pulse to Data Delay | | Note 18 | | Note 18 | | Note 18 | ns |
| INTERRUPT TIMING ^[19] | | | | | | | | |
| t _{WINS} | R/W to INTERRUPT Set Time | | 15 | | 25 | | 25 | ns |
| t _{EINS} | \overline{CE} to INTERRUPT Set Time | | 15 | | 25 | | 25 | ns |
| t _{INS} | Address to INTERRUPT Set Time | | 15 | | 25 | | 25 | ns |
| t _{OINR} | \overline{OE} to INTERRUPT Reset Time ^[16] | | 15 | | 25 | | 25 | ns |
| t _{EINR} | \overline{CE} to INTERRUPT Reset Time ^[16] | | 15 | | 25 | | 25 | ns |
| t _{INR} | Address to INTERRUPT Reset Time ^[16] | | 15 | | 25 | | 25 | ns |

Shaded area contains preliminary information.

Switching Characteristics Over the Operating Range^[6, 11]

| Parameter | Description | 7C132-35 7C136-35 7C142-35 7C146-35 | | 7C132-45 7C136-45 7C142-45 7C146-45 | | 7C132-55 7C136-55 7C142-55 7C146-55 | | Unit |
|-------------------|--|--|------|--|------|--|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 35 | | 45 | | 55 | | ns |
| t _{AA} | Address to Data Valid ^[12] | | 35 | | 45 | | 55 | ns |
| t _{OHA} | Data Hold from Address Change | 0 | | 0 | | 0 | | ns |
| t _{ACE} | \overline{CE} LOW to Data Valid ^[12] | | 35 | | 45 | | 55 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid ^[12] | | 20 | | 25 | | 25 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z ^[10, 13] | 3 | | 3 | | 3 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[10, 13, 14] | | 20 | | 20 | | 25 | ns |
| t _{LZCE} | \overline{CE} LOW to Low Z ^[10, 13] | 5 | | 5 | | 5 | | ns |
| t _{HZCE} | \overline{CE} HIGH to High Z ^[10, 13, 14] | | 20 | | 20 | | 25 | ns |
| t _{PU} | \overline{CE} LOW to Power-Up ^[10] | 0 | | 0 | | 0 | | ns |
| t _{PD} | \overline{CE} HIGH to Power-Down ^[10] | | 35 | | 35 | | 35 | ns |



Switching Characteristics Over the Operating Range^[6, 11] (continued)

| | | 7C132-35 7C136-35 7C142-35 7C146-35 | 7C132-45 7C136-45 7C142-45 7C146-45 | 7C132-55 7C136-55 7C142-55 7C146-55 | |
|--|---|--|--|--|---------|
| WRITE CYCLE^[15] | | | | | |
| t _{WC} | Write Cycle Time | 35 | 45 | 55 | ns |
| t _{SCE} | \overline{CE} LOW to Write End | 30 | 35 | 40 | ns |
| t _{AW} | Address Set-Up to Write End | 30 | 35 | 40 | ns |
| t _{HA} | Address Hold from Write End | 2 | 2 | 2 | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | 0 | 0 | ns |
| t _{PWE} | R/ \overline{W} Pulse Width | 25 | 30 | 30 | ns |
| t _{SD} | Data Set-Up to Write End | 15 | 20 | 20 | ns |
| t _{HD} | Data Hold from Write End | 0 | 0 | 0 | ns |
| t _{HZWE} | R/ \overline{W} LOW to High Z ^[10] | | 20 | 20 | 25 |
| t _{LZWE} | R/ \overline{W} HIGH to Low Z ^[10] | 0 | 0 | 0 | ns |
| BUSY/INTERRUPT TIMING | | | | | |
| t _{BLA} | BUSY LOW from Address Match | | 20 | 25 | 30 |
| t _{BHA} | BUSY HIGH from Address Mismatch ^[16] | | 20 | 25 | 30 |
| t _{BLC} | BUSY LOW from \overline{CE} LOW | | 20 | 25 | 30 |
| t _{BHC} | BUSY HIGH from \overline{CE} HIGH ^[16] | | 20 | 25 | 30 |
| t _{PS} | Port Set Up for Priority | 5 | 5 | 5 | ns |
| t _{WB} | R/ \overline{W} LOW after BUSY LOW ^[17] | 0 | 0 | 0 | ns |
| t _{WH} | R/ \overline{W} HIGH after BUSY HIGH | 30 | 35 | 35 | ns |
| t _{BDD} | BUSY HIGH to Valid Data | | 35 | 45 | 45 |
| t _{DDD} | Write Data Valid to Read Data Valid | | Note 18 | Note 18 | Note 18 |
| t _{WDD} | Write Pulse to Data Delay | | Note 18 | Note 18 | Note 18 |
| INTERRUPT TIMING^[19] | | | | | |
| t _{WINS} | R/ \overline{W} to INTERRUPT Set Time | | 25 | 35 | 45 |
| t _{EINS} | \overline{CE} to INTERRUPT Set Time | | 25 | 35 | 45 |
| t _{INS} | Address to INTERRUPT Set Time | | 25 | 35 | 45 |
| t _{OINR} | \overline{OE} to INTERRUPT Reset Time ^[16] | | 25 | 35 | 45 |
| t _{EINR} | \overline{CE} to INTERRUPT Reset Time ^[16] | | 25 | 35 | 45 |
| t _{INR} | Address to INTERRUPT Reset Time ^[16] | | 25 | 35 | 45 |

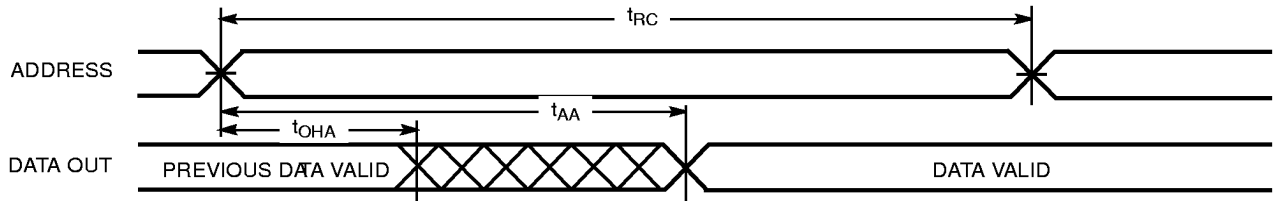
Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
- At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
- t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and R/ \overline{W} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
- CY7C142/CY7C146 only.
- A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
 BUSY on Port B goes HIGH.
 Port B's address toggled.
 \overline{CE} for Port B is toggled.
 R/ \overline{W} for Port B is toggled during valid read.
- 52-pin PLCC and PQFP versions only.



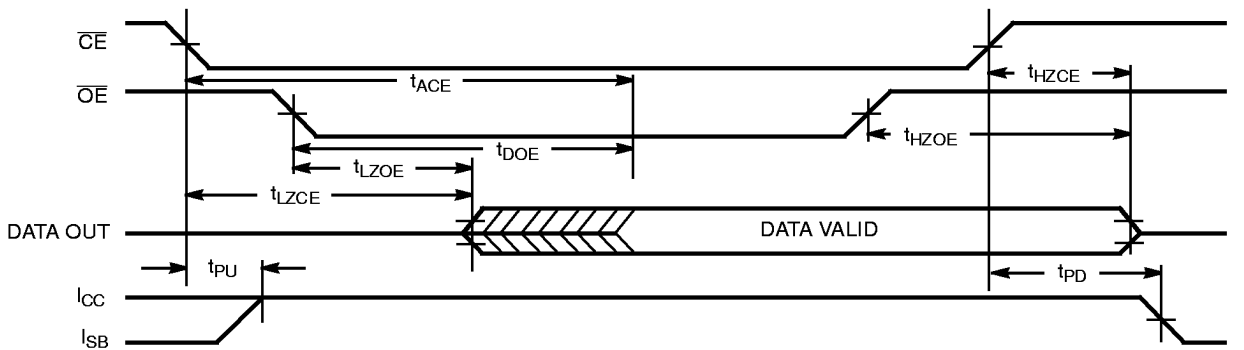
Switching Waveforms

Read Cycle No. 1 (Either Port-Address Access)^[20, 21]



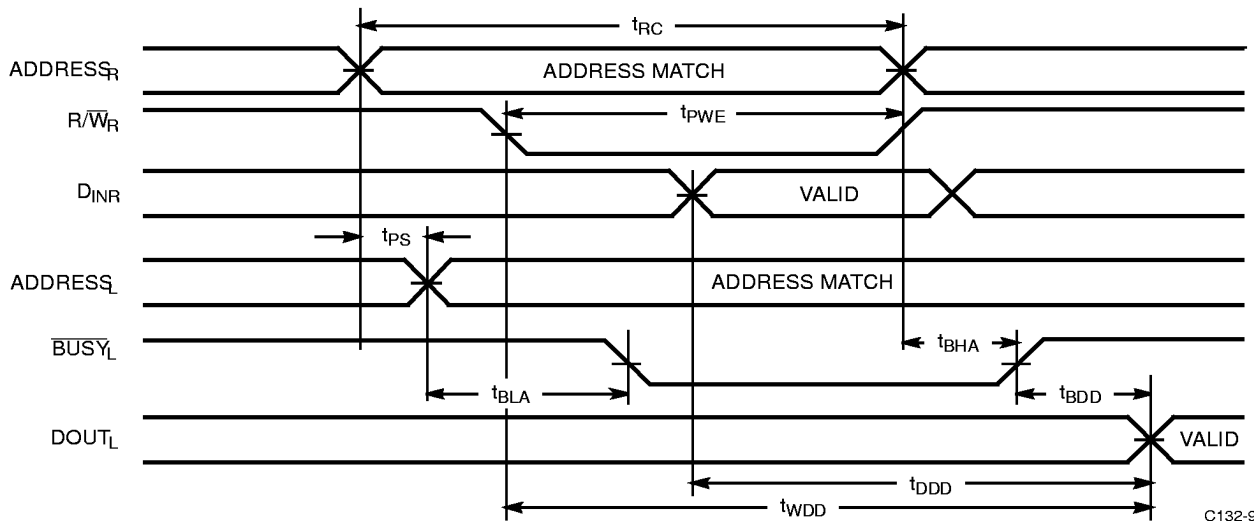
C132-7

Read Cycle No. 2 (Either Port- $\overline{\text{CE}}$ / $\overline{\text{OE}}$)^[20, 22]



C132-8

Read Cycle No. 3 (Read with $\overline{\text{BUSY}}$ Master: CY7C132 and CY7C136)



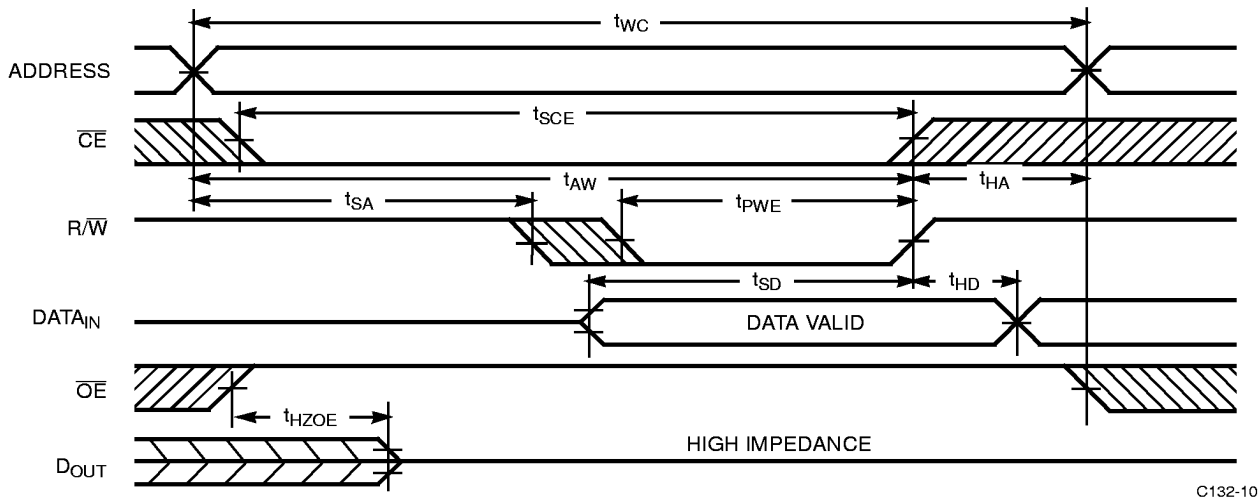
C132-9

Notes:

20. R/ $\overline{\text{W}}$ is HIGH for read cycle.
21. Device is continuously selected, $\overline{\text{CE}} = V_{\text{IL}}$ and $\overline{\text{OE}} = V_{\text{IL}}$.
22. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.

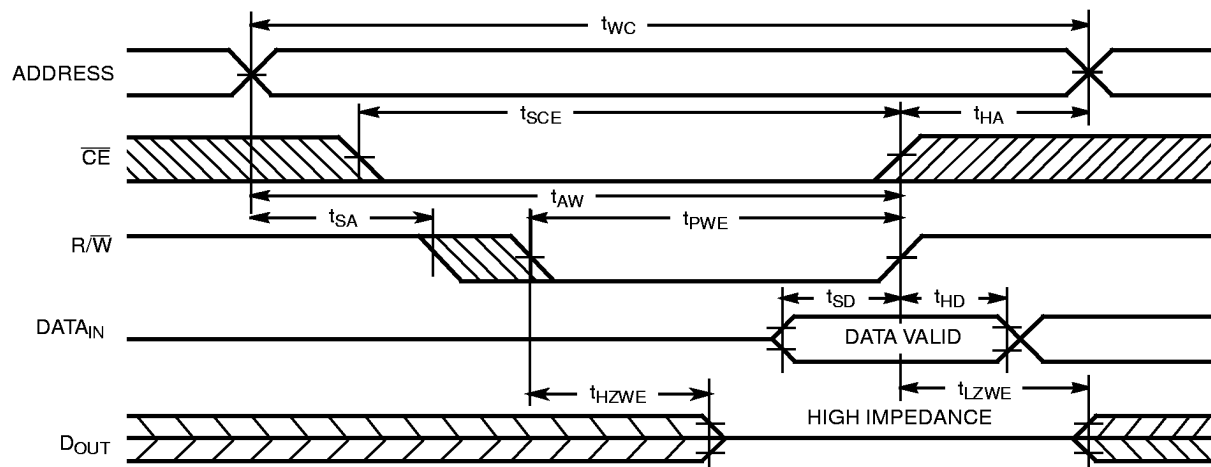
Switching Waveforms (continued)

Write Cycle No.1 (\overline{OE} Three-States Data I/Os-Either Port)^[15, 23]



C132-10

Write Cycle No. 2 (R/W Three-States Data I/Os-Either Port)^[15, 24]



C132-11

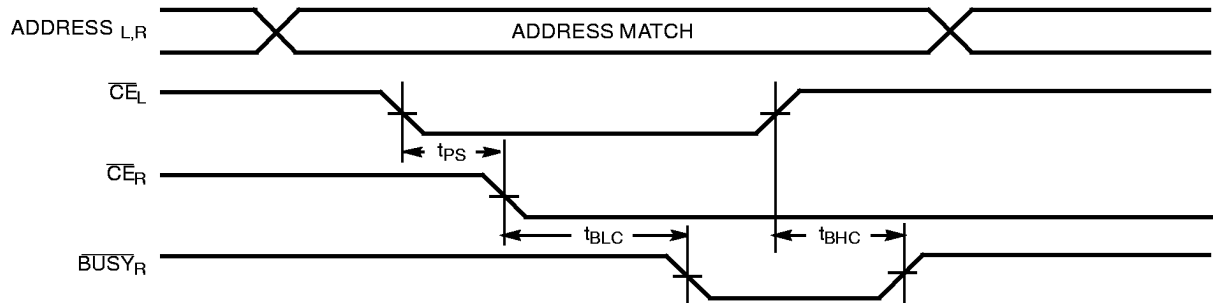
Notes:

23. If \overline{OE} is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD} .
24. If the \overline{CE} LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in a high-impedance state.

Switching Waveforms (continued)

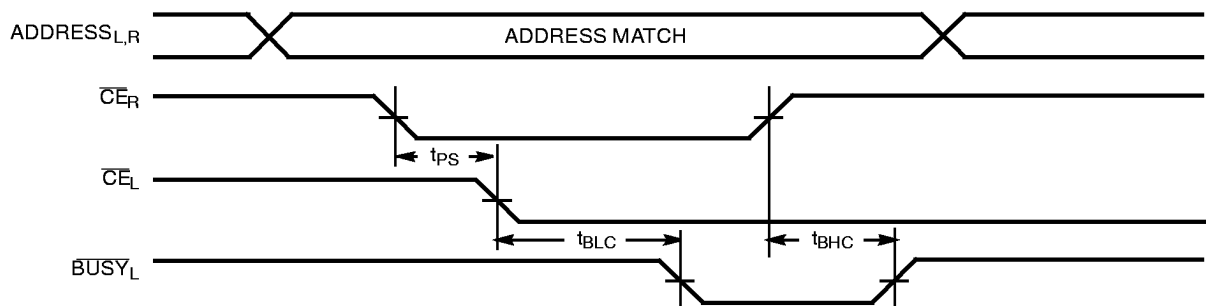
Busy Timing Diagram No. 1 (\overline{CE} Arbitration)

\overline{CE}_L Valid First:



C132-12

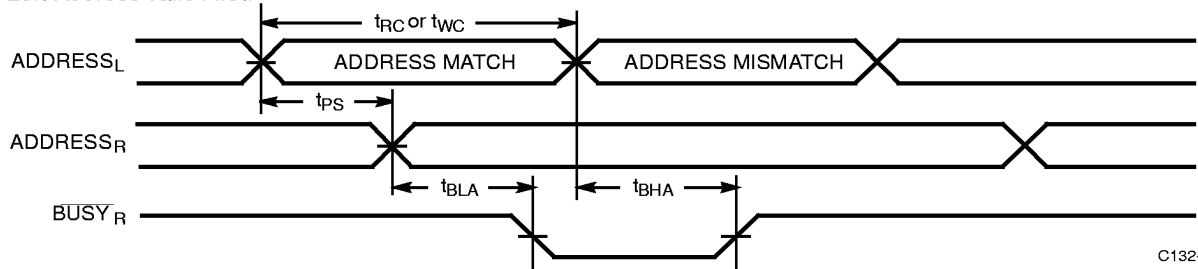
\overline{CE}_R Valid First:



C132-13

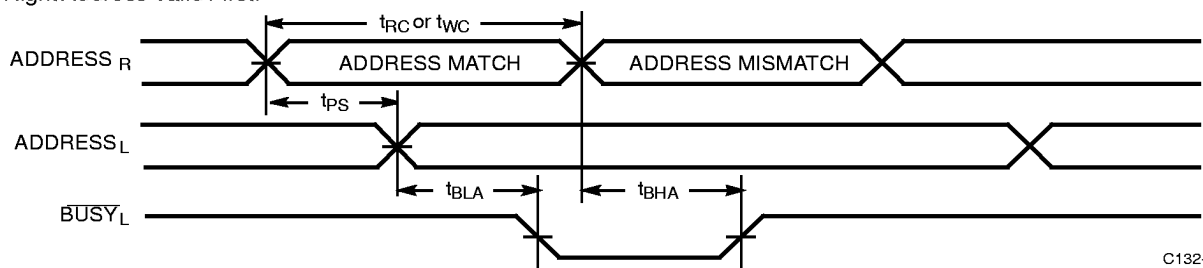
Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:



C132-14

Right Address Valid First:

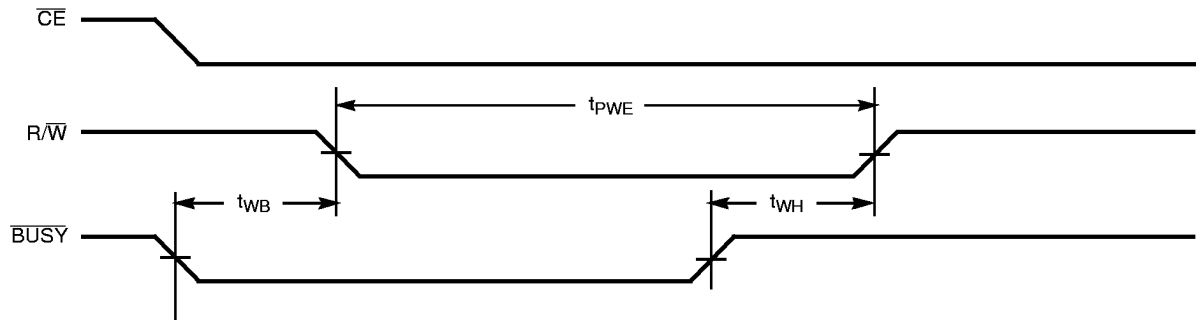


C132-15



Switching Waveforms (continued)

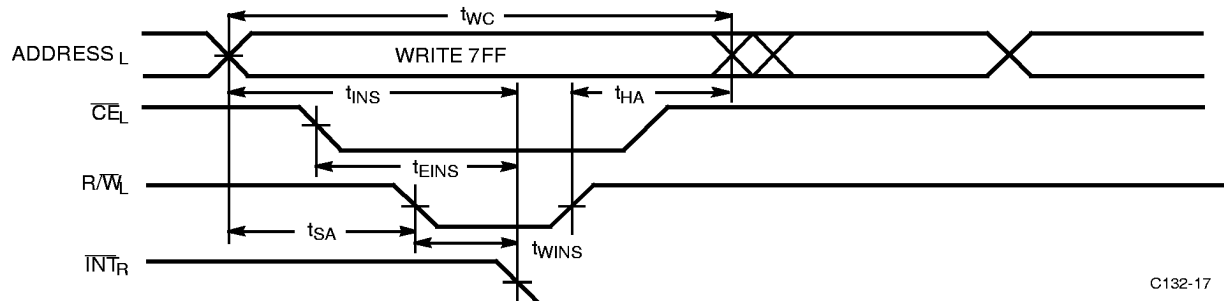
Busy Timing Diagram No. 3 (Write with $\overline{\text{BUSY}}$, Slave: CY7C142/CY7C146)



C132-16

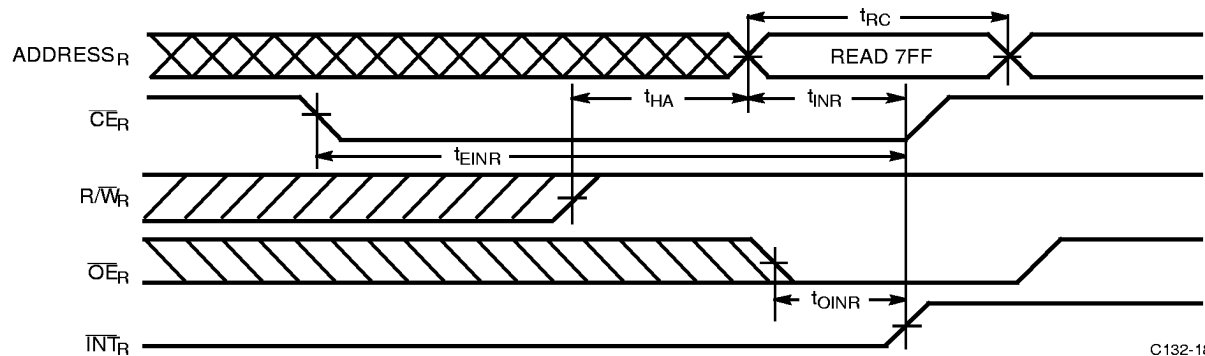
Interrupt Timing Diagrams^[19]

Left Side Sets $\overline{\text{INT}}_{\text{R}}$:



C132-17

Right Side Clears $\overline{\text{INT}}_{\text{R}}$:

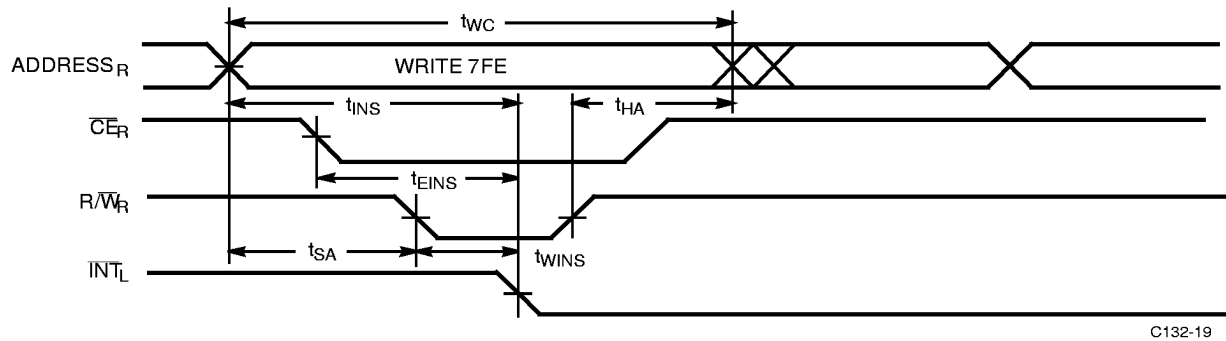


C132-18

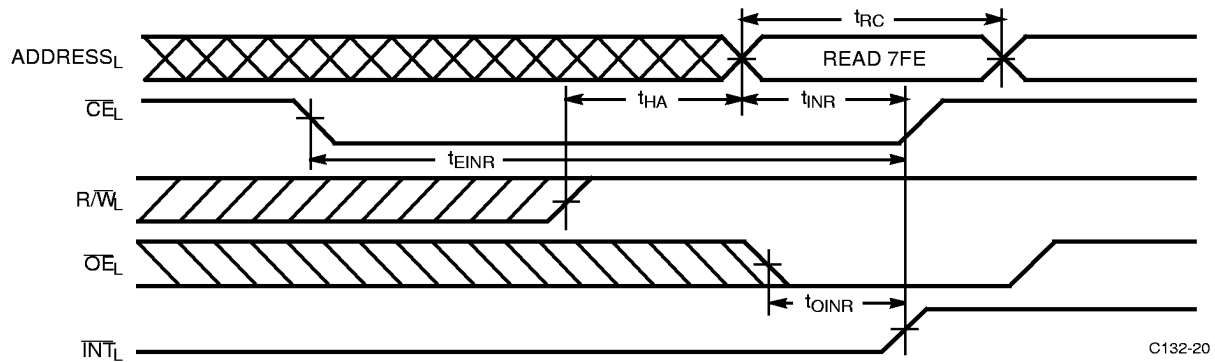


Interrupt Timing Diagrams^[19] (continued)

Right Side Sets \overline{INT}_L :

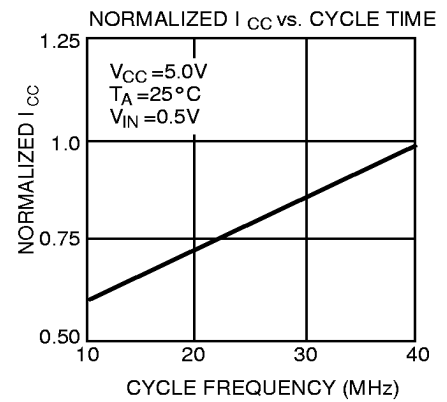
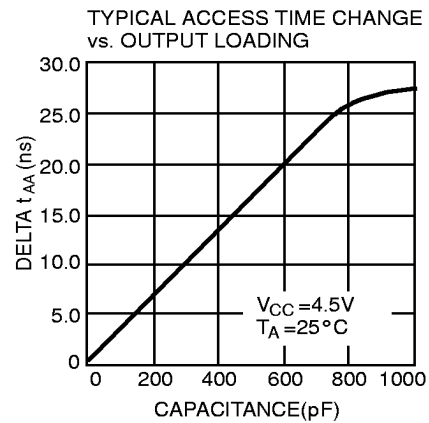
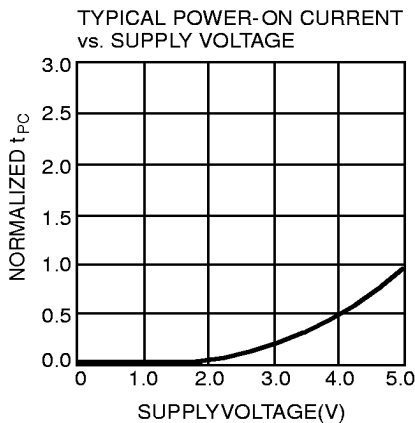
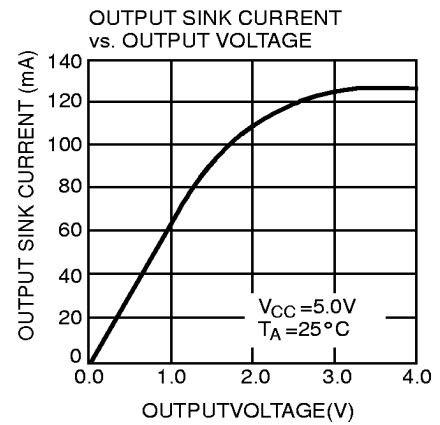
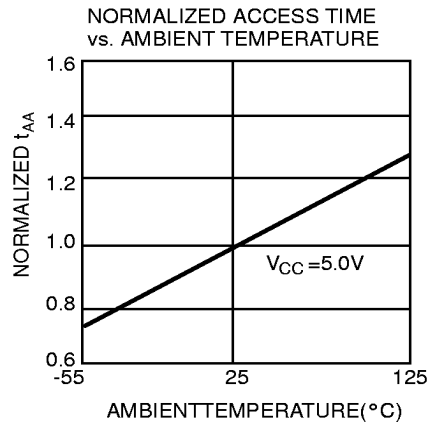
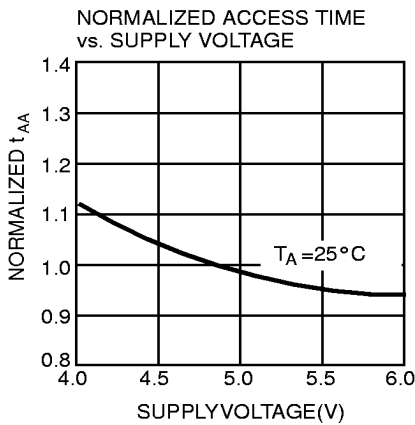
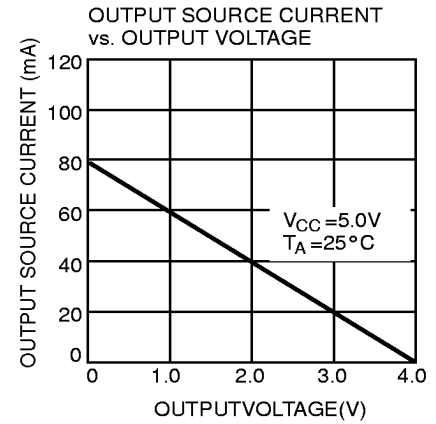
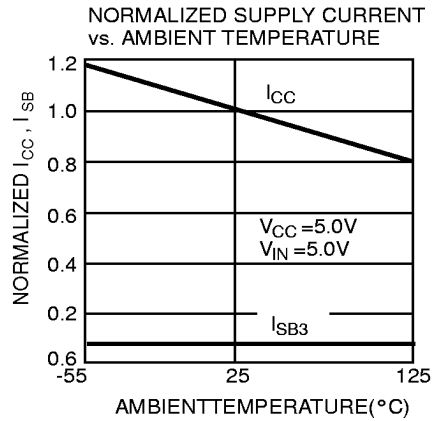
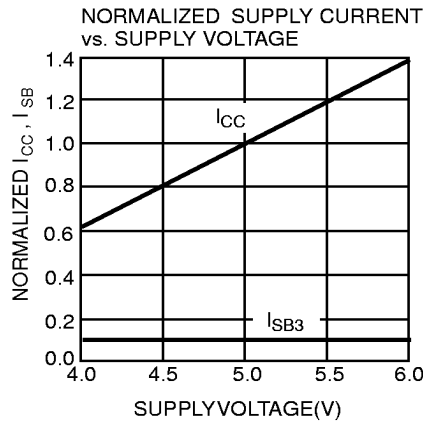


Right Side Clears \overline{INT}_L :





Typical DC and AC Characteristics





Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|---------------|--------------|-------------------------------------|-----------------|
| 30 | CY7C132-30PC | P25 | 48-Lead (600-Mil) Molded DIP | Commercial |
| | CY7C132-30PI | P25 | 48-Lead (600-Mil) Molded DIP | Industrial |
| 35 | CY7C132-35PC | P25 | 48-Lead (600-Mil) Molded DIP | Commercial |
| | CY7C132-35PI | P25 | 48-Lead (600-Mil) Molded DIP | Industrial |
| | CY7C132-35DMB | D26 | 48-Lead (600-Mil) Sidebrazed DIP | Military |
| 45 | CY7C132-45PC | P25 | 48-Lead (600-Mil) Molded DIP | Commercial |
| | CY7C132-45PI | P25 | 48-Lead (600-Mil) Molded DIP | Industrial |
| | CY7C132-45DMB | D26 | 48-Lead (600-Mil) Sidebrazed DIP | Military |
| 55 | CY7C132-55PC | P25 | 48-Lead (600-Mil) Molded DIP | Commercial |
| | CY7C132-55PI | P25 | 48-Lead (600-Mil) Molded DIP | Industrial |
| | CY7C132-55DMB | D26 | 48-Lead (600-Mil) Sidebrazed DIP | Military |
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
| 15 | CY7C136-15JC | J69 | 52-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C136-15NC | N52 | 52-Pin Plastic Quad Flatpack | |
| 25 | CY7C136-25JC | J69 | 52-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C136-25NC | N52 | 52-Pin Plastic Quad Flatpack | |
| 30 | CY7C136-30JC | J69 | 52-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C136-30NC | N52 | 52-Pin Plastic Quad Flatpack | |
| | CY7C136-30JI | J69 | 52-Lead Plastic Leaded Chip Carrier | |
| 35 | CY7C136-35JC | J69 | 52-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C136-35NC | N52 | 52-Pin Plastic Quad Flatpack | |
| | CY7C136-35JI | J69 | 52-Lead Plastic Leaded Chip Carrier | |
| | CY7C136-35LMB | L69 | 52-Square Leadless Chip Carrier | |
| 45 | CY7C136-45JC | J69 | 52-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C136-45NC | N52 | 52-Pin Plastic Quad Flatpack | |
| | CY7C136-45JI | J69 | 52-Lead Plastic Leaded Chip Carrier | |
| | CY7C136-45LMB | L69 | 52-Square Leadless Chip Carrier | |
| 55 | CY7C136-55JC | J69 | 52-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C136-55NC | N52 | 52-Pin Plastic Quad Flatpack | |
| | CY7C136-55JI | J69 | 52-Lead Plastic Leaded Chip Carrier | |
| | CY7C136-55LMB | L69 | 52-Square Leadless Chip Carrier | |

Shaded area contains preliminary information.



Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|---------------|--------------|-------------------------------------|-----------------|
| 30 | CY7C142-30PC | P25 | 48-Lead (600-Mil) Molded DIP | Commercial |
| | CY7C142-30PI | P25 | 48-Lead (600-Mil) Molded DIP | Industrial |
| 35 | CY7C142-35PC | P25 | 48-Lead (600-Mil) Molded DIP | Commercial |
| | CY7C142-35PI | P25 | 48-Lead (600-Mil) Molded DIP | Industrial |
| | CY7C142-35DMB | D26 | 48-Lead (600-Mil) Sidebrazed DIP | Military |
| 45 | CY7C142-45PC | P25 | 48-Lead (600-Mil) Molded DIP | Commercial |
| | CY7C142-45PI | P25 | 48-Lead (600-Mil) Molded DIP | Industrial |
| | CY7C142-45DMB | D26 | 48-Lead (600-Mil) Sidebrazed DIP | Military |
| 55 | CY7C142-55PC | P25 | 48-Lead (600-Mil) Molded DIP | Commercial |
| | CY7C142-55PI | P25 | 48-Lead (600-Mil) Molded DIP | Industrial |
| | CY7C142-55DMB | D26 | 48-Lead (600-Mil) Sidebrazed DIP | Military |
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
| 15 | CY7C136-15JC | J69 | 52-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C136-15NC | N52 | 52-Pin Plastic Quad Flatpack | |
| 25 | CY7C146-25JC | J69 | 52-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C146-25NC | N52 | 52-Pin Plastic Quad Flatpack | |
| 30 | CY7C146-30JC | J69 | 52-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C146-30NC | N52 | 52-Pin Plastic Quad Flatpack | |
| | CY7C146-30JI | J69 | 52-Lead Plastic Leaded Chip Carrier | Industrial |
| 35 | CY7C146-35JC | J69 | 52-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C146-35NC | N52 | 52-Pin Plastic Quad Flatpack | |
| | CY7C146-35JI | J69 | 52-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C146-35LMB | L69 | 52-Square Leadless Chip Carrier | Military |
| 45 | CY7C146-45JC | J69 | 52-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C146-45NC | N52 | 52-Pin Plastic Quad Flatpack | |
| | CY7C146-45JI | J69 | 52-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C146-45LMB | L69 | 52-Square Leadless Chip Carrier | Military |
| 55 | CY7C146-55JC | J69 | 52-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C146-55NC | N52 | 52-Pin Plastic Quad Flatpack | |
| | CY7C146-55JI | J69 | 52-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C146-55LMB | L69 | 52-Square Leadless Chip Carrier | Military |

Shaded area contains preliminary information.



MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

| Parameter | Subgroups |
|---------------|-----------|
| V_{OH} | 1, 2, 3 |
| V_{OL} | 1, 2, 3 |
| V_{IH} | 1, 2, 3 |
| V_{IL} Max. | 1, 2, 3 |
| I_{IX} | 1, 2, 3 |
| I_{OZ} | 1, 2, 3 |
| I_{CC} | 1, 2, 3 |
| I_{SB1} | 1, 2, 3 |
| I_{SB2} | 1, 2, 3 |
| I_{SB3} | 1, 2, 3 |
| I_{SB4} | 1, 2, 3 |

Switching Characteristics

| Parameter | Subgroups |
|------------------------------|-----------------|
| READ CYCLE | |
| t_{RC} | 7, 8, 9, 10, 11 |
| t_{AA} | 7, 8, 9, 10, 11 |
| t_{ACE} | 7, 8, 9, 10, 11 |
| t_{DOE} | 7, 8, 9, 10, 11 |
| WRITE CYCLE | |
| t_{WC} | 7, 8, 9, 10, 11 |
| t_{SCE} | 7, 8, 9, 10, 11 |
| t_{AW} | 7, 8, 9, 10, 11 |
| t_{HA} | 7, 8, 9, 10, 11 |
| t_{SA} | 7, 8, 9, 10, 11 |
| t_{PWE} | 7, 8, 9, 10, 11 |
| t_{SD} | 7, 8, 9, 10, 11 |
| t_{HD} | 7, 8, 9, 10, 11 |
| BUSY/INTERRUPT TIMING | |
| t_{BLA} | 7, 8, 9, 10, 11 |
| t_{BHA} | 7, 8, 9, 10, 11 |
| t_{BLC} | 7, 8, 9, 10, 11 |
| t_{BHC} | 7, 8, 9, 10, 11 |
| t_{PS} | 7, 8, 9, 10, 11 |
| t_{WINS} | 7, 8, 9, 10, 11 |
| t_{EINS} | 7, 8, 9, 10, 11 |
| t_{INS} | 7, 8, 9, 10, 11 |
| t_{OINR} | 7, 8, 9, 10, 11 |
| t_{EINR} | 7, 8, 9, 10, 11 |
| t_{INR} | 7, 8, 9, 10, 11 |
| BUSY TIMING | |
| $t_{WB}^{[25]}$ | 7, 8, 9, 10, 11 |
| t_{WH} | 7, 8, 9, 10, 11 |
| t_{BDD} | 7, 8, 9, 10, 11 |

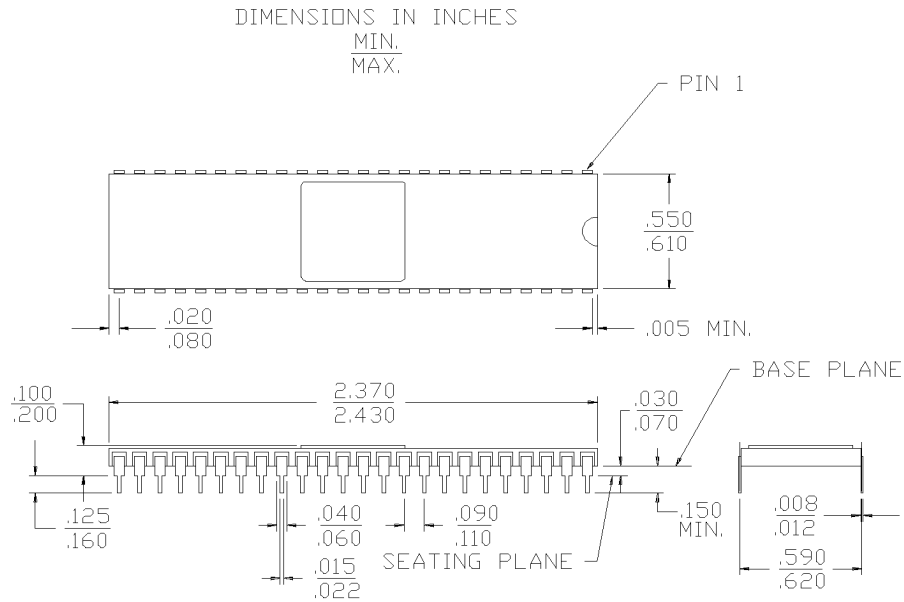
Note:

25. CY7C142/CY7C146 only.

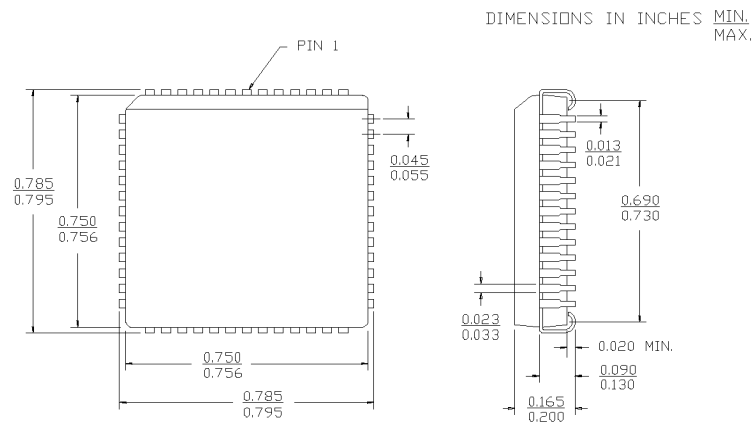
Document #: 38-00061-L

Package Diagrams

48-Lead (600-Mil) Sidebrazed DIP D26



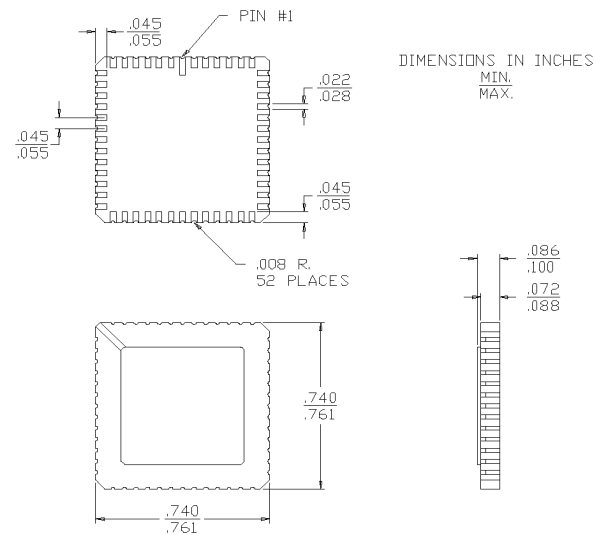
52-Lead Plastic Leaded Chip Carrier J69



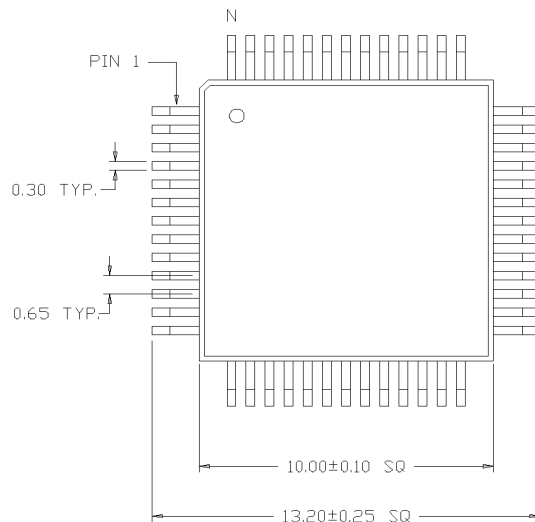


Package Diagrams (continued)

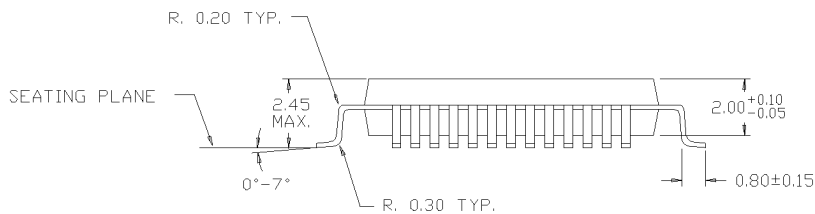
52-Square Leadless Chip Carrier L69



52-Lead Plastic Quad Flatpack N52



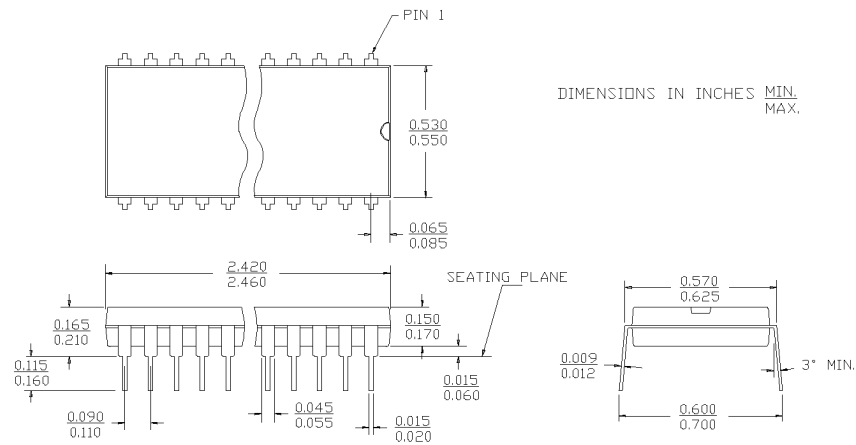
DIMENSIONS ARE IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.





Package Diagrams (continued)

48-Lead (600-Mil) Molded DIP P25



© Cypress Semiconductor Corporation, 1997. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress Semiconductor product. Nor does it convey or imply any license under patent or other rights. Cypress Semiconductor does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress Semiconductor products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress Semiconductor against all charges.