CD54HC74, CD74HC74, CD54HCT74, CD74HCT74

Dual D Flip-Flop with Set and Reset
Positive-Edge Trigger

Features

- **Hysteresis on Clock Inputs for Improved Noise Immunity and Increased Input Rise and Fall Times**

- **Asynchronous Set and Reset**

- **Complementary Outputs**

- **Buffered Inputs**

- **Typical f_{MAX} = 50MHz at V_{CC} = 5V, C_L = 15pF, T_A = 25°C**

- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**

- **Wide Operating Temperature Range . . . -55°C to 125°C**

- **Balanced Propagation Delay and Transition Times**

- **Significant Power Reduction Compared to LSTTL Logic ICs**

- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**

- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu$A at V_{OL}, V_{OH}**

Description

The 'HC74 and 'HCT74 utilize silicon gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

This flip-flop has independent DATA, $\overline{SET}$, $\overline{RESET}$ and CLOCK inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. $\overline{SET}$ and $\overline{RESET}$ are independent of the clock and are accomplished by a low level at the appropriate input.

The HCT logic family is functionally as well as pin compatible with the standard LS logic family.
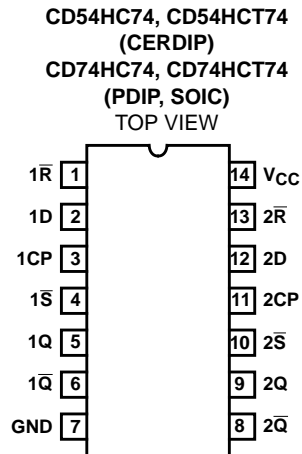
Ordering Information

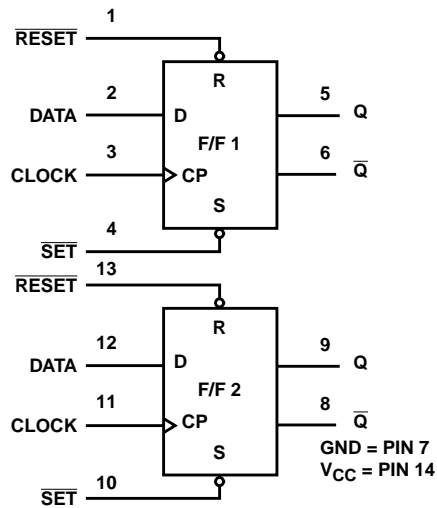| PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
CD54HC74F3A	-55 to 125	14 Ld CERDIP
CD54HCT74F3A	-55 to 125	14 Ld CERDIP
CD74HC74E	-55 to 125	14 Ld PDIP
CD74HC74M	-55 to 125	14 Ld SOIC
CD74HC74MT	-55 to 125	14 Ld SOIC
CD74HC74M96	-55 to 125	14 Ld SOIC
CD74HCT74E	-55 to 125	14 Ld PDIP
CD74HCT74M	-55 to 125	14 Ld SOIC
CD74HCT74MT	-55 to 125	14 Ld SOIC
CD74HCT74M96	-55 to 125	14 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

**CD54HC74, CD54HCT74
(CERDIP)
CD74HC74, CD74HCT74
(PDIP, SOIC)**
TOP VIEW

```
        ┌───┬───┐
1R̄  1 │   U   │ 14  VCC
1D  2 │       │ 13  2R̄
1CP 3 │       │ 12  2D
1S̄  4 │       │ 11  2CP
1Q  5 │       │ 10  2S̄
1Q̄  6 │       │ 9   2Q
GND 7 │       │ 8   2Q̄
        └───────┘
```

Functional Diagram

```
RESET ──1──o─┐
             R
DATA ──2── D      F/F 1    Q ──5──
CLOCK ──3── >CP            Q̄ ──6──
             S
SET ──4──o─┘

RESET ──13──o─┐
              R
DATA ──12── D     F/F 2    Q ──9──
CLOCK ──11── >CP           Q̄ ──8──
              S
SET ──10──o─┘
```

GND = PIN 7
VCC = PIN 14

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{SET}$	$\overline{RESET}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

H= High Level (Steady State)
L= Low Level (Steady State)
X= Don't Care
↑= Low-to-High Transition
Q0 = the level of Q before the indicated input conditions were established.
NOTE:

1. This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

CD54HC74, CD74HC74, CD54HCT74, CD74HCT74

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
   For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . ±20mA
DC Drain Current, per Output, I_O
   For -0.5V < V_O < V_{CC} + 0.5V . . . . ±25mA
DC Output Diode Current, I_{OK}
   For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
   For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . ±50mA

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (^{o}C/W)
   E (PDIP) Package 80
   M (SOIC) Package. 86
Maximum Junction Temperature (Hermetic Package or Die) . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Storage Temperature Range . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
  (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A) . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
  HC Types . . . . .2V to 6V
  HCT Types . . . . .4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
  2V . . . . 1000ns (Max)
  4.5V. . . . . 500ns (Max)
  6V . . . . 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
				4.5	4.4	-	-	4.4	-	4.4	-	V
				6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
				4.5	-	-	0.1	-	0.1	-	0.1	V
				6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	4	-	40	-	80	μA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	-	5.5	-		±0.1	-	±1	-	±1	μA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	4	-	40	-	80	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 3)	V_{CC} - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

3. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
D	0.5
$\overline{R}$	0.5
CP	0.7
$\overline{S}$	0.75

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

Prerequisite For Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Data to CP Setup Time (Figure 5)	t_{SU}	-	2	60	-	-	75	-	90	-	ns
			4.5	12	-	-	15	-	18	-	ns
			6	10	-	-	13	-	15	-	ns

Prerequisite For Switching Specifications   (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Hold Time (Figure 5)	t_H	-	2	3	-	-	3	-	3	-	ns
			4.5	3	-	-	3	-	3	-	ns
			6	3	-	-	3	-	3	-	ns
Removal Time $\overline{R}$, $\overline{S}$, to CP (Figure 5)	t_{REM}	-	2	30	-	-	40	-	45	-	ns
			4.5	6	-	-	8	-	9	-	ns
			6	5	-	-	7	-	8	-	ns
Pulse Width $\overline{R}$, $\overline{S}$ (Figure 1)	t_W	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Pulse Width CP (Figure 1)	t_W	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
CP Frequency	f_{MAX}	-	2	6	-	-	5	-	4	-	MHz
			4.5	30	-	-	25	-	20	-	MHz
			6	35	-	-	29	-	23	-	MHz
HCT TYPES											
Data to CP Setup Time (Figure 6)	t_{SU}	-	4.5	12	-	-	15	-	18	-	ns
Hold Time (Figure 6)	t_H	-	4.5	3	-	-	3	-	3	-	ns
Removal Time $\overline{R}$, $\overline{S}$, to CP (Figure 6)	t_{REM}	-	4.5	6	-	-	8	-	9	-	ns
Pulse Width $\overline{R}$, $\overline{S}$ (Figure 2)	t_W	-	4.5	16	-	-	20	-	24	-	ns
Pulse Width CP (Figure 2)	t_W	-	4.5	18	-	-	23	-	27	-	ns
CP Frequency	f_{MAX}	-	4.5	25	-	-	20	-	16	-	MHz

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, CP to Q, $\overline{Q}$ (Figure 3)	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	175	-	220	-	265	ns
		C_L = 50pF	4.5	-	-	35	-	44	-	53	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	30	-	37	-	45	ns
Propagation Delay, $\overline{R}$, $\overline{S}$ to Q, $\overline{Q}$ (Figure 3)	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	200	-	250	-	300	ns
		C_L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C_L = 15pF	5	-	17	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	34	-	43	-	51	ns
Transition Time (Figure 3)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
		C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
		C_L = 50pF	6	-	-	13	-	16	-	19	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF

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Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_CC (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CP Frequency	f_{MAX}	CL = 15pF	5	-	50	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	-	25	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay, CP to Q, $\overline{Q}$ (Figure 4)	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	35	-	44	-	53	ns
Propagation Delay, R, S to Q, Q (Figure 4)	t_{PHL}, t_{PLH}	C_L = 50pF	4.5	-	-	40	-	50	-	60	ns
Transition Time (Figure 4)	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
CP Frequency	f_{MAX}	CL = 15pF	5	-	50	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	-	30	-	-	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per flip-flop.

5. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms
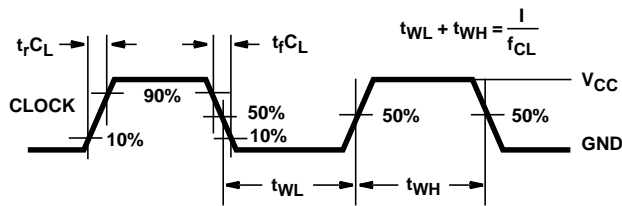
NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH
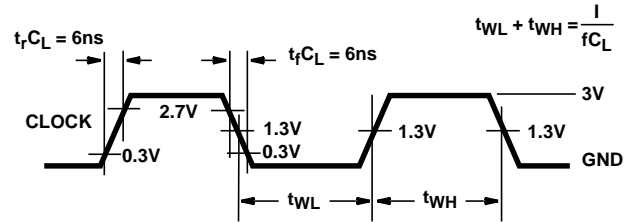
NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH
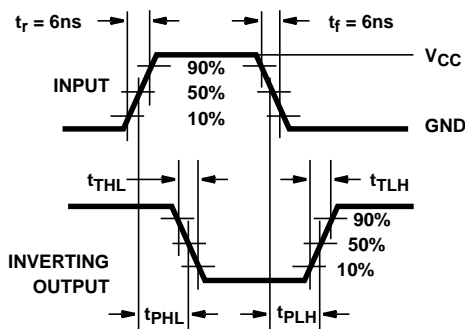
FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC
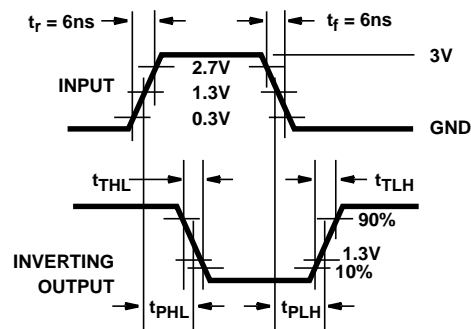
FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Test Circuits and Waveforms (Continued)
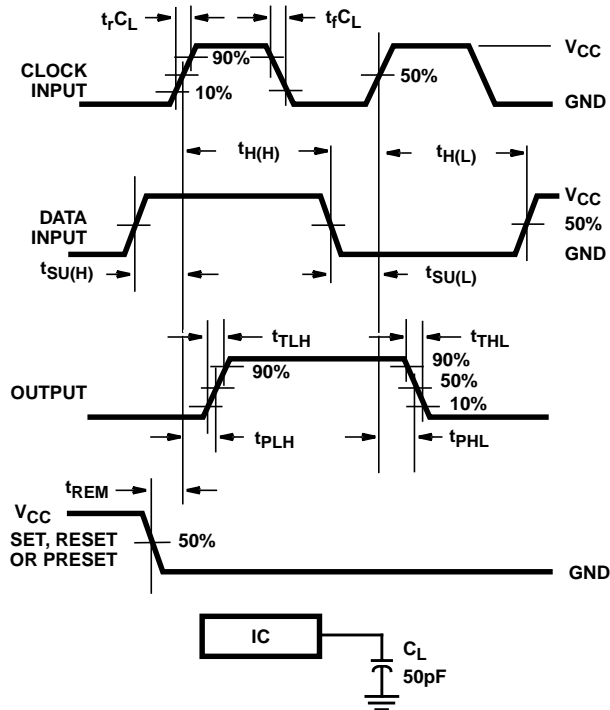
FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS
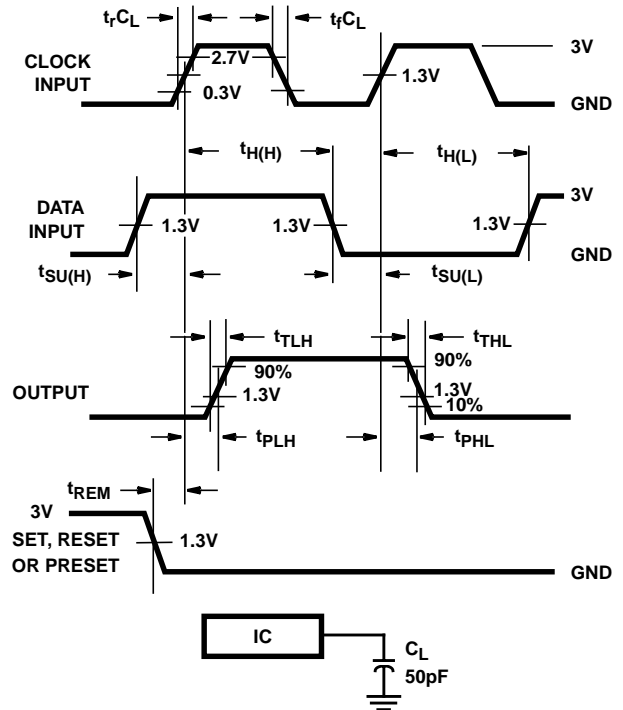
FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8685301CA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-8685301CA CD54HCT74F3A	Samples
CD54HC74F	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	CD54HC74F	Samples
CD54HC74F3A	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8405601CA CD54HC74F3A	Samples
CD54HCT74F	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT74F	Samples
CD54HCT74F3A	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-8685301CA CD54HCT74F3A	Samples
CD74HC74E	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC74E	Samples
CD74HC74EE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC74E	Samples
CD74HC74M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74M	Samples
CD74HC74M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74M	Samples
CD74HC74M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74M	Samples
CD74HC74MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74M	Samples
CD74HC74MTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74M	Samples
CD74HCT74E	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT74E	Samples
CD74HCT74M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT74M	Samples
CD74HCT74M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT74M	Samples
CD74HCT74M96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT74M	Samples
CD74HCT74ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT74M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT74MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT74M	Samples
CD74HCT74MTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT74M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
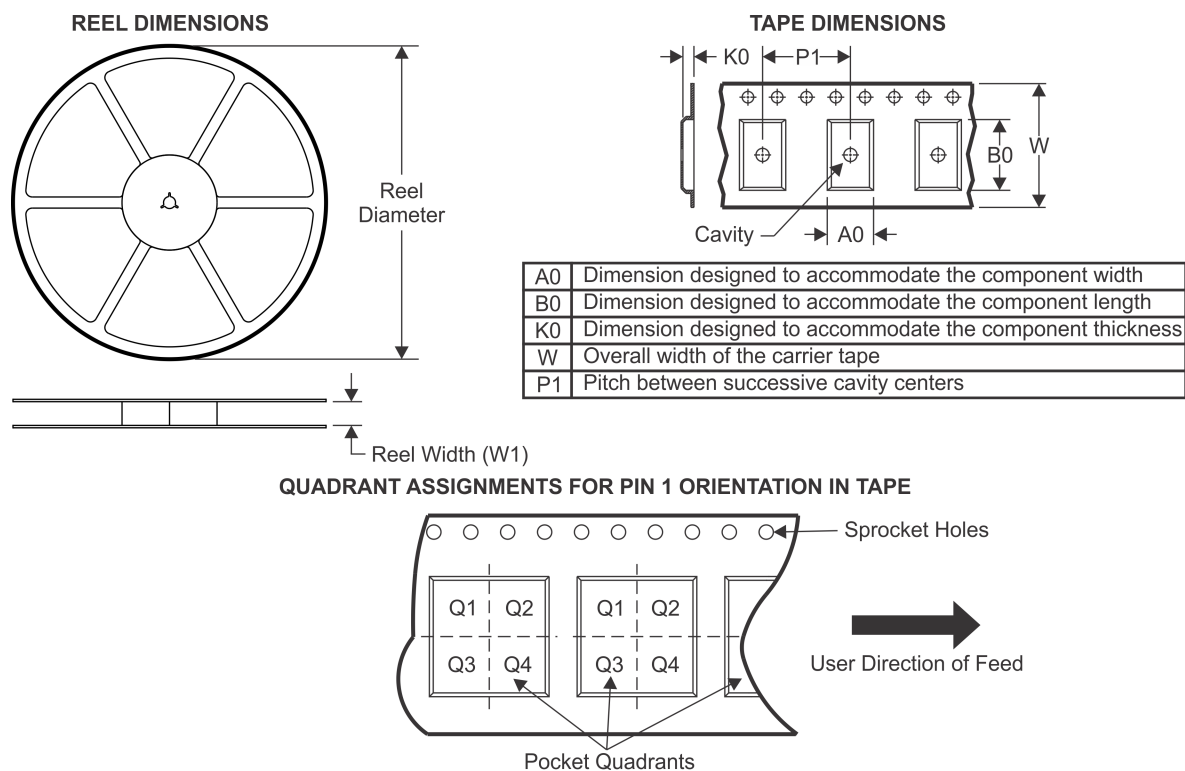
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo]

PACKAGE OPTION ADDENDUM

OTHER QUALIFIED VERSIONS OF CD54HC74, CD54HCT74, CD74HC74, CD74HCT74 :

● Catalog: CD74HC74, CD74HCT74

● Military: CD54HC74, CD54HCT74

NOTE: Qualified Version Definitions:

    ● Catalog - TI's standard catalog product

    ● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC74M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC74MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT74M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT74MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS
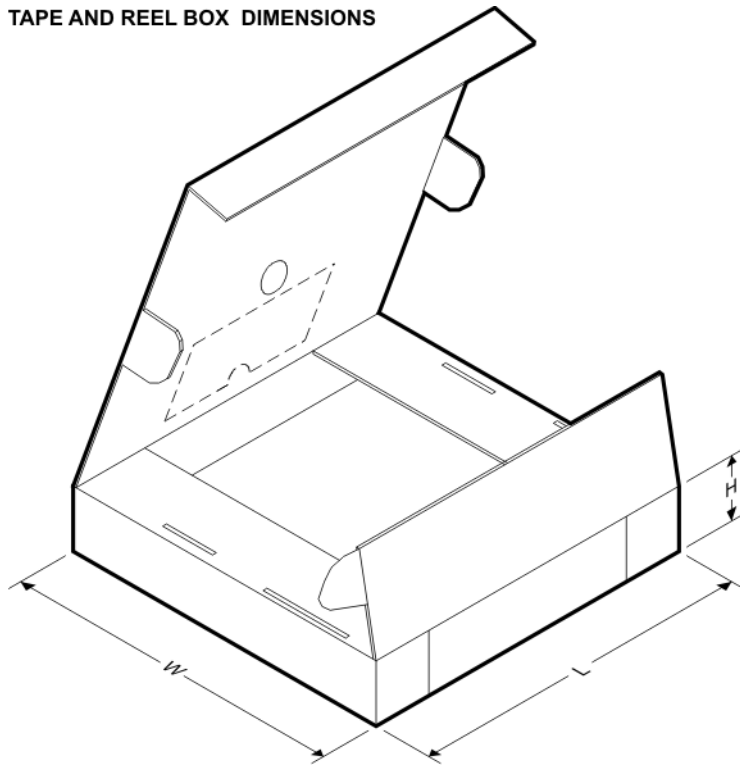
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC74M96	SOIC	D	14	2500	367.0	367.0	38.0
CD74HC74MT	SOIC	D	14	250	210.0	185.0	35.0
CD74HCT74M96	SOIC	D	14	2500	367.0	367.0	38.0
CD74HCT74MT	SOIC	D	14	250	210.0	185.0	35.0
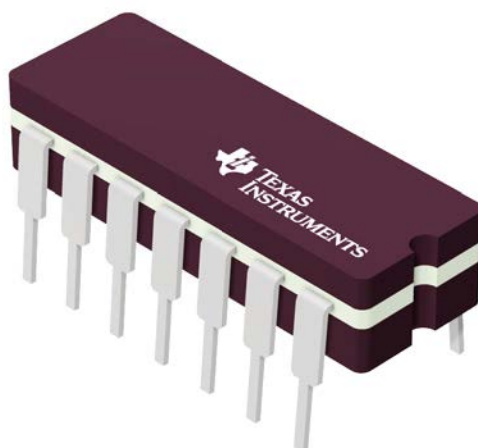
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

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PIN 1 ID
(OPTIONAL)

1

14

12X .100
[2.54]

7

8

B

.245-.283
[6.22-7.19]

.754-.785
[19.15-19.94]

A

4X .005 MIN
[0.13]

14X .045-.065
[1.15-1.65]

.015-.060 TYP
[0.38-1.52]

14X .014-.026
[0.36-0.66]

⊕ .010 [0.25] C A B

.2 MAX TYP
[5.08]

.13 MIN TYP
[3.3]

C

SEATING PLANE

.308-.314
[7.83-7.97]
AT GAGE PLANE

.015
[0.38]

GAGE PLANE

0°-15°
TYP

14X .008-.014
[0.2-0.36]
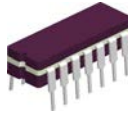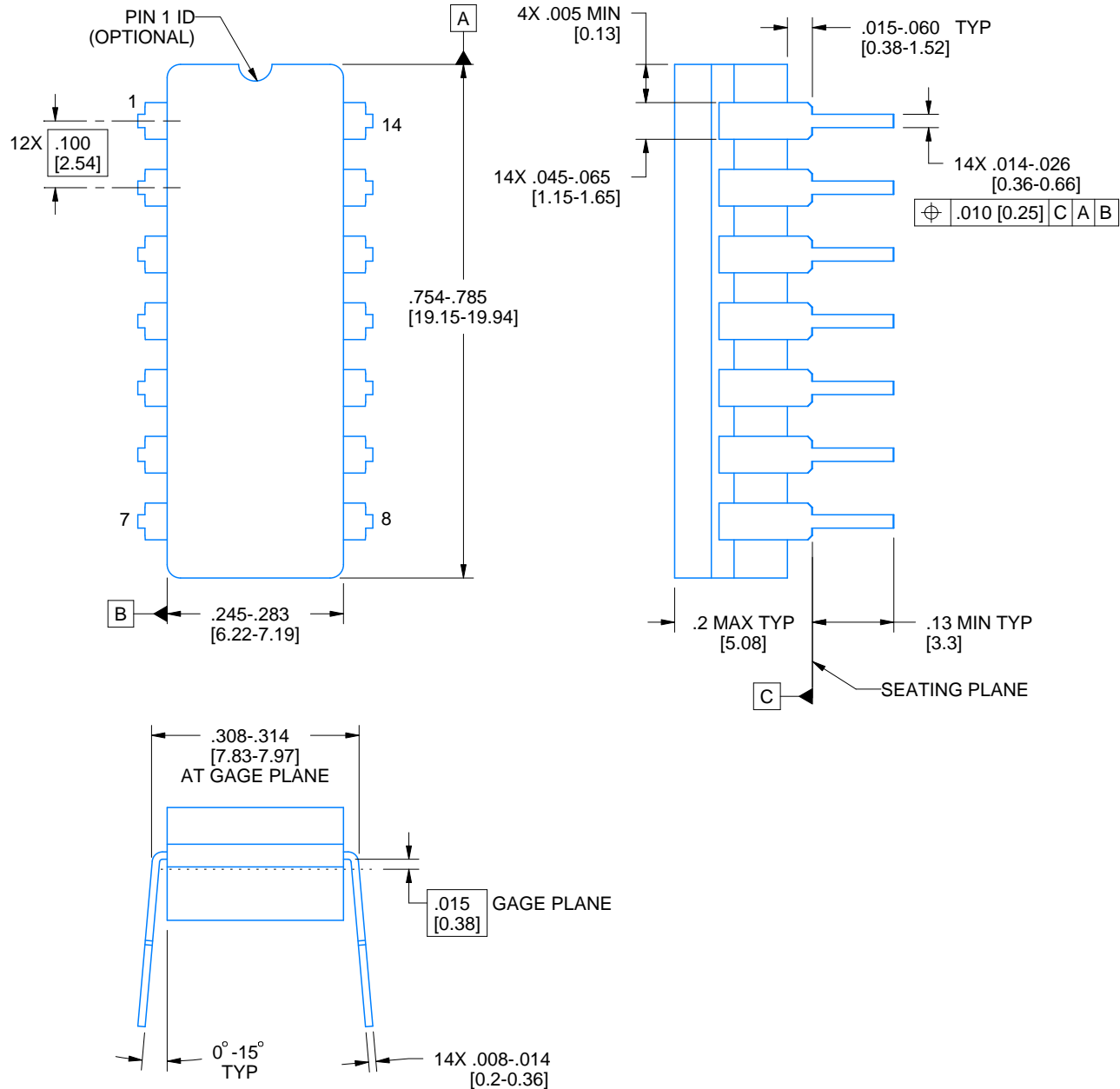
4214771/A   05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

TEXAS INSTRUMENTS

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(.300) TYP
[7.62]

SEE DETAIL A

SEE DETAIL B

1

14

12X (.100)
[2.54]

SYMM
₵

14X (Ø .039)
[1]

7

8

SYMM
₵
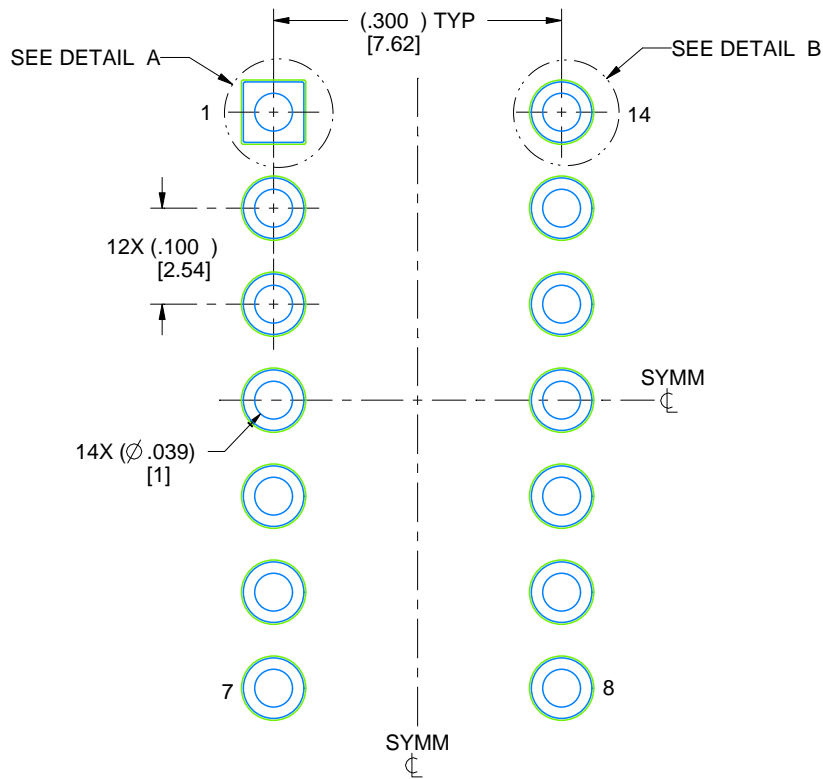
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

.002 MAX
[0.05]
ALL AROUND

(.063)
[1.6]

SOLDER MASK
OPENING

METAL

(R.002) TYP
[0.05]

DETAIL A
SCALE: 15X

METAL

(Ø .063)
[1.6]

SOLDER MASK
OPENING

.002 MAX
[0.05]
ALL AROUND

DETAIL B
13X, SCALE: 15X
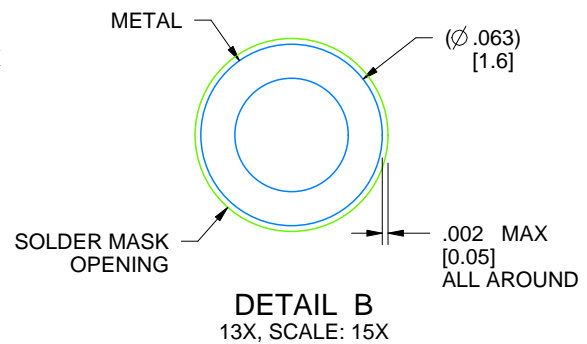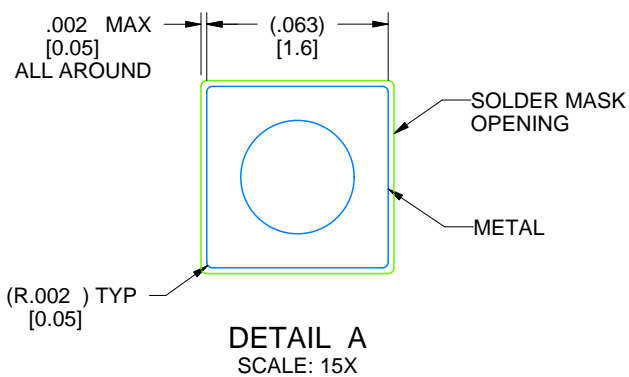
4214771/A 05/2017

D (R−PDSO−G14) PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)
/C\

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)   /D\
0.150 (3,80)

Pin 1
Index Area
1   7

0.050 (1,27)   0.020 (0,51)
                      0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)
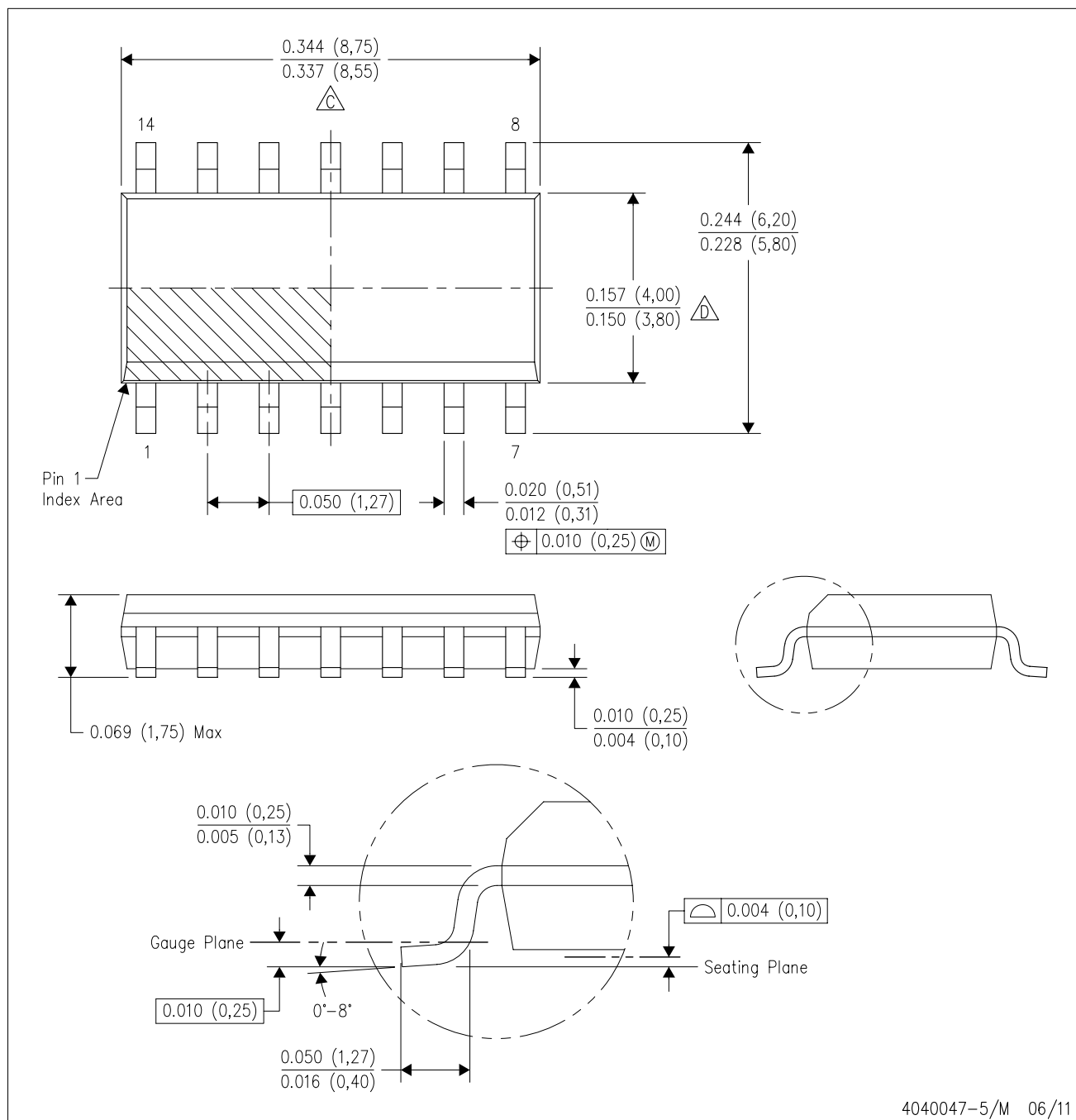
4040047−5/M 06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
      /C\ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
           not exceed 0.006 (0,15) each side.
      /D\ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AB.

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INSTRUMENTS**
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D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

←12x1,27

←14x0,55

←12x1,27

14x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

←0,60

1,55

←0.07
All Around

4211283−3/E   08/12
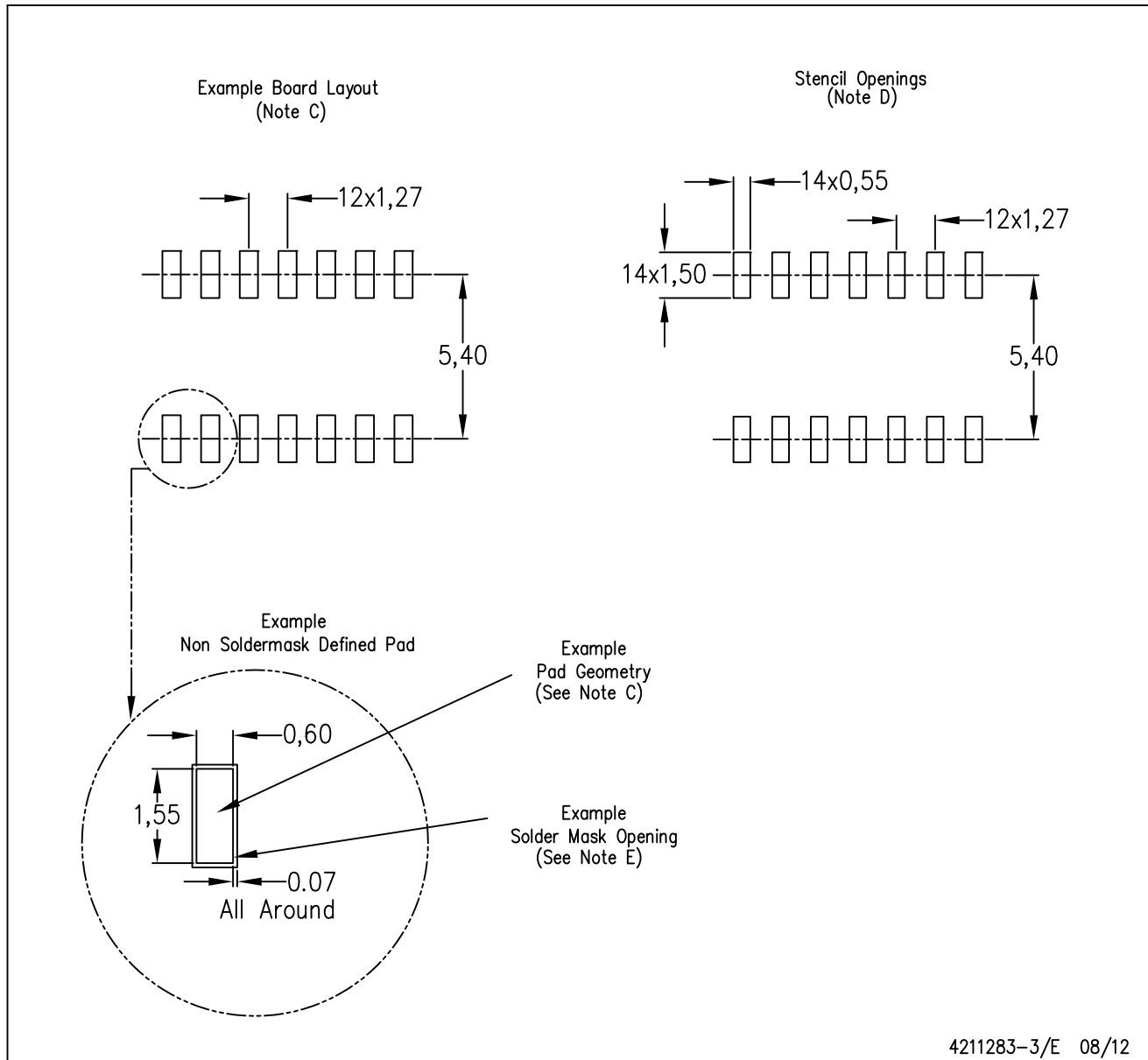
NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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N (R−PDIP−T**)

16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE
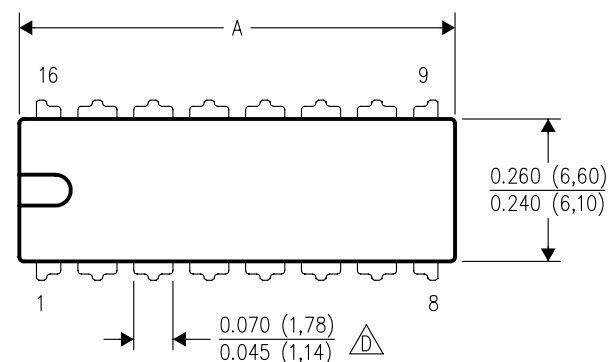
DIM / PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) △D

0.045 (1,14) / 0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX
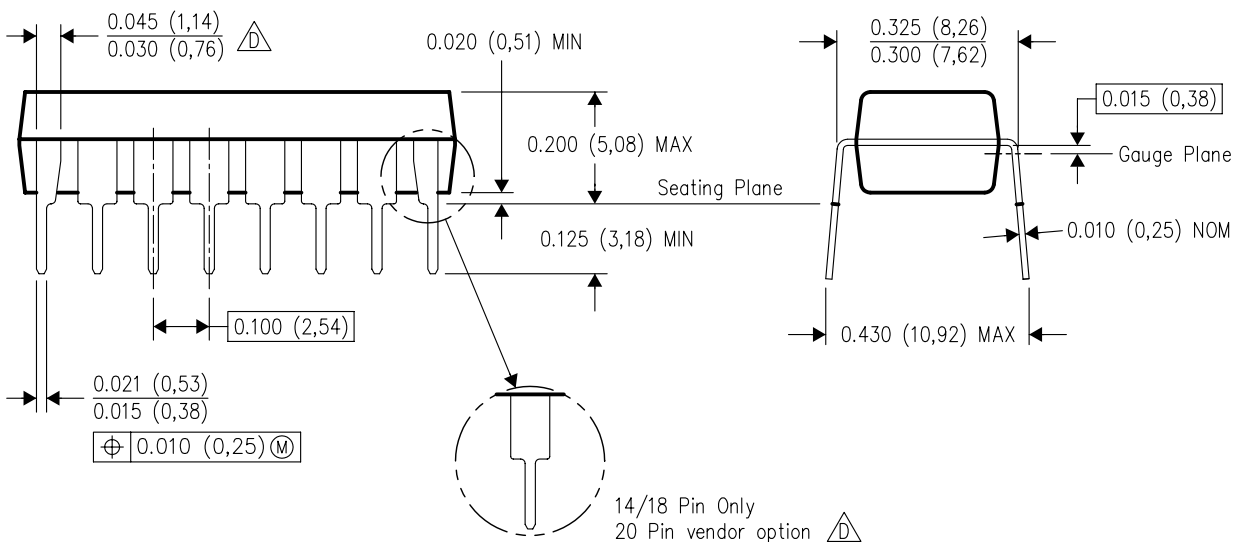
4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         △C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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