POWER MANAGEMENT IC FOR DIGITAL SET TOP BOXES

FEATURES

- Wide Input Supply Voltage Range (10.8 V - 22 V)
- One Adjustable PWM Buck Controller
  - 10.8-V - 22-V Input Voltage Range
  - 3.3-V - 6.1-V Output Voltage Range
  - 500kHz switching frequency
  - Type III Compensation
  - Programmable Current Limit
- Two Adjustable Step-Down Converter with Integrated Switching FETs:
  - 4.75-V - 5.5-V Input
  - 0.9-V-3.3-V Output Voltage Range
  - 3-A Output Current
  - 1-MHz Switching Frequency
  - Voltage Scaling Option
  - Type III Compensation
- Two 100-mΩ, 0.5-A (TPS65230) 1-A (TPS65231) USB Switches with Over Current Protection and Open-Drain Fault Pin
- Early Supply Failure Flag (Open Drain Output) is Set when Input Voltage Drops Below 9.3 V
- Early Temperature Warning Flag (Open Drain Output) is Set if Temperature Approaches Shut-Down Threshold
- Supply Voltage Supervisor Circuit with Two Monitor Inputs and Open Drain Output
- Parallel I/O or I^2C Control with User Selectable Address
- Advanced Fault Detection and Output Voltage Adjustment Options in I^2C Mode
- Pull-Up Current Sources on Buck Enable Pins for Accurate Start-Up Timing Control with Preset Default
- Over Current Protection on All Rails
- Thermal Shutdown to Protect Device During Excessive Power Dissipation
- Thermally Enhanced Package for Efficient Heat Management (48-pin HTSSOP)

APPLICATIONS

- Digital Set Top Boxes
- xDSL & Cable Modems
- DVD Players
- Home Gateway and Access Point Networks
- Wireless Routers

DESCRIPTION/ORDERING INFORMATION

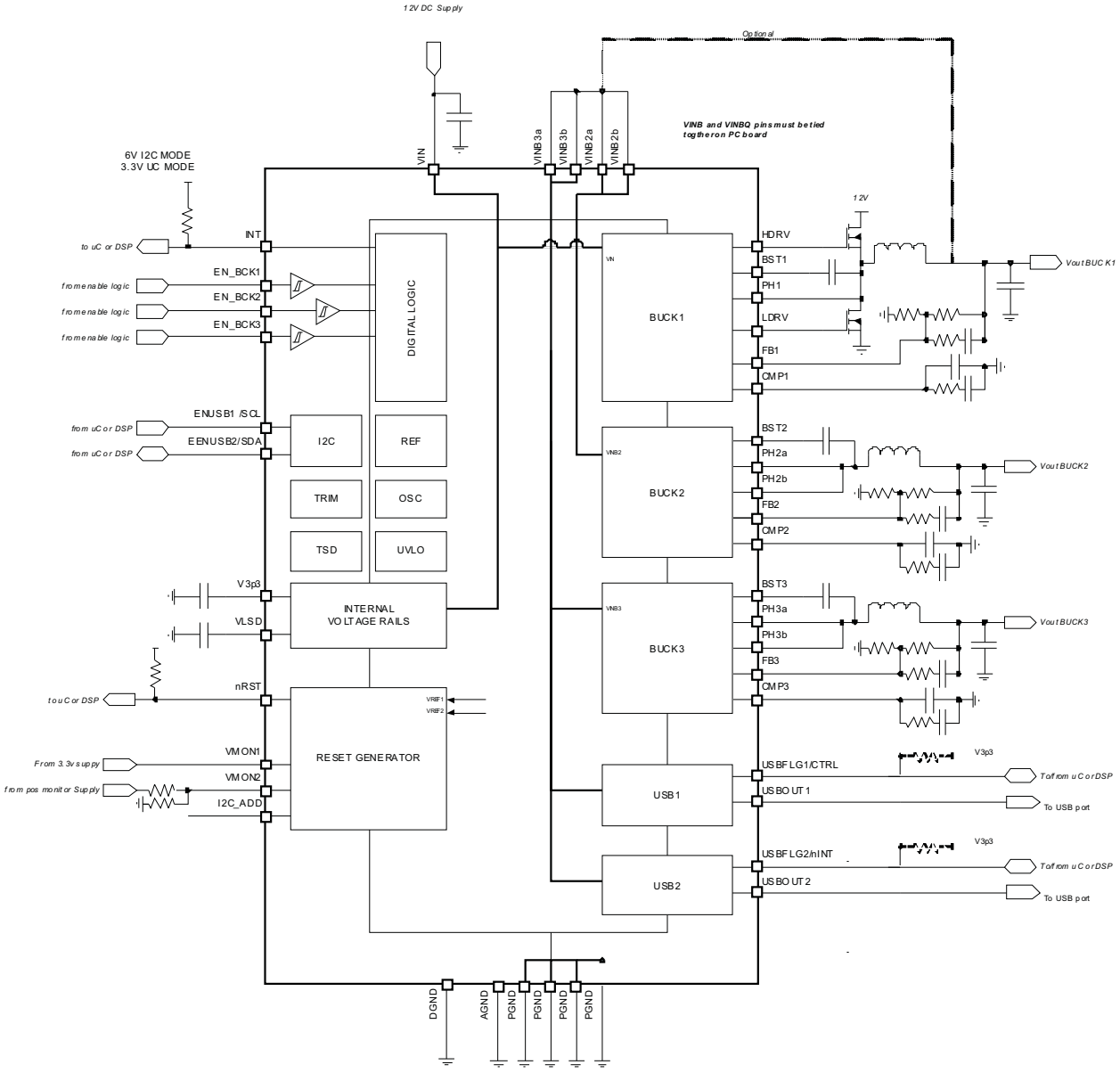
The TPS652x provides one PWM buck controller, two adjustable, synchronous buck regulators, two independent USB power switches and a supply voltage supervisor (SVS) to provide main power functions for satellite set top boxes, xDSL and cable modem applications operating off a single 12- to 22-V supply.

The SMPS have integrated switching FETs for optimized power efficiency and reduced external component count. Each USB switch provides up to 0.5-A (TPS65230) or 1-A (TPS65231) of current as required by downstream USB devices. All power blocks have thermal and over current/short circuit protection.

The SVS provides two inputs for monitoring positive supply rails. The active-low open-drain output remains low for at least 180 ms after all supply rails rise above their rising edge threshold. Threshold value for VMON1 input is set for monitoring a 3.3-V rail without the need for additional external components. Threshold for VMON2 input is set to 0.8 V and requires resistor dividers on the input to monitor any positive voltage in the system. The nBOR/nHOT open-drain output is pulled low if the input supply drops below 9.3 V or the chip temperature approaches the thermal shutdown limit. This allows the system processor to save critical data and shut down gracefully before the supply fails.

The TPS65230 and TPS65231 can be controlled either through parallel I/Os or through I^2C interface. When the pull-up resistor on the USBFLAG2/nINT pin is connected to a 3.3-V or lower supply the I^2C interface is disabled and the device is controlled through parallel I/O pins only. With the pull-up resistor connected to 6 V the I^2C interface is enabled and the device is controlled by writing to the control registers. Any fault or abnormal operating condition is flagged by the interrupt pin. The interrupt is cleared by reading the status register via the I^2C interface.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 85°C	48-pin (HTSSOP) - DCA	Reel of 2000	TPS65230A2DCAR	TPS65230
			TPS65231A2DCAR	TPS65231

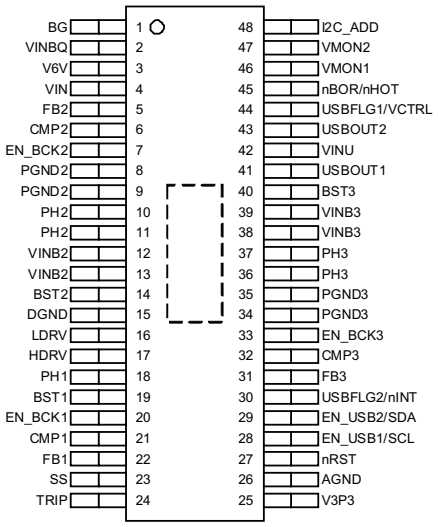
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

TERMINAL FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
BG	1	I	Reference filter pin
VINBQ	2	I	Reference supply for BUCK2 and BUCK3
V6V	3	I	Filter pin for internal voltage regulator (6 V)
VIN	4	I	Input supply for BUCK1 and support circuitry
FB2	5	I	Feedback pin (BUCK2)
CMP2	6	I	Regulator compensation (BUCK2)
EN_BCK2	7	I	Enable pin for BUCK2, active high
PGND2	8, 9		Power ground BUCK2
PH2	10, 11	O	Switching pin (BUCK2)
VINB2	12, 13		Input supply for BUCK2 (must be tied to VINB3, VINBQ)
BST2	14	I	Bootstrap input (BUCK2)
DGND	15		Digital ground. All grounds should be joined together.
LDRV	16	O	Low-side gate drive output (PWM controller)
HDRV	17	O	High-side gate drive output (PWM controller)
PH1	18	O	Switching pin (BUCK1)
BST1	19	I	Bootstrap input (BUCK1)
EN_BCK1	20	I	Enable pin for BUCK1, active high
CMP1	21	I	Regulator compensation (PWM controller)
FB1	22	I	Feedback pin (PWM controller)
SS	23	I	External capacitor for soft start
TRIP	24	I	BUCK1 over current trip point set-up
V3P3	25	I	Filter pin for internal voltage regulator (3.3 V)
AGND	26		Analog ground
nRST	27	O	Reset output (open drain), active low
EN_USB1/SCL	28	I	Enable pin for USB switch 1, active high / Clock input (I^2C enabled).
EN_USB2/SDA	29	I	Enable pin for USB switch 2, active high / Data input (I^2C enabled)
USBFLAG2/nINT	30	I/O	USB2 fault flag / Interrupt pin
FB3	31	I	Feedback pin (BUCK3)
CMP3	32	I	Regulator compensation (BUCK3)
EN_BCK3	33	I	Enable pin for BUCK3, active high
PGND3	34, 35		Power ground BUCK3
PH3	36, 37	O	Switching pin (BUCK3)
VINB3	38, 39	I	Input supply for BUCK3 (must be tied to VINB2, VINBQ)
BST3	40	I	Bootstrap input (BUCK3)
USBOUT1	41	O	USB switch output (channel1)
VINU	42	I	Input supply for USB switches
USBOUT2	43	O	USB switch output (channel2)
USBFLG1/VCTRL	44	I/O	USB1 fault flag, active low, open drain / Voltage control pin for BUCK2 (I^2C enabled)
nBOR/nHOT	45	I/O	Brownout and hot warning, active low, open drain
VMON1	46	I	Voltage monitor input (3.3 V rail)
VMON2	47	I	Voltage monitor input (positive reference)
I2C_ADD	48	I	If grounded, I^2C address is 48h. Tied to V3P3 I^2C address is 49.

DCA HTSSOP PACKAGE
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

	Input voltage range at VIN		–0.3 to 25	V
	Input voltage range at VINB, VINBQ, VINU		–0.3 to 7.0	V
	Voltage range at INT		–0.3 to 7.0	V
	Voltage range at EN_BCK1, EN_BCK2, EN_BCK3, EN_USB1/SCL, EN_USB2/SDA, nRST, USBFLG1/VCTRL2, USBFLG2/VCTRL3		–0.3 to 3.6	V
	Voltage on HDRV, BST1		–0.3 to 31	V
	Voltage on PH1		–0.3 to 24	V
	Voltage on FB1, CMP1, FB2, CMP2, FB3, CMP3		–0.3 to 3.6	V
	Voltage on PH2, PH3, LDRV		–0.3 to 7.0	V
	Voltage on BST2, BST3		–0.3 to 15V	V
	Voltage on VMON1, VMON2, VMON3		–0.3 to 3.6	V
	Output Current BUCK2, BUCK3		3.8	A
	Peak output current		Internally limited	
	ESD rating	Human body model (HBM)	2 k	V
		Charged device model (CDM)	500	
θ_{JA}	Thermal Resistance – Junction to ambient(3)		25	°C/W
	Continuous total power dissipation 55°C(3) no thermal warning		2.6	W
T_J	Operating virtual junction temperature range		0 to 150	°C
T_A	Operating ambient temperature range		0 to 85	°C
T_{STG}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Using JEDEC 51-5 (High K) board. This is based on standard 48DCA package, 4 layers, top/bottom layer: 2 oz Cu, inner layer: 1 oz Cu. Board size: 114.3 x 76.2 mm (4.5 x 3 inches), board thickness: 1.6 mm (0.0629 inch).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Input voltage range at VIN	10.8	12	22	V
	Input voltage range at VINU	4.75		5.5	V
	Input voltage range at VINB	4.75		6.1	
	Voltage range, EN_BCK1, EN_BCK2, EN_BCK3, EN_USB1/SCL, EN_USB2/SDA, nRST, USBFLG1/VCTRL2, USBFLG2/VCTRL3 pins			3.3	V
	Input voltage, nRST pin			3.3	V
	Voltage range, INT pin (I^2C disabled)	5.4		6.6	V
	Voltage range, INT pin (I^2C enabled)			3.3	V
T_A	Ambient operating temperature			50	°C

ELECTRICAL CHARACTERISTICS

VIN = 12 V ±5%, VINB2, VINB3 = 5 V ±5%, VINU = 5 V ±5% T_J = 0°C to 150°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
VIN	Input supply voltage		10.8	12	22	V
VBOR	Brown Out Reset threshold	VIN rising			10.8	V
		VIN falling	9.3			
UVLO VIN	UVLO threshold – VIN (main supply)	VIN rising			10.8	V
		VIN falling	4.7			
UVLO VINB	UVLO threshold – VINB (BUCK2/BUCK3 supply)	VINB rising			4.75	V
		VINB falling	4.25			
UVLO VINU	UVLO threshold – VINU (USB supply)	VINU rising			4.4	V
		VINU falling	3.8			
INPUT CURRENT						
I_{CCQ}	Input supply current	All regulators/USB switches disabled			4	mA
LOGIC INPUT LEVEL (SCL, SDA, INT, VCTRL2, VCTRL3)						
V_{IH}	Input high level		1.2			V
V_{IL}	Input low level				0.4	V
$V_{I2C\_disable}$	I^2C disable voltage (INT)		4			V
BUCK ENABLE INPUTS (EN_BCK1,2,3)						
VEN	Enable threshold			1.2		V
VEN_{HYS}	Enable voltage hysteresis			100		mV
I_{PULLUP}	Pull-up current	t_{EN} = 0.2 ms/nF		6		uA
R_D	Discharge resistor				1	kΩ
t_D	Discharge time	Power-up		5		ms
I^2C ENABLE THRESHOLD (INT pin)						
$VINT_{TH}$	I^2C enable threshold	I^2C enabled if pull-up resistor is connected to a value above threshold		4.8		V
LOGIC OUTPUT LEVEL(SDA, INT, nRST, USBFLG1, USBFLG2)						
OL	Output low level	I_{OUT} = 3 mA through pull-up		0.3	0.4	V
PWM CONTROLLER (BUCK1)						
V_{OUT}	Output voltage range (1)		3.3		6.1	V
PG	Power good threshold	VOUT rising		95		%

(1) Output voltage range is limited by the minimum and maximum duty cycle. V_{OUT}(min) ~ d(min) x V_{INPUT} and V_{OUT}(max) ~ d(max) x V_{INPUT}.

ELECTRICAL CHARACTERISTICS (continued)

VIN = 12 V ±5%, VINB2, VINB3 = 5 V ±5%, VINU = 5 V ±5% T_J = 0°C to 150°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVD	Under voltage detect	VOUT falling		75		%
V_{FB}	Feedback voltage		–2%	0.804	2%	V
LDRV HDRV	High and low side drive voltage	No load		6		V
R_ON_{LDRV}	Low side ON resistance			8		Ω
R_OFF_{LDRV}	Low side OFF resistance			1		Ω
R_ON_{HDRV}	High side ON resistance			20		Ω
R_OFF_{HDRV}	High side OFF resistance			1		Ω
d	Duty cycle (2)		20		80	%
A_{MOD}	Modulator gain			12		
f_{SW}	Switching frequency			500		kHz
I_{TRIP}	Current source for setting OCP trip point	T_A = 25°C		10		µA
TC_{TRIP}	Temperature coefficient of I_{TRIP}			3700		ppm/°C
R_{TRIP}	Current-limit setting resistor		80		250	kW
C_{OUT}	Output capacitance		22 (3)	47		µF
L	Nominal Inductance	Recommended		4.7		µH
BUCK2						
V_{OUT}	Output voltage range (4)		0.9		3.3	V
PG	Power good threshold	V_{OUT} rising		95		%
UVD	Under voltage detect	V_{OUT} falling		75		%
V_{FB}	Feedback voltage		– 2%	0.804	2%	V
I_{OUT}	Output current				3000	mA
η	Efficiency	I_O = 2 A, V_{OUT} = 3.3V		95		%
$R_{DS(ON)}$	Low-side MOSFET On resistance	VIN12V = 12 V		32		mΩ
	High-side MOSFET On resistance			36		
I_{LIMIT}	Switch current limit			5		A
	Current limit accuracy		–30		30	%
$V_{LINEREG}$	Line regulation - DC ΔVOUT/ΔVINB	VINB = 4.75 V - 6.1 V, I_{OUT} = 1 A			1	%
$V_{LOADREG}$	Load regulation - DC ΔVOUT/ΔIOUT	I_{OUT} = 10 – 90% $I_{OUT,MAX}$		0.5		%/A
V_{OUTTOL}	DC set tolerance	Feedback resistor tolerance not included	–2		2	%
d	Duty cycle (5)		15		85	%
A_{MOD}	Modulator gain			5		
f_{SW}	Switching frequency			1		MHz
C_{OUT}	Output capacitance		10 (3)	47		µF
ESR	Capacitor ESR				50	mW
L	Nominal inductance			2.2		µH
BUCK3						
V_{OUT}	Output voltage range (4)		0.9		3.3	V
PG	Power good threshold	VOUT rising		95		%
UVD	Under voltage detect	VOUT falling		75		%

(2) Performance outside these limits is not guaranteed.
(3) Absolute value. User should make allowances for tolerance and variations due to component selection.
(4) Output voltage range is limited by the minimum and maximum duty cycle. V_{OUT}(min) ~ d(min) x V_{INPUT} and V_{OUT}(max) ~ d(max) x V_{INPUT}.
(5) Performance outside these limits is not guaranteed.

ELECTRICAL CHARACTERISTICS (continued)

VIN = 12 V ±5%, VINB2, VINB3 = 5 V ±5%, VINU = 5 V ±5% T_J = 0°C to 150°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	PG glitch rejection			50		µs
V_{FB}	Feedback voltage		–2%	0.804	2%	V
I_{OUT}	Output current				3	A
η	Efficiency	I_O = 2 A, V_{OUT} = 1.2 V		86		%
$R_{DS(ON)}$	Low-side MOSFET On resistance	VIN12V = 12 V		32		mΩ
	High-side MOSFET On resistance			36		
I_{LIMIT}	Switch current limit			5		A
	Current limit accuracy		–30		30	%
$V_{LINEREG}$	Line regulation - DC ΔVOUT/ΔVINB	VINB = 4.75 V - 6.1 V, I_{OUT} = 1000 mA			1	%
$V_{LOADREG}$	Load regulation - DC ΔVOUT/ΔIOUT	I_{OUT} = 10 – 90% $I_{OUT,MAX}$		0.5		%/A
V_{OUTTOL}	DC Set Tolerance	Feedback resistor tolerance not included	–2		2	%
d	Duty cycle(5)		15		85	%
A_{MOD}	Modulator gain			5		
f_{SW}	Switching frequency			1		MHz
C_{OUT}	Output capacitance		10			µF
ESR	Capacitor ESR				50	mW
L	Nominal inductance			2.2		µH
SOFT START (BUCK1, 2, and 3)						
I_{SS}	Soft start current source			2		µA
$V_{SS, MAX}$	Soft start ramp voltage	Ramp end		0.8		V
C_{SS}	Soft start capacitor	t_{SS} = 0.4 ms/nF	2	3.3	5	nF
SSDONE_BK	Deglitch time			2.5		ms
SSDONE_DCH	SS discharge time			500		µS
SUPPLY VOLTAGE SUPERVISOR						
VMON1	Threshold voltage (VMON1)	Supply rising			3.2	V
		Supply falling	3			
		Hysteresis		.05		
VMON2	Threshold voltage (VMON2)	Supply rising		850		mV
		Supply falling		750		
		Hysteresis		20		
$t_{deglitch}$	Deglitch time (both edges)			192		µs
V_{OL}	Reset pin output-low voltage	I_{sink} = 3.2 mA			0.4	V
t_{RP}	Minimum reset period			180		ms
USB POWER SWITCHES						
$R_{DS(on)}$	On resistance			100		mΩ
t_r	Rise time output	VINU = 5.5 V, C_L = 120 mF, V_{OUT} 10% to 90%.			1	ms
t_{on}	Turn-on time	C_L = 100 µF, r_L = 10 Ω			3	ms
t_{off}	Turn-off time	C_L = 100 µF, r_L = 10 Ω			10	ms
I_{OC}	Over Current limit	TPS65230	0.6	0.8	1	A
	Output shorted to ground	TPS65231	1.2	1.6	2	
OC deglitch	Over current deglitch		4	8	15	ms
THERMAL SHUTDOWN						
T_{hot}	Thermal warning			120		°C

ELECTRICAL CHARACTERISTICS (continued)

VIN = 12 V ±5%, VINB2, VINB3 = 5 V ±5%, VINU = 5 V ±5% T_J = 0°C to 150°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{trip}	Thermal S/D trip point			160		°C
T_{hyst}	Thermal S/D hysteresis			20		°C

SUPPLY VOLTAGE SUPERVISOR (SVS)

The supply voltage supervisor monitors two inputs, VMON1 and VMON2, and generates a reset pulse of at least 180-ms length when one or more supplies fall below their respective thresholds. All inputs are deglitched for very short dips on the supplies. The reference values for VMON1 is specified for monitoring a 3.3-V rail without the need of external components. The reference for VMON2 is set to monitor arbitrary supply voltages and require resistor dividers at the inputs.

Please note that the reset signal generated by the SVS is for external use only and has no impact on the power rails or USB switches of the TPS65230 and TPS65231.

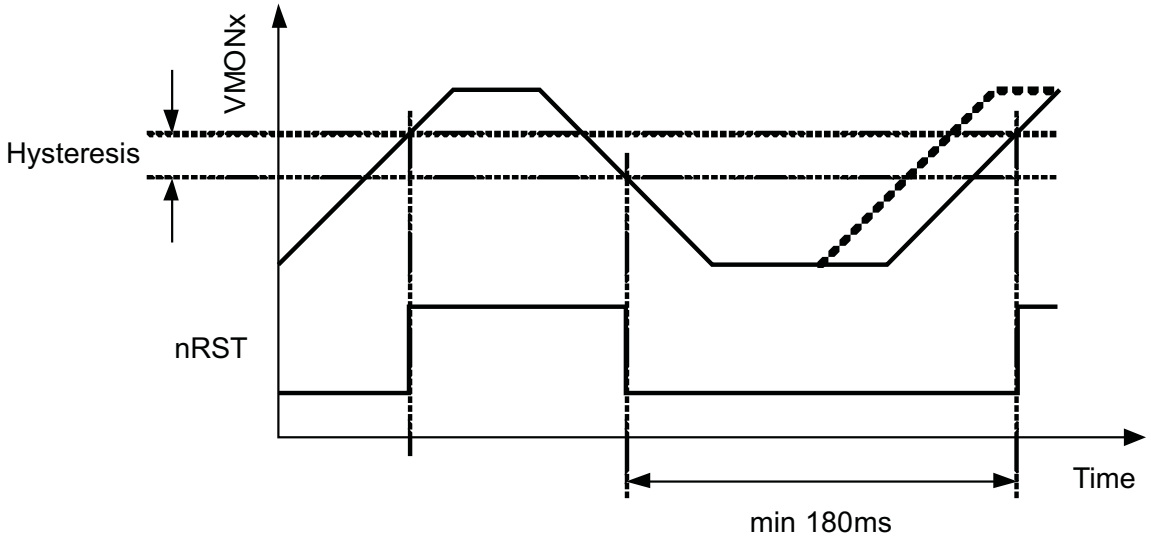


Figure 1. Supply Voltage Supervisor Reset Generation

USB POWER SWITCHES

The TPS65230 and TPS65231 provide two power-distribution switches intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. Gate drive is provided by an internal regulator. Each switch is controlled by a logic enable input or, when I^2C interface is enabled, switches are controlled through EN_USBx bits of the ENABLE register.

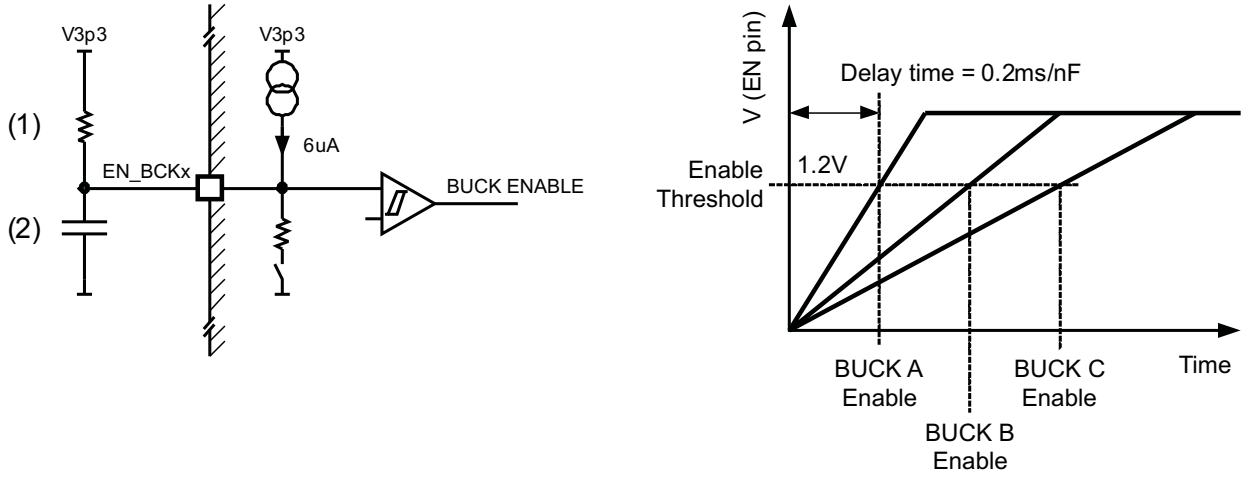
When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the USBFAULTx output low. When continuous heavy overloads and short-circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switches when a thermal warning condition occurs to prevent damage. Recovery from a thermal warning is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present.

POWER-UP SEQUENCING

ON/OFF control and power sequencing of the three buck regulators is controlled through EN_BCK1, EN_BCK2, and EN_BCK3 enable pins. Each pin is internally connected to a 6-µA constant-current source and monitored by a comparator with Schmitt trigger input with defined threshold. Connecting EN_BCKn pin to ground disables BUCKn and connecting EN_BCKn to V3P3 will enable the respective buck without delay. If more than one buck enable pin is connected to V3P3 the default startup sequence is BUCK1, BUCK2, BUCK3 and the minimum startup delay between rails is the soft-start time (typical 1.5 ms) plus 1 ms.

To create a startup-sequence different from the default, capacitors are connected between the EN_BUCKn pins and ground. At power-up the capacitors are first discharged and then charged to V3P3 level by internal current sources (6 µA typical) creating a constant-slope voltage ramp. A regulator is enabled when its EN pin voltage crosses the enable threshold (typical 1.2 V). A delay of 0.2 ms is generated for each 1-nF of capacitance connected to the enable pin. If two enable pins are pulled high while the third regulator is starting up, the default sequence will be applied to enable the remaining two regulators. To override default power-up sequence it is recommended that delay times differ by more than the soft-start time (typical 1.3 ms) plus 1 ms.

In I^2C mode regulators can also be enabled by setting their respective EN bits in the ENABLE register. The same startup-time limitations and arbitration rules apply in I^2C mode as described above.



(1) Connect EN_BCKx pin to V3P3 to follow the default power-up sequence or
(2) Connect a capacitor from EN_BCKx to GND to generate a custom power-up sequence.

Figure 2. Customizing the Power-Up Sequence

OVER CURRENT PROTECTION

Over current protection (OCP) for BUCK1 is achieved by comparing the drain-to-source voltage of the low-side MOSFET to a set-point voltage, which is defined by both the internal current source, I_{TRIP}, and the external resistor connected between the TRIP pin and ground. Over current threshold is calculated as Equation 1.

$$I_{LIM} = \frac{R_{TRIP} \bullet I_{TRIP}}{10 \bullet R_{DS(ON)}} \quad (1)$$

ITRIP has a typical value of 10 µA at 25°C and a temperature coefficient of 3700 ppm/°C to compensate the temperature dependency of the MOS $R_{DS(ON)}$. The TPS65230 and TPS65231 support cycle-by-cycle over current limiting control which means that the controller compares the drain-to-source voltage of the low-side FET to the set-point voltage once per switching cycle and blanks out the next switching cycle if an over-current condition is detected. If in the following cycle over current condition is detected again, the controller blanks out 2, then 4, 8, and up to 16 cycles before turning on the high-side driver again. In an over current condition the current to the load exceeds the current to the output capacitor thus the output voltage will drop, and eventually cross the under

voltage protection threshold and shut down the BUCK controller. Buck 2 and 3 show a similar mode of operation. All converters operate in hiccup mode: Once an over-current is sensed, the controller shuts off the converter for a given time and then tries to start again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case the converter will see another over-current event and shuts-down again repeating the cycle (hiccup) until the failure is cleared.

SOFT START

Soft start (SS) for all three BUCKs is controlled by a single capacitor connected to the SS pin and an internal current source. When one of the BUCKs is enabled, the SS capacitor is pre-charged to the output voltage divided by the feed-back ratio before the internal SS current source starts charging the external capacitor. The output voltage of the BUCK ramps up as the SS pin voltage increased from its pre-charged value to 0.8 V. The soft start time is calculated from the SS supply current (ISS) and the capacitor value and has a typical value of 0.4 ms/nF or 1.3 ms for a 3.3-nF capacitor connected to the SS pin. Before the next rail is enabled, the SS cap is discharged and the SS cycle starts over again.

BROWNOUT MONITOR (BOR)

The TPS65230 and TPS65231 monitor the input supply and issues a warning if the input voltage drops below the BOR threshold of 9.3 V. The nBOR/nHOT pin is pulled low to alarm the host processor of the brown-out condition. nBOR is released after the supply voltage has risen above 10.8 V. nBOR/nHOT pin is also pulled low when the chip temperature rises above the HOT threshold and is released when the chip has cooled off. The purpose of the nBOR/nHOT function is to give the host processor time to finish operations and store data before the system shuts down. Both events, BOR and HOT, are individually flagged in the STATUS1 register. Note that unlike the INT output pin, reading the STATUSx registers has no effect on the state of the nBOR/nHOT pin in I^2C mode. nBOR/nHOT depends only of the input voltage and temperature condition.

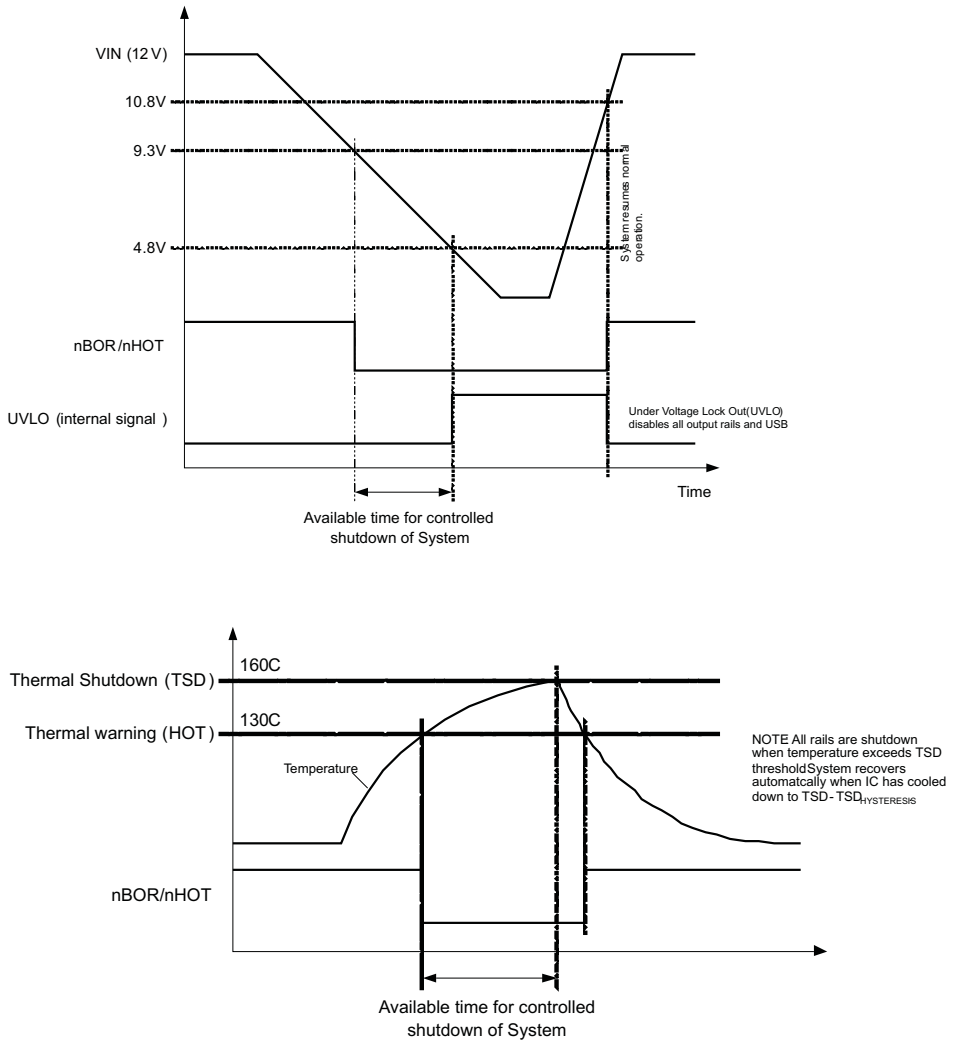


Figure 3. Brownout Monitoring

UNDER VOLTAGE LOCKOUT (UVLO)

TPS65230 and TPS65231 monitors VIN, VINB, and VINU pin voltages and will disable one or more power paths depending on the current use condition:

- If VIN drops below 9.3 V, both USB power paths are disabled and the nBOR/nHOT output pin is pulled low.
- If VIN drops below 4.7 V, BUCK1, 2, and 3 are disabled.
- If VINB drops below 4.25 V and either BUCK2 or BUCK3 are enabled, all three output rails are disabled.
- If VINU drops below 3.9V and either USB1 or USB2 are enabled, both USB switches are disabled.

UVLO state is not latched and the system recovers as soon as the input voltage rises above its respective threshold. All three BUCK_ENx pins are discharged and remain discharged during UVLO to ensure proper power sequencing when the system recovers.

In I^2C mode the EN_BUCKx and EN_USBx bits of the ENABLE register are reset in an UVLO event and interrupt is issued. To re-enable the output supplies, the respective EN_BUCKx bits have to be set through the I^2C interface or the BUCK_ENx pins have to be pulled high. To re-enable the USB power switches in I^2C mode, the EN_USBx bits of the ENABLE register have to be set through the I^2C interface.

THERMAL SHUTDOWN (TSD)

TPS65230x monitors junction temperature and will disable all power paths (BUCK1-3, USB1 and 2) if junction temperature rises above the specified trip point. nBOR/nHOT pin will be pulled low if the temperature approaches the TSD trip point within 40°C. In I^2C mode the device will also issue an interrupt and set the HOT bit in STATUS1 register. The system recovers as soon as the temperature falls below the falling-edge trip temperature. All three BUCK_ENx pins are discharged and remain discharged during TSD to ensure proper power sequencing when the system recovers.

In I^2C mode the EN_BUCKx and EN_USBx bits of the ENABLE register are reset in a TSD event and interrupt is issued. To re-enable the output supplies the respective EN_BUCKx bits have to be set through the I^2C interface or the BUCK_ENx pins have to be pulled high. To re-enable the USB power switches in I^2C mode, the EN_USBx bits of the ENABLE register have to be set through the I^2C interface.

LOOP COMPENSATION

All three BUCKs are voltage mode converters designed to be stable with ceramic capacitors. Refer to Component Selection Procedure section for calculating feedback components.

3.3-V REGULATOR

The TPS6532x has a built-in 3.3-V regulator for powering internal circuitry. The 3.3-V rail can also be used for enabling the BUCK regulators and/or the USB switches, but is not intended for supplying any other external circuitry. For light loading of this rail during stand-by operation consult TI FAE.

6-V REGULATOR

The TPS6532x has a built-in 6-V regulator for powering internal circuitry. The 6-V rail can also be used for enabling I^2C functionality by connecting the pull-up resistor on the USBFLG2/nINT pin to V6V but is not intended for supplying any other external circuitry. For light loading of this rail during stand-by operation consult TI FAE.

USER SELECTABLE SERIAL INTERFACE

TPS65230 and TPS65231 feature an I^2C slave interface which can be enabled or disabled by the user and offers advanced control and diagnostic features. I^2C control is enabled when the pull-up resistor on the USBFLG2/nINT pin is connected to a supply voltage > 4.5 V and is disabled otherwise. When disabled, BUCK1, 2, 3, and USB1, 2 are controlled through their respective enable pins. When the I^2C interface is enabled, USB1 and USB2 are controlled through the serial interface and BUCK1, 2, and 3 are controlled either through the serial interface or their respective enable pins. In addition, the USBFLG1/VCTRL pin is reconfigured when I^2C is enabled to offer output voltage control for BUCK2 and BUCK3.

I^2C operation offers brownout and thermal shutdown warning, thermal shut down flag, power-good and under-voltage indicator for BUCK1-3 and USB fault indicator for both USB switches. Whenever a fault is detected, the associated status bit in the STATUS1 and 2 registers are set and the INT pin is pulled low. Reading of the STATUS1 and 2 registers resets the flag bits and INT pin is released after all flags have been reset. Note that in I^2C mode the nINT pin is active high with voltage swing of > 3.3 V. To invert the signal and shift the voltage level down to an I/O compatible level, connect the circuit shown in Figure 5 to the USBFL2/nINT pin.

INT Dependent Device Pin Configuration

PIN NO.	DEVICE PIN	USBFLG2/INT CONNECTED TO V6V(1)	USBFLG2/INT CONNECTED TO 3.3V(1)
30	USBFLG2/nINT	nINT	Error flag for USB switch 2
28	EN_USB1/SCL	SCL (Clock)	Enable pin for USB switch 1
29	EN_USB2/SDA	SDA (Data)	Enable pin for USB switch 2
44	USBFLG1/VCTRL	Voltage control input for BUCK2 and 3	Error flag for USB switch 1

(1) Via pull-up resistor

I²C operation also offers output voltage adjustment options for BUCK2 and BUCK3. This is feature is useful to reduce power dissipation in the system by lowering the supply voltages when the system is in idle state. Output voltage can be scaled down by 5, 10 and 15% depending on the VBCKn[1:0] bit settings in the VADJUST register. Settings are activated when the USBFLG1/VCTRL pin is pulled high and are deactivated when the pin is pulled low. This allows for fast output voltage transition without involvement of the I²C interface. Alternatively the settings can be activated by setting the the VCTRLx bits of the ENABLE register.

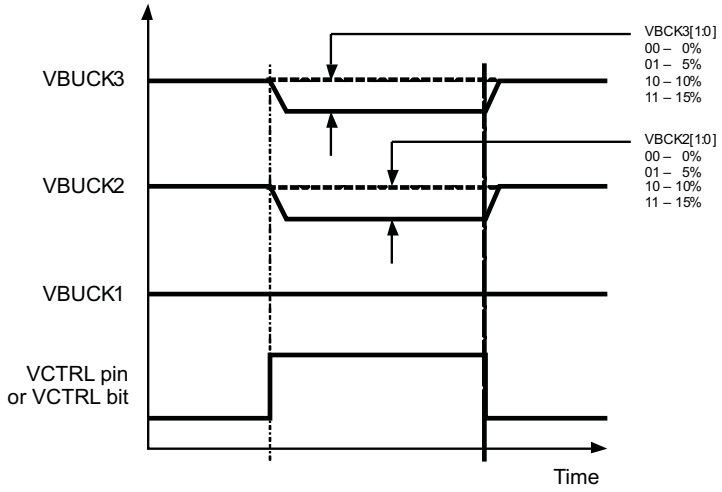


Figure 4. BUCK2 and BUCK3 Output Voltages

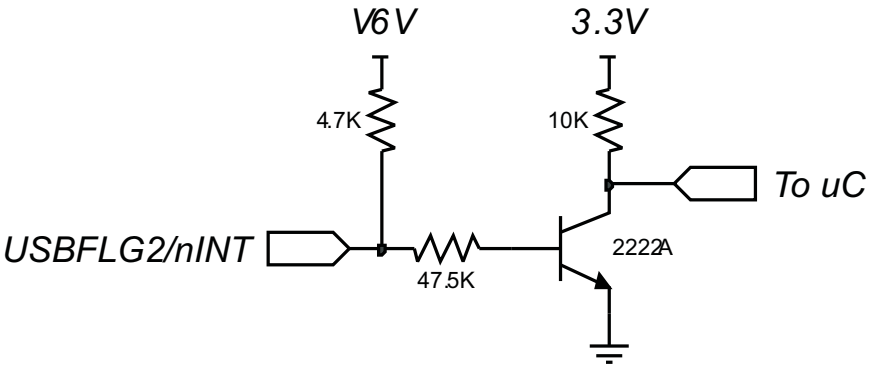


Figure 5. Circuit for Level-Shifting and Inverting nINT Signal

I²C BUS OPERATION

The TPS65230 hosts a slave I²C interface that supports data rates up to 400 kbit/s and auto-increment addressing and is compliant to I²C standard 3.0.

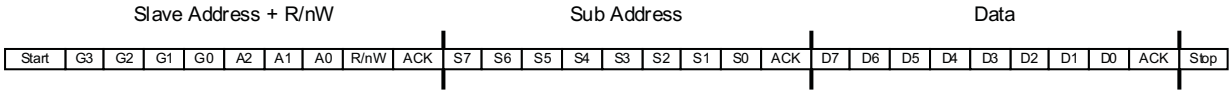


Figure 6. Subaddress in I²C Transmission

Start — Start condition

G(3:0) — Group ID: 1001

A(2:0) — Device address: 000

R/nW — Read/not write select bit

ACK — Acknowledge

S(7:0) — Subaddress: defined per register map

D(7:0) — Data: data to be loaded into the device

Stop — Stop condition

The I^{2}C Bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the slave terminals. Each device has an open drain output to transmit data on the serial data line. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission is initiated with a start bit from the controller as shown in Figure 7. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device will receive serial data on the SDA input and check for valid address and control information. If the appropriate group and address bits are set for the device, then the device will issue an acknowledge pulse and prepare the receive subaddress data. Subaddress data is decoded and responded to as per the Register Map section of this document. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. The I^{2}C interface will auto-sequence through register addresses, so that multiple data words can be sent for a given I^{2}C transmission. Reference Figure 7.

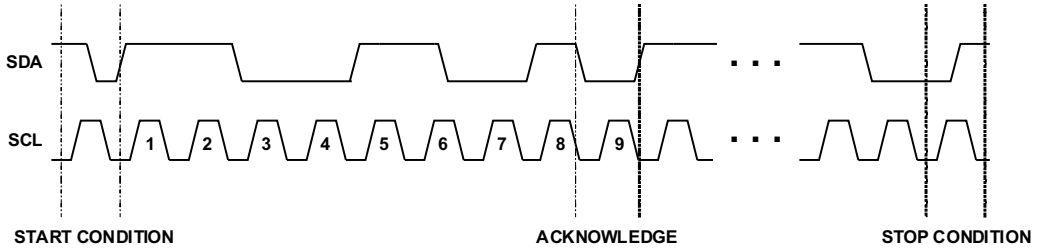


Figure 7. I^{2}C Start / Stop / Acknowledge Protocol

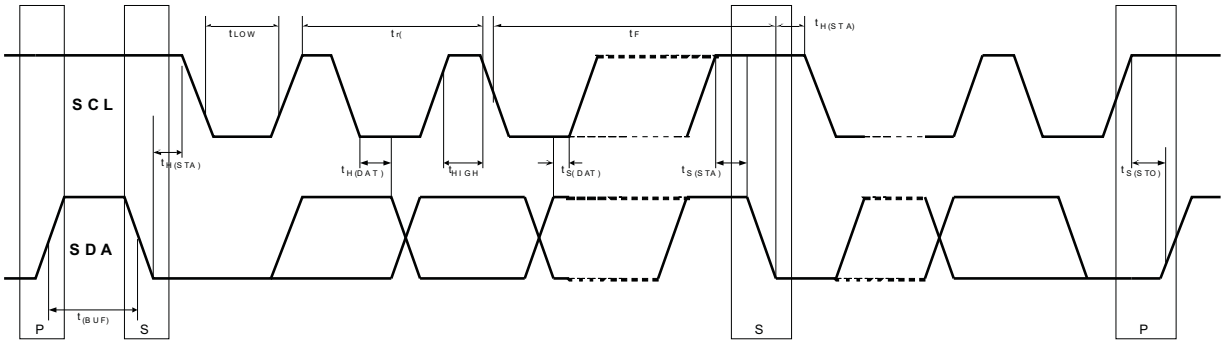


Figure 8. I^{2}C Data Transmission Timing

DATA TRANSMISSION TIMING

VBUS = 3.6 V ±5%, T_A = 25 °C, C_L = 100 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	Serial clock frequency	SCL = 100 kHz		100	kHz
		SCL = 400 kHz		400	
$t_{(BUF)}$	Bus free time between stop and start condition	SCL = 100 kHz	4.7		µs
		SCL = 400 kHz	1.3		
$t_{(SP)}$	Tolerable spike width on bus	SCL = 100 kHz		50	ns
		SCL = 400 kHz			
t_{LOW}	SCL low time	SCL = 100 kHz	4.7		µs
		SCL = 400 kHz	1.3		
t_{HIGH}	SCL high time	SCL = 100 kHz	4		µs
		SCL = 400 kHz	0.6		
$t_{S(DAT)}$	SDA → SCL setup time	SCL = 100 kHz	250		ns
		SCL = 400 kHz	100		
$t_{S(STA)}$	Start condition setup time	SCL = 100 kHz	4.7		µs
		SCL = 400 kHz	0.6		
$t_{S(STO)}$	Stop condition setup time	SCL = 100 kHz	4		µs
		SCL = 400 kHz	0.6		
$t_{H(DAT)}$	SDA → SCL hold time	SCL = 100 kHz		3.45	µs
		SCL = 400 kHz		0.9	
$t_{H(STA)}$	Start condition hold time	SCL = 100 kHz	4		µs
		SCL = 400 kHz	0.6		
$t_{r(SCL)}$	Rise time of SCL signal	SCL = 100 kHz		1000	ns
		SCL = 400 kHz		300	
$t_{f(SCL)}$	Fall time of SCL signal	SCL = 100 kHz		300	ns
		SCL = 400 kHz		300	
$t_{r(SDA)}$	Rise time of SDA signal	SCL = 100 kHz		1000	ns
		SCL = 400 kHz		300	
$t_{f(SDA)}$	Fall time of SDA signal	SCL = 100 kHz		300	ns
		SCL = 400 kHz		300	

THERMAL MANAGEMENT AND SAFE OPERATING AREA

Total power dissipation inside TPS6523x is limited not to exceed the maximum allowable junction temperature of 150°C. The maximum allowable power dissipation is a function of the thermal resistance of the package (θ_{JA}) and ambient temperature. θ_{JA} itself is highly dependent on board layout. The maximum allowable power inside the IC for operation at maximum ambient temperature without exceeding the temperature warning flag using the JEDEC High-K board is calculated as Equation 3.

$$\Delta T = \theta_{JA} \bullet P \tag{2}$$

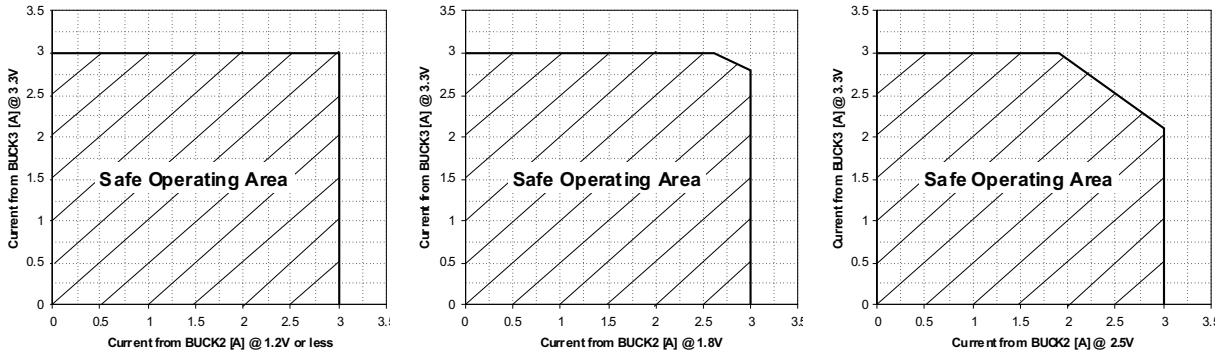
$$P_{MAX} = \frac{T_{MAX} - T_{ambient}}{\theta_{JA}} = \frac{120°C - 55°C}{25°C/W} \approx 2.6\ W \tag{3}$$

For different PCB layout arrangements the thermal resistance (θ_{JA}) will change as the following table shows.

BOARD TYPE	STACK-UP	θ_{JA}
8" x 10" FR4 PCB, four layers	1.5-oz Cu, 60% Cu coverage top layer, 80% Cu coverage bottom layer, no airflow 0.5-oz 30%Cu coverage inner layers	29
8” x 10” FR4 PCB, two layers	1-oz Cu, 20% Cu coverage top layer, 90% Cu coverage bottom layer, no airflow	44

A minimum of two layers of 1-oz Cu with 20% Cu coverage on the top and 90% coverage on the bottom and the use of thermal vias to connect the thermal pad to the bottom layer is recommended. Note that the maximum allowable power inside the device will depend on the board layout. For recommendations on board layout for thermal management using TPS6523x consult your TI field application engineer.

In the example shown above the maximum allowable power dissipation for the IC has been calculated. This figure includes all heat sources inside the device including the power dissipated in BUCK1, BUCK2, BUCK3, USB switches, and all supporting circuitry. Power dissipated in BUCK1, USB switches (500 mA full load) , and all supporting circuitry is approximately 0.4 W and almost independent of the application. Power dissipated in BUCK2 and BUCK3 depends on the output voltage, output current, and efficiency of the switching converters. The following examples of safe operating area assume 90% efficiency for BUCK2 and BUCK3, 3.3-V output from BUCK3 and 1.2-V, 1.8-V, and 2.5-V output from BUCK2, respectively.



For any voltage / current comination inside the shaded area, the dissipated power inside the chip is below the allowable maximum. The examples assume $T_{ambient}$ < 60°C, η = 90% and θ_{JA} < 44°C/W.

Figure 9. Examples of Thermal Safe Operating Area for V(BUCK3) = 3.3 V and V(BUCK1) = 1.2 V, 1.8 V and 2.5 V, Respectively

COMPONENT SELECTION PROCEDURE

The following example illustrates the design procedure for selecting external components for the three buck converters. The example focuses on BUCK1 but the procedure can be directly applied to BUCK2 and 3 as well. The design goal parameters are given in the table below. A list of symbol definitions is found at the end of this section. For this example the schematic in Figure 10 will be used.

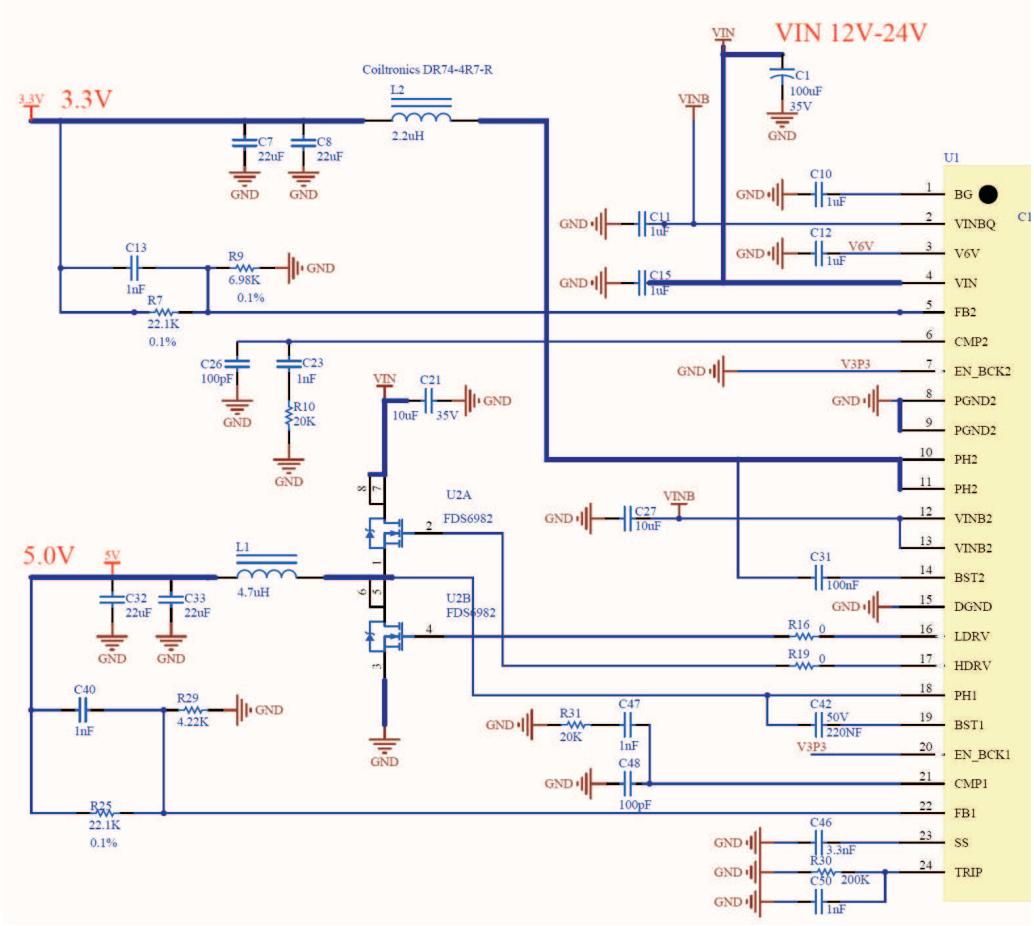


Figure 10. Sample Schematic for TPS6523x Showing Components Relevant to BUCK1

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage		10.8	12	13.2	V
$V_{IN\ RIPPLE}$	Input voltage ripple	$I_{OUT,\ BUCK1}$ = 6 A			60	mV
V_{OUT}	Output Voltage		4.75	5	5.25	V
	Line regulation	V_{IN} = 10.8 V to 13.2 V		25		mV
	Load regulation	$I_{OUT,\ BUCK1}$ = 0 A to 6 A		25		mV
$V_{OUT\ RIPPLE}$	Output ripple	$I_{OUT,\ BUCK1}$ = 6 A			50	mV
V_{TRANS}	Transient deviation	$I_{OUT,\ BUCK1}$ = 2 A to 6 A		125		mV
I_{OUT}	Output current	V_{IN} = 10.8 V to 13.2 V	0		6	A
f_{SW}	Switching frequency			500		kHz

INDUCTOR SELECTION

For BUCK1 the recommended inductor value is 4.7 µH and for BUCK2 and 3 it is 2.2 µH. These values will provide a good balance between ripple current, efficiency, loop bandwidth and inductor cost. The inductor is typically sized for < 30% peak-to-peak ripple current (I_{RIPPLE}). Given this target ripple current, the required inductor size is calculated by Equation 4.

$$L = \frac{V_{IN(MAX)} - V_{OUT}}{0.3 \bullet I_{OUT}} \bullet \frac{V_{OUT}}{V_{IN(MAX)}} \bullet \frac{1}{f_{SW}} \quad (4)$$

Solving Equation 4 with $V_{IN(MAX)}$ = 13.2 V, an inductor value of 3.5 µH is obtained. A standard value of 4.7 µH is selected, resulting in 1.25-A peak-to-peak ripple. The RMS current through the inductor is approximated by Equation 5.

$$I_{L(RMS)} = \sqrt{\left(I_{L(avg)}^{2} + \frac{1}{12}(I_{RIPPLE})^{2}\right)} = \sqrt{(I_{OUT})^{2} + \frac{1}{12}(I_{RIPPLE})^{2}} \quad (5)$$

Using Equation 5, the maximum RMS current in the inductor is about 6.01 A.

OUTPUT CAPACITOR SELECTION

The selection of the output capacitor is typically driven by the output load transient response requirement. The output capacitance (base) proposed is 2 x 22 µF (or 4 X 10 µF or 1 x 47 µF) ceramic, providing a good balance between ripple, cost and performance. Extra caps added should be electrolyte or far from base cap to have considerable amount of ESR and not to affect compensation.

Equation 6 and Equation 7 estimate the output capacitance required for a given output voltage transient deviation.

$$C_{OUT(MIN)} = \frac{I_{TRAN(MAX)}^{2} \bullet L}{(V_{IN(MIN)} - V_{OUT}) \bullet V_{TRAN}} \quad \text{when } V_{IN(MIN)} < 2 \bullet V_{OUT} \quad (6)$$

$$C_{OUT(MIN)} = \frac{I_{TRAN(MAX)}^{2} \bullet L}{V_{OUT} \bullet V_{TRAN}} \quad \text{when } V_{IN(MIN)} > 2 \bullet V_{OUT} \quad (7)$$

For this example, Equation 7 is used in calculating the minimum output capacitance.

Based on a 4-A load transient with a maximum 125-mV deviation (2.5% of set voltage), a minimum of 120-µF output capacitance is required. We choose two 22-µF ceramic capacitors and two electrolytic 47 µF in parallel for a total capacitance of 138 µF.

The output ripple is divided into two components. The first is the ripple generated by the inductor ripple current flowing through the output capacitor's capacitance, and the second is the voltage generated by the ripple current flowing in the output capacitor's ESR. The maximum allowable ESR is then determined by the maximum ripple voltage and is approximated by Equation 8.

$$ESR_{MAX} = \frac{V_{RIPPLE(total)} - V_{RIPPLE(cap)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(total)} - \left(\frac{I_{RIPPLE}}{C_{OUT} \bullet f_{SW}}\right)}{I_{RIPPLE}} \quad (8)$$

Based only on the 138-µF of capacitance, 1.25-A ripple current, 500-kHz switching frequency and a design goal of 50-mV ripple voltage (1% of set voltage), we calculate a capacitive ripple component of 18 mV and a maximum ESR of 25 mΩ. The X5R ceramic capacitors selected provide significantly less than 25-mΩ of ESR.

PEAK CURRENT RATING OF THE INDUCTOR

With output capacitance known, it is now possible to calculate the charging current during start-up and determine the minimum saturation current rating of the inductor. The start-up charging current is approximated by Equation 9.

$$I_{CHARGE} = \frac{V_{OUT} \bullet C_{OUT}}{T_{SS}} \quad (9)$$

Using the TPS65230 and TPS65231's recommended 1.3-ms soft-start time, C_{OUT} = 188 µF and V_{OUT} = 5 V, I_{CHARGE} is found to be 720 mA. The peak current rating of the inductor is now found by Equation 10.

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{1}{2} I_{RIPPLE} + I_{CHARGE} \quad (10)$$

For this example an inductor with a peak current rating of 7.3 A is required. Note however that the inductor will need to withstand the current limit figure without a major reduction of its rated inductance.

INPUT CAPACITOR SELECTION

The input voltage ripple is divided between capacitance and ESR. For this design, $V_{RIPPLE(cap)}$ = 60 mV (0.5% of supply) and $V_{RIPPLE(ESR)}$ = 30 mV (0.25% of supply). The minimum capacitance and maximum ESR are estimated by Equation 11 and Equation 12.

$$C_{IN(MIN)} = \frac{I_{LOAD} \bullet V_{OUT}}{V_{RIPPLE(cap)} \bullet V_{IN} \bullet f_{SW}} \quad (11)$$

$$ESR_{MAX} = \frac{V_{RIPPLE(ESR)}}{I_{LOAD} + \frac{1}{2} I_{RIPPLE}} \quad (12)$$

For this design, C_{IN} > 8 µF and ESR < 4 mΩ. The RMS current in the output capacitors is estimated by Equation 13.

$$I_{RMS(CIN)} = I_{IN(RMS)} - I_{IN(avg)} = \sqrt{\left((I_{OUT})^2 + \frac{1}{12}(I_{RIPPLE})^2\right) \bullet \frac{V_{OUT}}{V_{IN}}} - \frac{V_{OUT} \bullet I_{OUT}}{V_{IN}} \quad (13)$$

With $V_{IN} = V_{IN(MAX)}$, the input capacitors must support a ripple current of 1.4-A RMS. It is important to check the DC bias voltage de-rating curves to ensure the capacitors provide sufficient capacitance at the working voltage. Typically a 10-µF capacitor per converter is used. These capacitors should be placed as close as possible to the VINB2 and VINB3 pins (BUCK2 and BUCK3) and to the external MOSFET arrangement for BUCK1.

BOOTSTRAP CAPACITOR

To ensure proper charging of the high-side MOSFET gate, limit the ripple voltage on the bootstrap capacitor to < 5% of the minimum gate drive voltage.

$$C_{BOOST} = \frac{20 \bullet Q_{GS,\ HSD}}{V_{IN(MIN)}} \quad (14)$$

Based on the FDS6982 MOSFET with a maximum total gate charge of 26 nC, calculate a minimum of 80-nF of capacitance. A standard value of 220 nF is selected for BUCK1 and 100 nF for BUCK2.

SHORT CIRCUIT PROTECTION (BUCK1 ONLY)

The TPS65230 and TPS65231 uses the forward drop across the low-side MOSFET during the OFF time to measure the inductor current. The voltage drop across the low-side MOSFET is given by Equation 15.

$$V_{DS} = I_{L(PEAK)} \bullet R_{DSON,\ LSD} \quad (15)$$

When V_{IN} = 10.8 V to 13.2 V, I_{PEAK} = 7.4A for full load (6 A). Using the FDS6982 MOSFET with a $R_{DSON,MAX}$ at T_J = 25°C of 20 mΩ we calculate the peak voltage drop to be 148 mV. Adding a 50% margin to include inductor variations and overload margin, the drop voltage for tip is set at 210 mV. Solving Equation 1 for R_{TRIP} and using I_{TRIP} = 10 µA:

$$R_{TRIP} = R_{DS(ON)} \bullet I_{LIM} \bullet 10^6 \quad (16)$$

We calculate a trip resistor value of 210 kΩ. Place a 1-nF capacitor parallel to R9. Please note that typical FET $R_{DS(ON)}$ is specified at 10 mΩ. Since we used $R_{DSON,MAX}$, for setting the current limit, the actual current flowing through the inductor with a nominal FET can be higher than the peak current of 7.4 A before the current limit kicks in. Make sure that the chosen inductor has the correct peak current capabilities.

SHORT CIRCUIT PROTECTION (BUCK2 AND 3 ONLY)

Current limits for BUCK2 and 3 are internally set to 5 A.

FEEDBACK LOOP DESIGN

For the TPS6523x, the switching frequency and nominal output filter combination have been chosen to be 0.5 MHz 4.7 µH/~40 µF for BUCK1 and 1 MHz 2.2 µH/~40 µF for BUCK2 and 3 respectively. These values were seen as a good compromise between efficiency and small solution size. The bandwidth has been chosen to be around 1/8th - 1/11th of the switching frequency to maximize transient response whilst retaining low noise sensitivity. As indicated before it is required that the output capacitor is ceramic and further that the very low ESR causes it's associated zero to be at or above the bandwidth of the converter.

The control loop for the TPS6523x has an internal mid- to high-frequency zero-pole pair to compensate the resonant pole caused by the output L-C filter. The maximum phase boost occurs at the geometric mean of the pole zero arrangement and therefore aimed to be equal to the desired bandwidth. The pole limits the gain at high frequencies to reduce noise sensitivity and it is about 5 times higher than the zero located at ~45 kHz.

The COMP pin of the buck converters is the output of an integrator Used to get high DC accuracy. The integrator also takes care of any offsets in the zero-pole pair amplifier and the summing comparator inside the device. Also a feed-forward loop is added to the attenuator circuit.

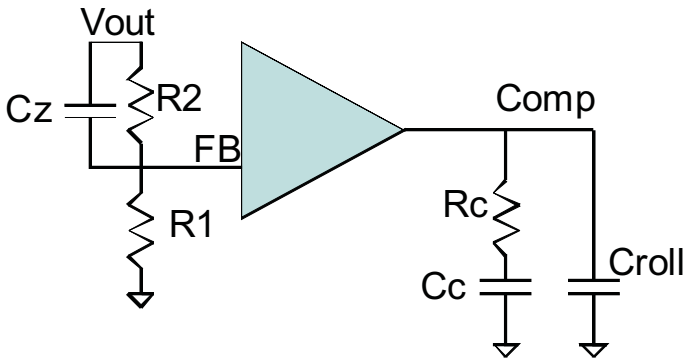


Figure 11. External Compensation Circuit

The procedure to set the integrator values is very simple (see Figure 11):

1. Set the feed-forward circuit making R2 = 20 kΩ, C_Z= 1 nF.
2. Calculate R1 as per output voltage requirement. Select R25 between 10 kΩ and 100 kΩ. For this design select 22.1 kΩ, 0.1% resistor for the upper side of all dividers. Next, R29 Is selected to produce the desired output voltage when V_{FB} = 0.8 V using Equation 17.

$$R29 = \frac{V_{FB} \bullet R25}{V_{OUT} - V_{FB}} \quad (17)$$

   V_{FB} = 0.8 V and R25 = 22.1 kΩ for V_{OUT} = 5.0 V, R25 = 4.209 kΩ. The closest value 4.22 kΩ.
3. Set the integrator values, R_C = 20 kΩ, C_C = 1 nF.
4. Make C_{roll} = 100 pf to roll-off gain at high frequencies.
5. If V_{IN} is ~20 - 24 V use 200 pF for C_{roll} on DCDC1.

Other Components

A 1-µF ceramic capacitor should be connected as close as possible to the following pins:

- BG (pin 1): Bandgap reference
- VIN (pin 4): Bypass capacitor (higher values are acceptable)
- V6V (pin 3): Internal 6 V supply
- V3P3 (pin 25): Internal 3.3 V supply

Register Address Map

REGISTER	ADDRESS (HEX)	NAME	DEFUALT VALUE	DESCRIPTION
0	00	ENABLE	0000 0000	Enable control register
1	01	VADJUST	0000 0000	Voltage adjustment register
2	02	STATUS1	0000 0000	Status bit register
3	03	STATUS2	0000 0000	Status bit register

ENABLE Register (ENABLE), Address - 0X00H

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	VCTRL	EN_BCK1	EN_BCK2	EN_BCK3	EN_USB1	EN_USB2
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME(1)	BIT DEFINITION
VCTRL	Voltage control bit for BUCK2 and BUCK3 0 – Nominal output voltage 1 – Enable voltage adjustment level set by VADJUST register
EN_BCK1	Enable BUCK1 0 – Disabled 1 - Enabled
EN_BCK2	Enable BUCK2 0 – Disabled 1 - Enabled
EN_BCK3	Enable BUCK3 0 – Disabled 1 - Enabled
EN-USB1	Enable USB1 0 – Disabled (OFF) 1 - Enabled
EN_USB2	Enable USB2 0 – Disabled (OFF) 1 – Enabled

(1) Enable bits EN_BCK1, EN_BCK2, and EN_BCK3 are ORed with EN_BCK1, EN_BCK2, and EN_BCK3 enable pins, respectively. To disable a block, EN bit and EN pin must be low.

VADJUST Register (VADJUST), Address - 0X01H

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	Not used	Not used	VBCK2[1:0]		VBCK3[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME(1)	BIT DEFINITION
VBCK2[1:0]	BUCK2 voltage adjustment 00 - Nominal 01 - 5% Decrease 10 - 10% Decrease 11 - 15% Decrease
VBCK3[1:0]	BUCK3 voltage adjustment 00 - Nominal 01 - 5% Decrease 10 - 10% Decrease 11 - 15% Decrease

(1) Voltage adjustment settings for BUCK2 and BUCK3 are effective only when VCTRL pin is pulled high or VCTRL bit of ENABLE register is set to ‘1’.

STATUS Register (STATUS1), Address - 0X02H

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	BOR	TSD	HOT	UVLO	UVLOB	UVLOU	USBFLG1	USBFLG2
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION(1)
BOR	Brownout. This bit is set whenever the input voltage drops below 9.3 V.
TSD	Thermal shutdown
HOT	Thermal shutdown early warning
UVLO	VIN under-voltage lockout
UVLOB	VINB under-voltage lockout
UVLOU	VINU under-voltage lockout
USBFLG1	USB fault flag (channel1)
USBFLG2	USB fault flag (channel2)

(1) All status bits are cleared after register read access. INT output pin will go high-impedance (open drain output) after STATUS1 and STATUS2 register have been read and / or all flags have been reset.

STATUS Register (STATUS2), Address - 0X03H

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	BCK1_UVD	BCK2_UVD	BCK3_UVD	BCK1_PG	BCK2_PG	BCK3_PG
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION(1)
BCK1_UVD	Under voltage detect, BUCK1
BCK2_UVD	Under voltage detect, BUCK2
BCK3_UVD	Under voltage detect, BUCK3
BCK1_PG	Power Good, BUCK1
BCK2_PG	Power Good, BUCK2
BCK3_PG	Power Good, BUCK3

(1) Bits [5:3] are cleared after register read access. INT output pin will go high-impedance (open drain output) after STATUS1 and STATUS2 register have been read and / or all flags have been reset.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65230A2DCA	NRND	HTSSOP	DCA	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	TPS65230 A2	
TPS65230A2DCAR	NRND	HTSSOP	DCA	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	TPS65230 A2	
TPS65231A2DCA	NRND	HTSSOP	DCA	48		TBD	Call TI	Call TI	0 to 85	TPS65231 A2	
TPS65231A2DCAR	NRND	HTSSOP	DCA	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	TPS65231 A2	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

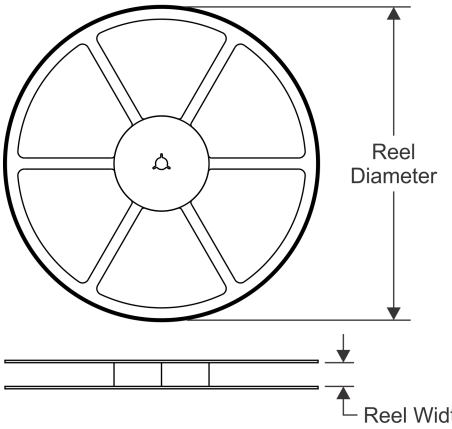
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

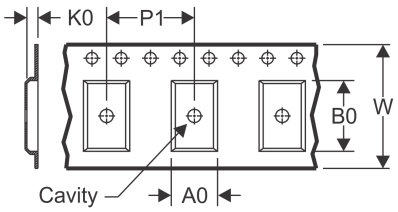
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

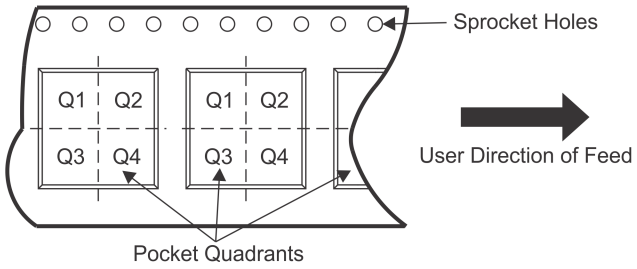


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

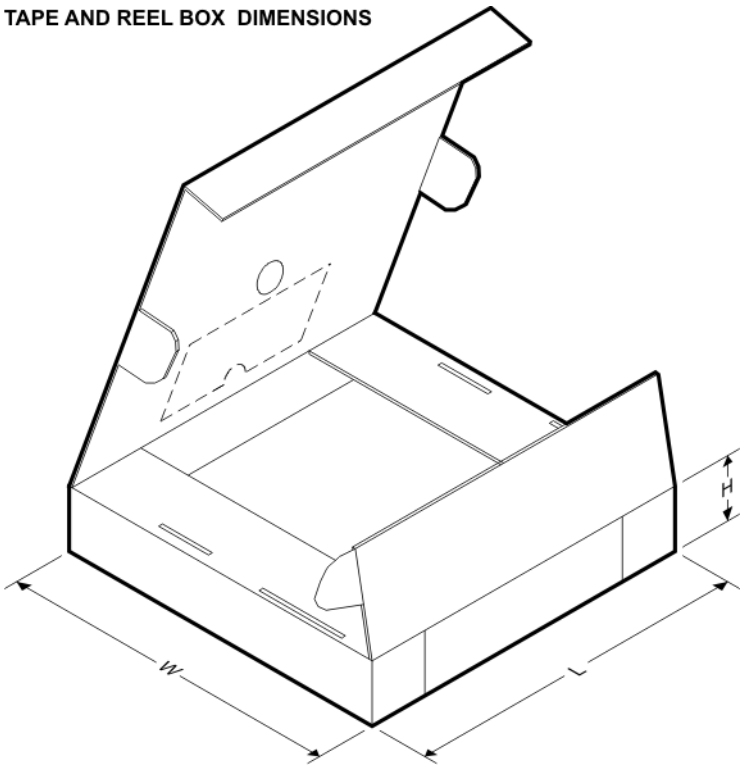
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65230A2DCAR	HTSSOP	DCA	48	1	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
TPS65231A2DCAR	HTSSOP	DCA	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1

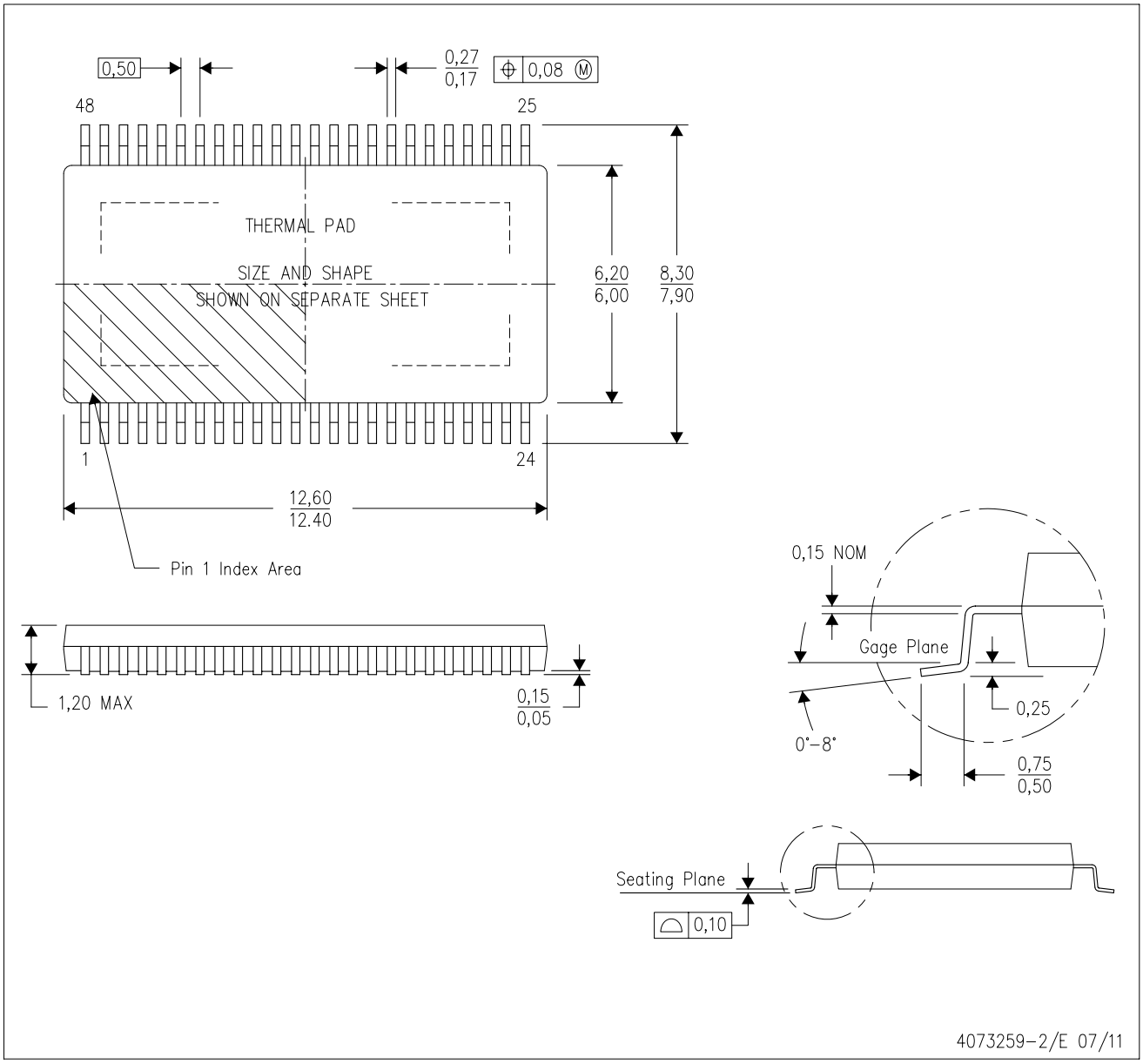
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65230A2DCAR	HTSSOP	DCA	48	1	367.0	367.0	45.0
TPS65231A2DCAR	HTSSOP	DCA	48	2000	367.0	367.0	45.0

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

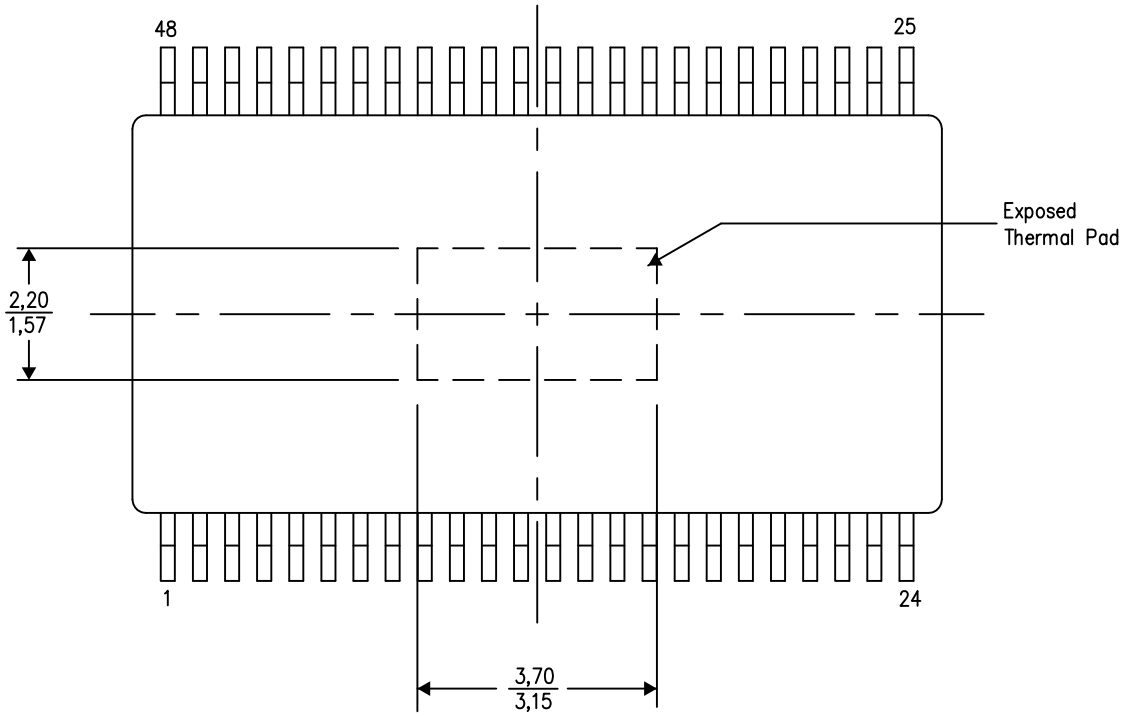
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

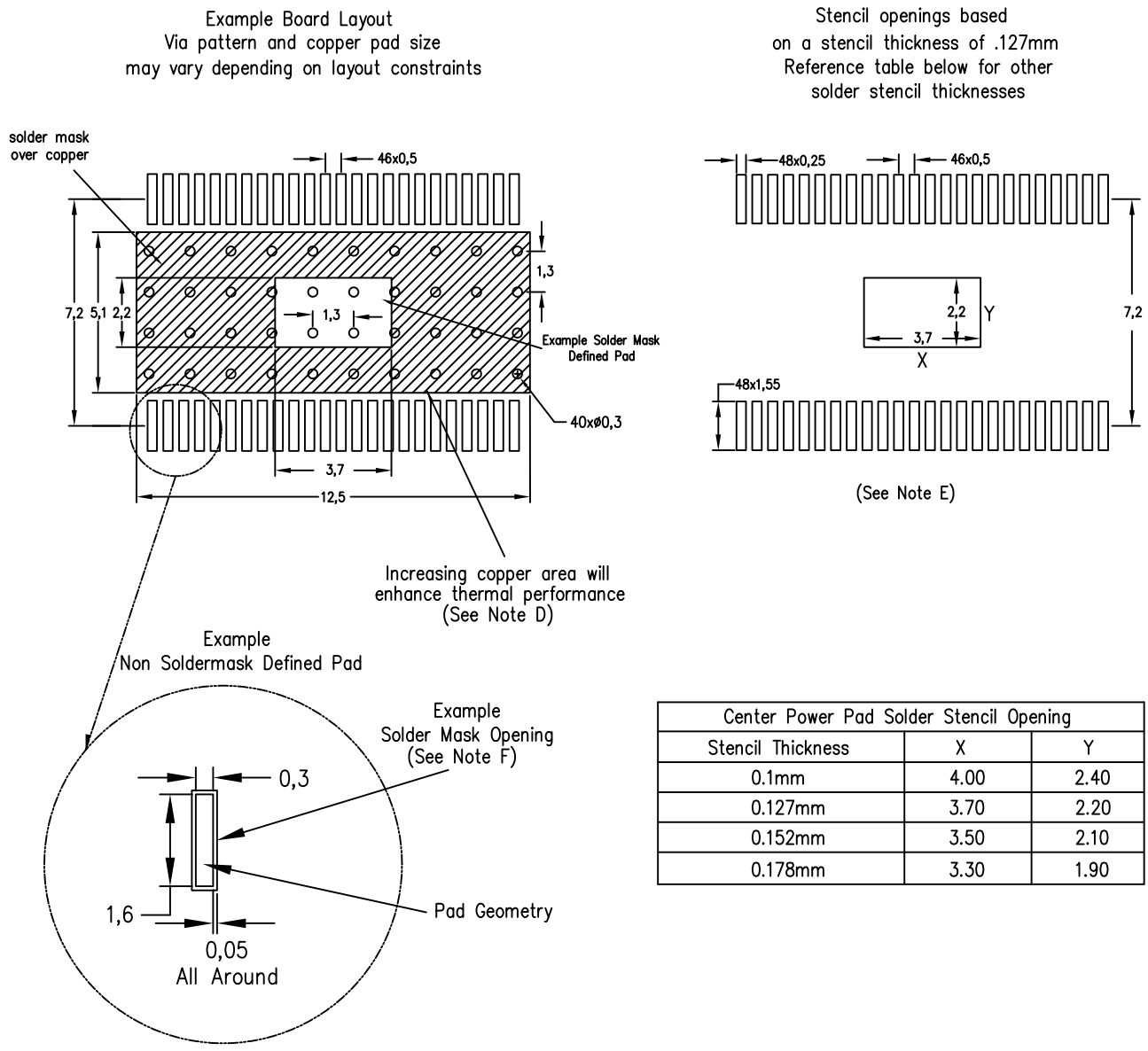
Exposed Thermal Pad Dimensions

4206320–5/R 03/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.00	2.40
0.127mm	3.70	2.20
0.152mm	3.50	2.10
0.178mm	3.30	1.90

4208546–4/G 12/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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