

# FQP5N60C / FQPF5N60C

## N-Channel QFET® MOSFET

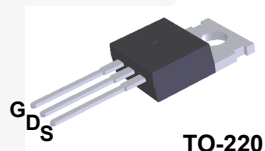
600 V, 4.5 A, 2.5 Ω

### Description

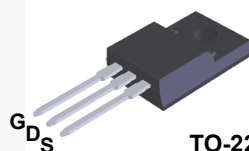
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

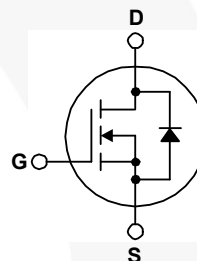
- 4.5 A, 600 V,  $R_{DS(on)} = 2.5 \Omega$  (Max.) @  $V_{GS} = 10 V$ ,  $I_D = 2.25 A$
- Low Gate Charge (Typ. 15 nC)
- Low Crss (Typ. 6.5 pF)
- 100% Avalanche Tested



TO-220



TO-220F



### Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	FQP5N60C	FQPF5N60C	Unit
$V_{DSS}$	Drain-Source Voltage	600		V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ C$ )	4.5	4.5 *	A
	- Continuous ( $T_C = 100^\circ C$ )	2.6	2.6 *	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	18	18 *	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	210		mJ
$I_{AR}$	Avalanche Current (Note 1)	4.5		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	10		mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	4.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ C$ )	100	33	W
	- Derate above $25^\circ C$	0.8	0.26	W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300		$^\circ C$

\* Drain current limited by maximum junction temperature.

### Thermal Characteristics

Symbol	Parameter	FQP5N60C	FQPF5N60C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.25	3.79	$^\circ C/W$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ, Max.	0.5	--	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	$^\circ C/W$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP5N60C	FQP5N60C	TO-220	Tube	N/A	N/A	50 units
FQPF5N60C	FQPF5N60C	TO-220F	Tube	N/A	N/A	50 units

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.6	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 2.25\text{ A}$	--	2.0	2.5	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 2.25\text{ A}$	--	4.7	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	515	670	pF
$C_{oss}$	Output Capacitance		--	55	72	pF
$C_{rss}$	Reverse Transfer Capacitance		--	6.5	8.5	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 4.5\text{ A},$ $R_G = 25\text{ }\Omega$  (Note 4)	--	10	30	ns
$t_r$	Turn-On Rise Time		--	42	90	ns
$t_{d(off)}$	Turn-Off Delay Time		--	38	85	ns
$t_f$	Turn-Off Fall Time		--	46	100	ns
$Q_g$	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 4.5\text{ A},$ $V_{GS} = 10\text{ V}$  (Note 4)	--	15	19	nC
$Q_{gs}$	Gate-Source Charge		--	2.5	--	nC
$Q_{gd}$	Gate-Drain Charge		--	6.6	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	4.5	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	18	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 4.5 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 4.5 A, dI <sub>F</sub> / dt = 100 A/μs	--	300	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	2.2	--	μC

#### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2.  $L = 18.9\text{ mH}, I_{AS} = 4.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 4.5\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Characteristics

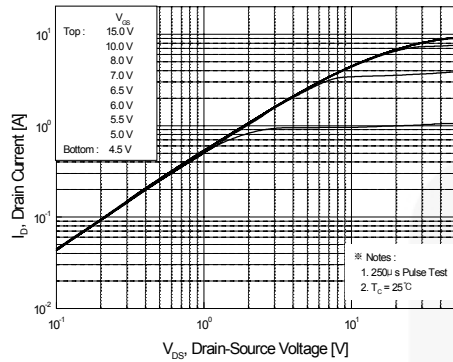


Figure 1. On-Region Characteristics

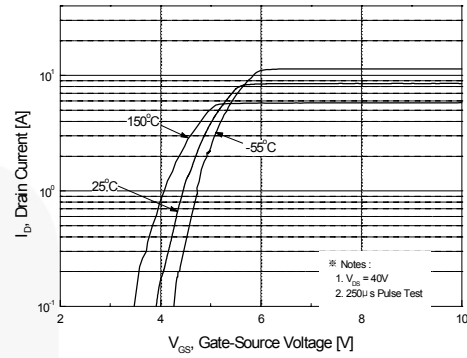


Figure 2. Transfer Characteristics

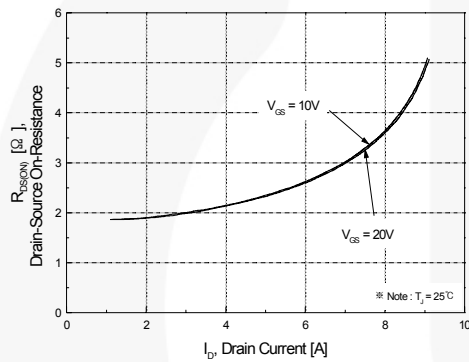


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

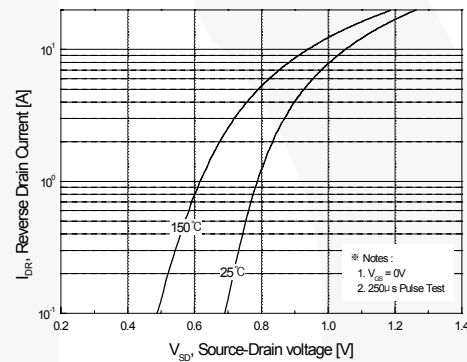


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

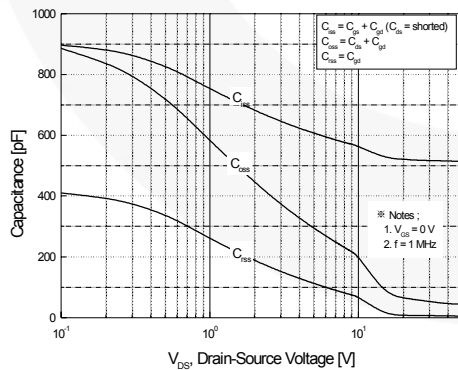


Figure 5. Capacitance Characteristics

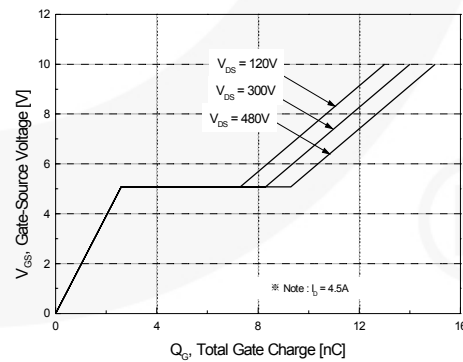


Figure 6. Gate Charge Characteristics

## Typical Characteristics (Continued)

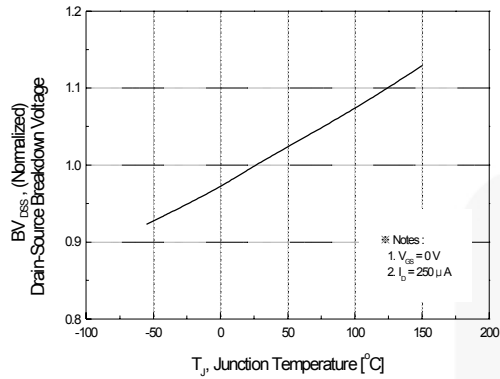


Figure 7. Breakdown Voltage Variation vs Temperature

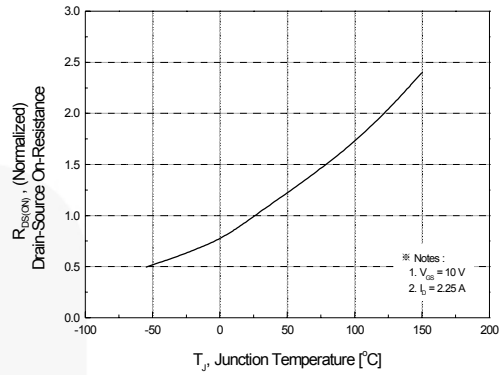


Figure 8. On-Resistance Variation vs Temperature

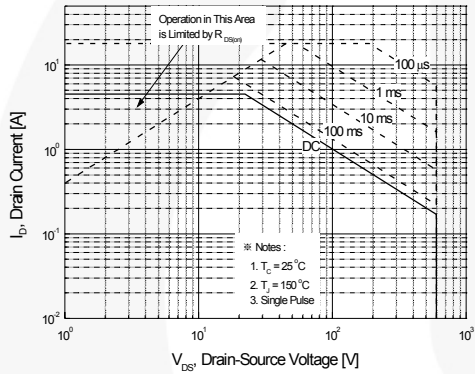


Figure 9-1. Maximum Safe Operating Area for FQP5N60C

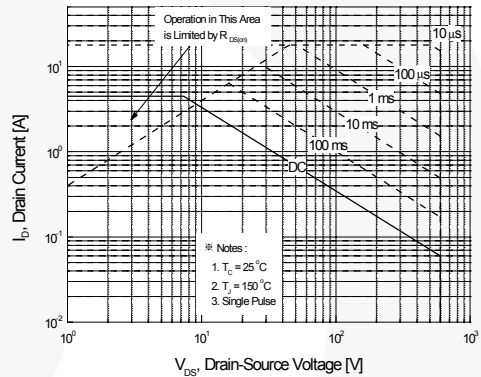


Figure 9-2. Maximum Safe Operating Area for FQPF5N60C

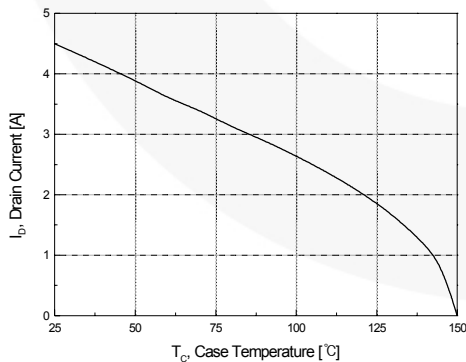


Figure 10. Maximum Drain Current vs Case Temperature

# Typical Characteristics (Continued)

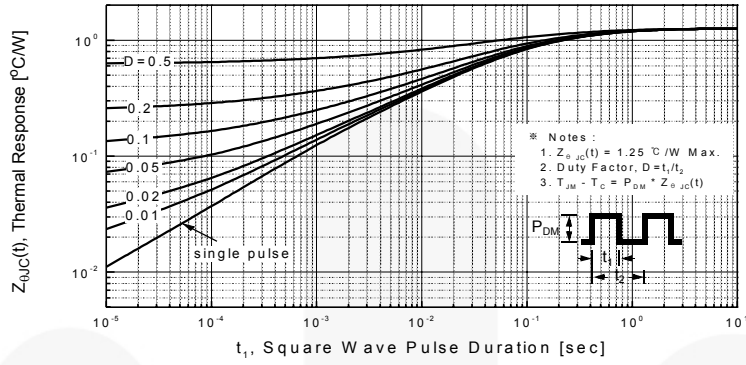


Figure 11-1. Transient Thermal Response Curve for FQP5N60C

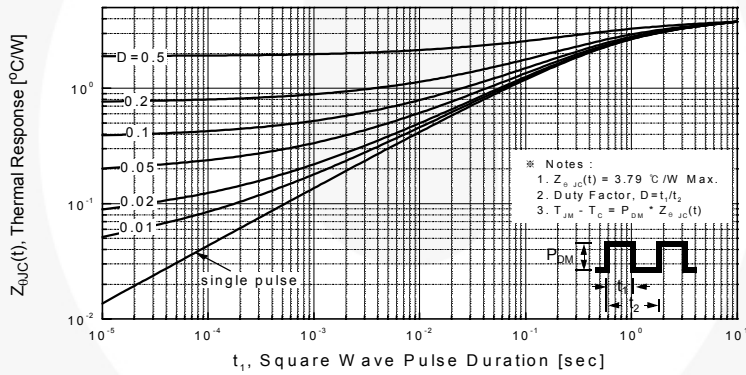


Figure 11-2. Transient Thermal Response Curve for FQPF5N60C

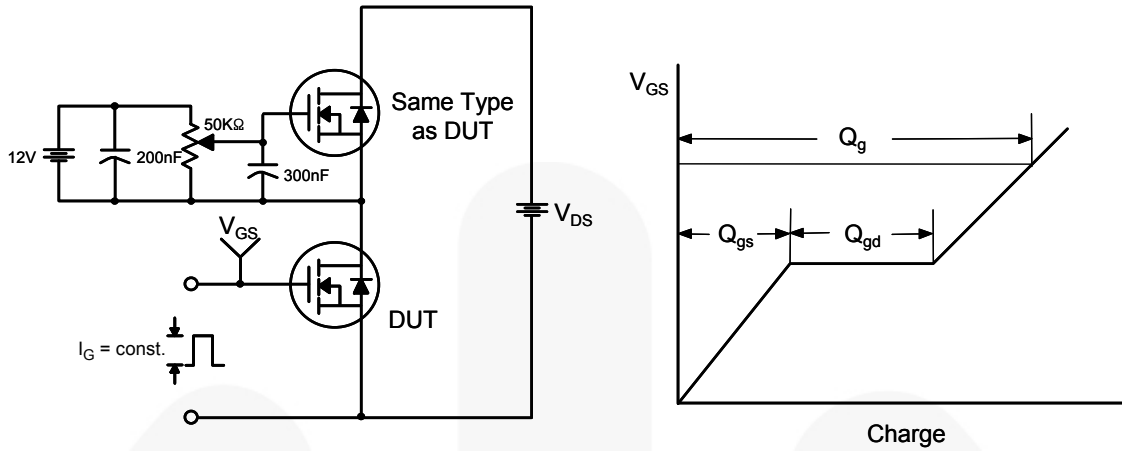


Figure 12. Gate Charge Test Circuit & Waveform

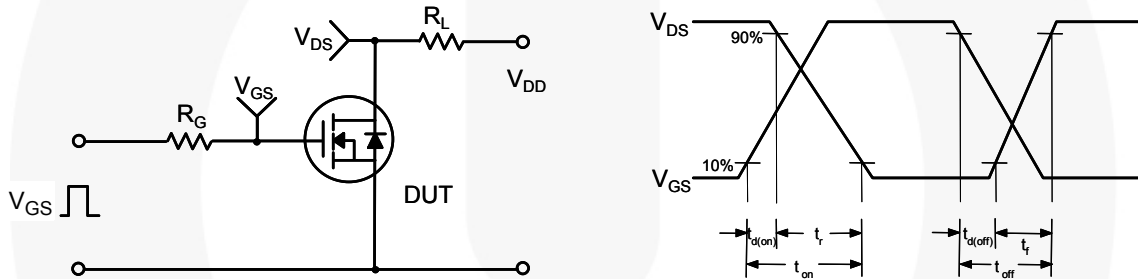


Figure 13. Resistive Switching Test Circuit & Waveforms

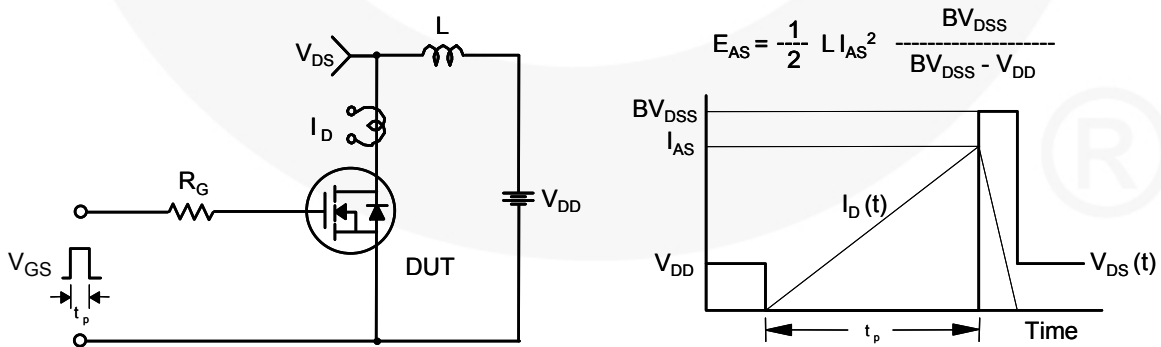
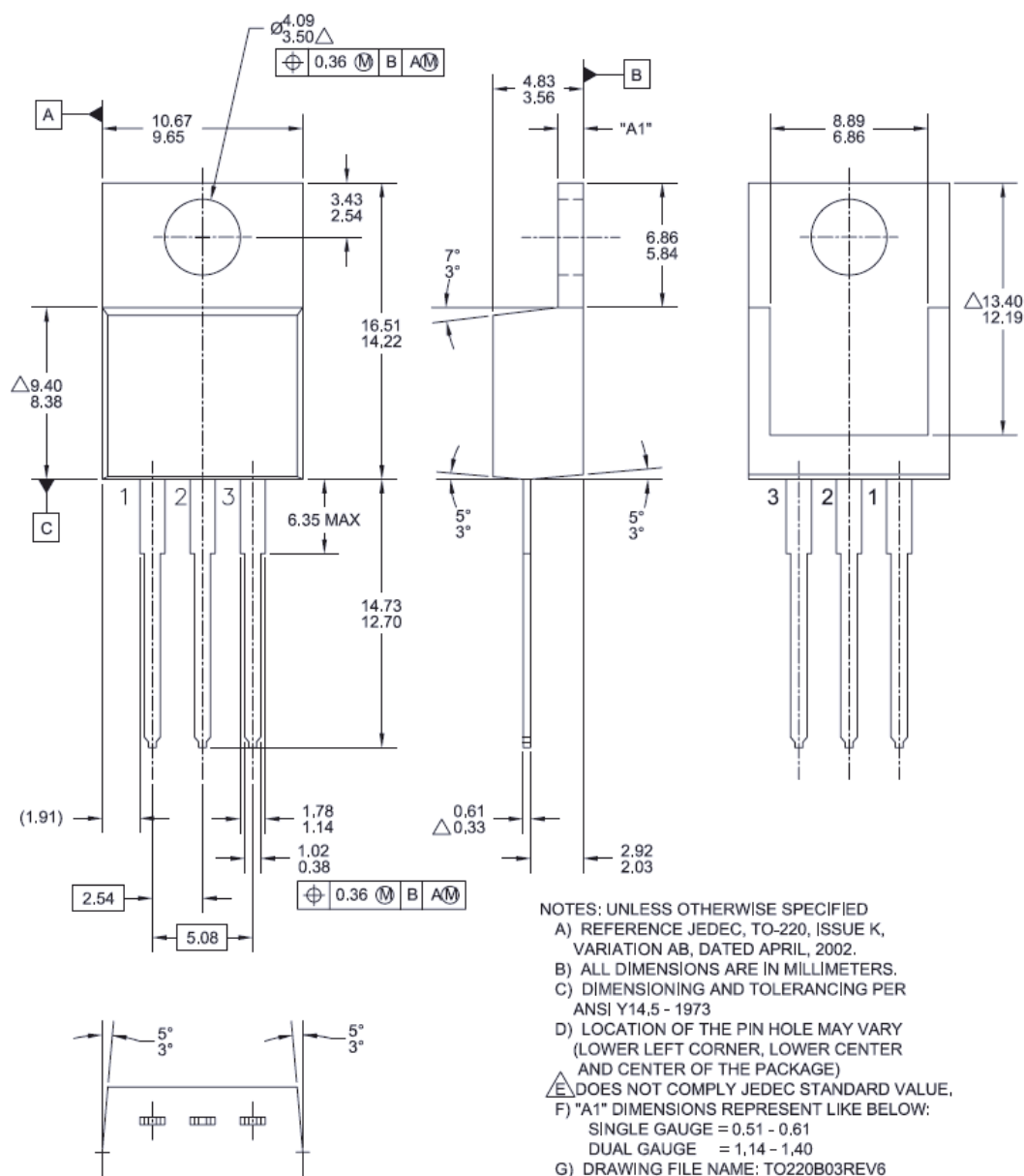


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



**Figure 16. TO-220, Molded, 3-Lead, Jedec Variation AB**

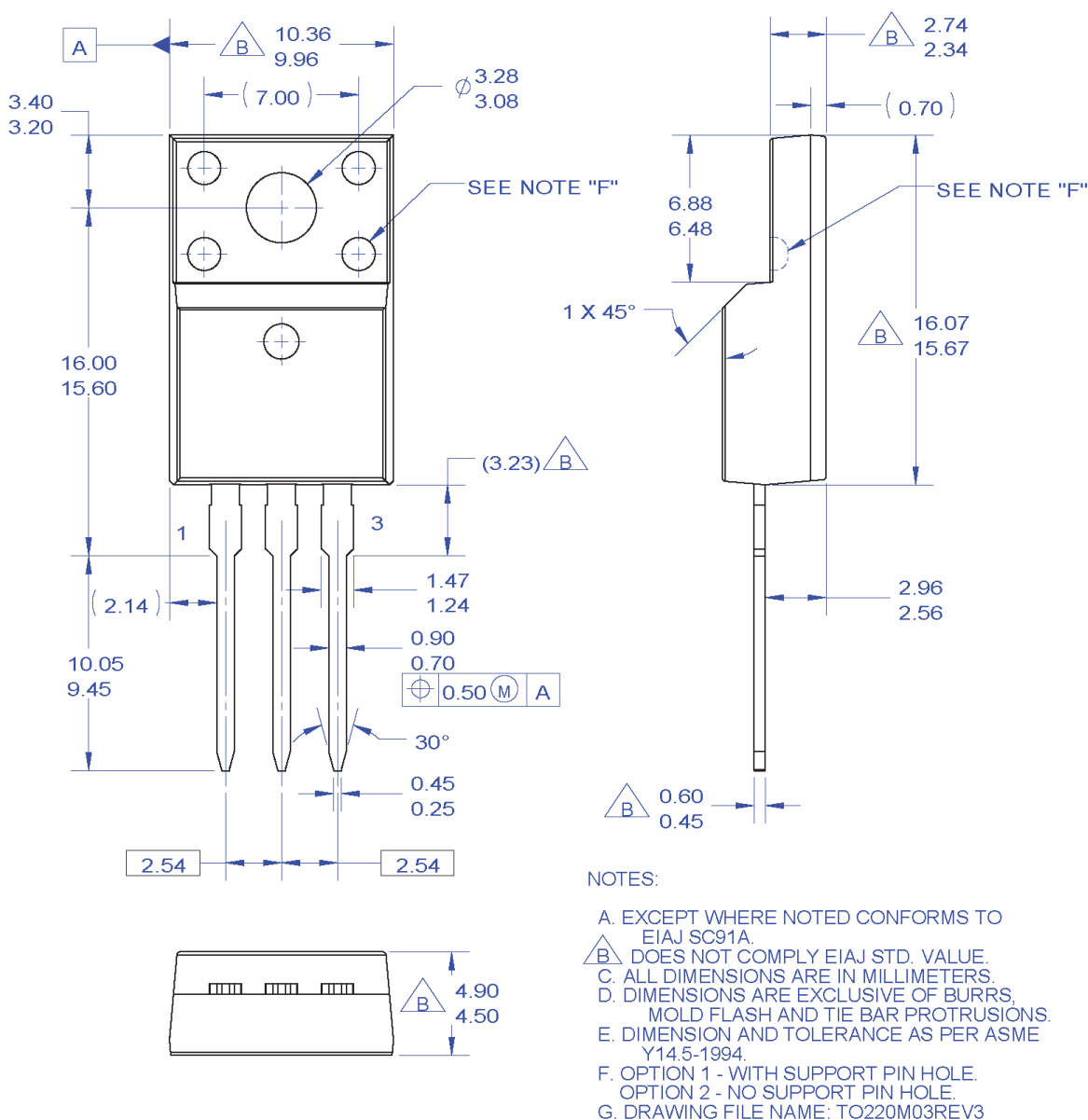
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## Mechanical Dimensions



**Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead**

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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