

1. Overview

The M16C/29 group of single-chip microcomputers is built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and is packaged in a 64-pin and 80-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. They also contain a CAN module, makes it suitable for control of cars and LAN system of FA. In addition, they contain a multiplier and a DMAC, also making it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Automotive body, safety & audio, LAN system of FA, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Table 1.2.1 lists performance outline of M16C/29 group 80-pin device.

Table 1.2.2 lists performance outline of M16C/29 group 64-pin device.

Table 1.2.1. Performance outline of M16C/29 group (80-pin device)

Item		Performance
CPU	Number of basic instructions	91 instructions
	Shortest instruction execution time	50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V) (Normal-ver./T-ver.) 100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V) (Normal-ver.) 50 ns (f(BCLK)= 20MHz, Vcc= 4.2V to 5.5V -40 to 105°C) (V-ver.) 62.5 ns (f(BCLK)= 16MHz, Vcc= 4.2V to 5.5V -40 to 125°C) (V-ver.)
	Operation mode	Single chip mode
	Address space	1M bytes
	Memory capacity	ROM/RAM : See the product list
	port	Input/Output : 71 lines
Peripheral function	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
	Serial I/O	2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I ² C bus ¹ , or IEBus ² 2 channels (SI/O3, SI/O4) Clock synchronous 1 channel (Multi-Master I ² C bus ¹)
	A/D converter	10 bits x 27 channels
	DMAC	2 channels
	CRC calculation circuit	2 polynomial (CRC-CCITT and CRC-16) with MSB/LSB selectable
	CAN module	1 channel 2.0B BOSCH compliant
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	28 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock • Sub-clock • On-chip oscillator(main-clock oscillation stop detect function) • PLL frequency synthesizer (These circuits contain a built-in feedback resistor and external ceramic/quartz oscillator)
	Low voltage detection circuit	Available (Normal-ver.) Not available (T-ver./V-ver.)
	Electrical Characteristics	Vcc=3.0V to 5.5V (f(BCLK)=20MHz) (Normal-ver.) Vcc=2.7V to 5.5V (f(BCLK)=10MHz) Vcc=3.0V to 5.5V (T-ver.) Vcc=4.2V to 5.5V (V-ver.)
		Power consumption 18mA (Vcc=5V, f(BCLK)=20MHz) 25 μA (Vcc=5V, f(BCLK)=f(X _{CIN})=32KHz on RAM) 1.8 μA (Vcc=5V, f(BCLK)=f(X _{CIN})=32KHz, in wait mode) 0.8 μA (Vcc=5V, when stop mode)
		Flash memory
		Program/erase voltage 2.7V to 5.5V (Normal-ver.) 3.0V to 5.5V (T-ver.) 4.2V to 5.5V (V-ver.) Number of program/erase 100 times (Block A, Block B : 10,000 times (option ³))
	Operating ambient temperature	
	-20 to 85°C / -40 to 85°C (option ³) (Normal-ver.) -40 to 85°C (T-ver.) -40 to 125°C (V-ver.)	
Package		80-pin plastic mold QFP

Notes:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. If you desire this option, please so specify.

Table 1.2.2. Performance outline of M16C/29 group (64-pin device)

Item		Performance
CPU	Number of basic instructions	91 instructions
	Shortest instruction execution time	50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V) (Normal-ver./T-ver.) 100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V) (Normal-ver.) 50 ns (f(BCLK)= 20MHz, Vcc= 4.2V to 5.5V -40 to 105°C) (V-ver.) 62.5 ns (f(BCLK)= 16MHz, Vcc= 4.2V to 5.5V -40 to 125°C) (V-ver.)
	Operation mode	Single chip mode
	Address space	1M bytes
	Memory capacity	ROM/RAM : See the product list
	port	Input/Output : 55 lines
Peripheral function	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
	Serial I/O	2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I ² C bus ¹ , or IEBus ² 1 channel (SI/O3) Clock synchronous 1 channel (Multi-Master I ² C bus ¹)
	A/D converter	10 bits x 16 channels
	DMAC	2 channels
	CRC calculation circuit	2 polynomial (CRC-CCITT and CRC-16) with MSB/LSB selectable
	CAN module	1 channel 2.0B BOSCH compliant
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	28 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock • Sub-clock • On-chip oscillator(main-clock oscillation stop detect function) • PLL frequency synthesizer (These circuits contain a built-in feedback resistor and external ceramic/quartz oscillator)
	Low voltage detection circuit	Available (Normal-ver.) Not available (T-ver./V-ver.)
Electrical Characteristics	Power supply voltage	Vcc=3.0V to 5.5V (f(BCLK)=20MHz) (Normal-ver.) Vcc=2.7V to 5.5V (f(BCLK)=10MHz) Vcc=3.0V to 5.5V (T-ver.) Vcc=4.2V to 5.5V (V-ver.)
	Power consumption	18mA (Vcc=5V, f(BCLK)=20MHz) 25 μA (Vcc=5V, f(BCLK)=f(X _{CIN})=32KHz on RAM) 1.8 μA (Vcc=5V, f(BCLK)=f(X _{CIN})=32KHz, in wait mode) 0.8 μA (Vcc=5V, when stop mode)
Flash memory	Program/erase voltage	2.7V to 5.5V (Normal-ver.) 3.0V to 5.5V (T-ver.) 4.2V to 5.5V (V-ver.)
	Number of program/erase	100 times (Block A, Block B : 10,000 times (option ³))
Operating ambient temperature		-20 to 85°C / -40 to 85°C (option ³) (Normal-ver.) -40 to 85°C (T-ver.) -40 to 125°C (V-ver.)
Package		64-pin plastic mold QFP

Notes:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
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1.3 Block Diagram

Figure 1.3.1 is a block diagram of the M16C/29 group, 80-pin device.

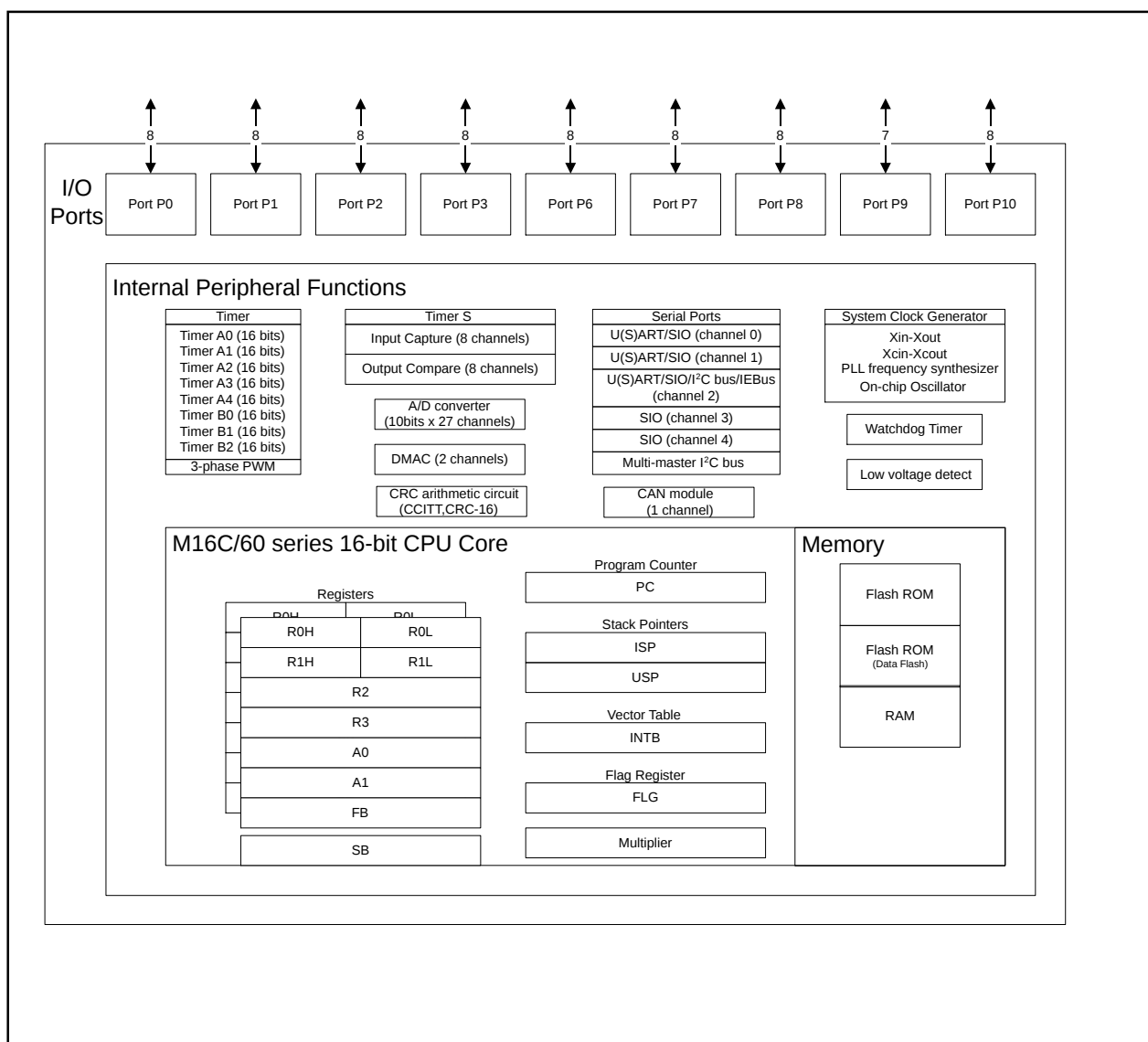


Figure 1.3.1. M16C/28 Group, 80-pin Block Diagram

Figure 1.3.2 is a block diagram of the M16C/29 group, 64-pin device.

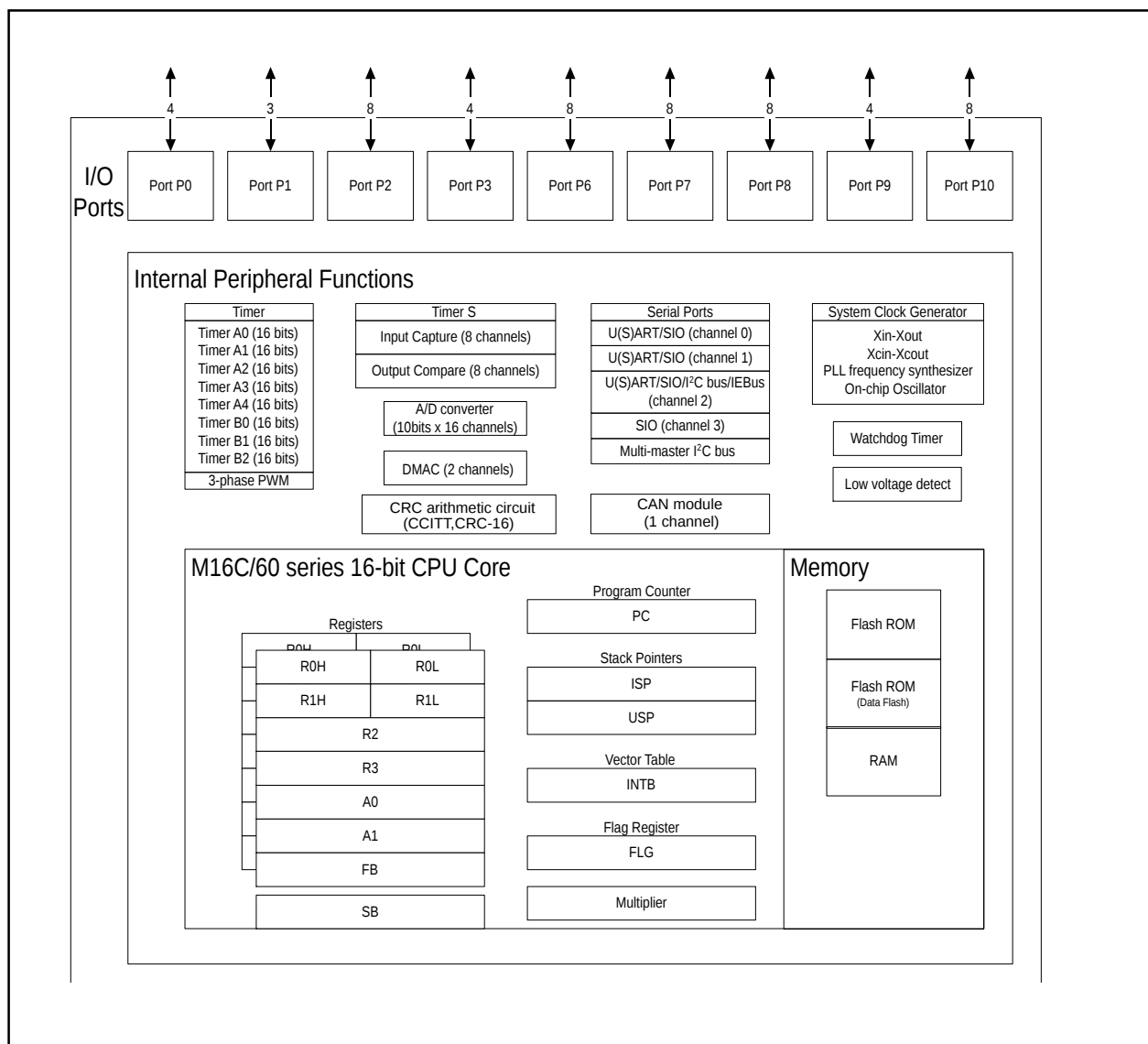


Figure 1.3.2. M16C/28 Group, 64-pin Block Diagram

1.4 Product List

Tables 1.4.1 to 1.4.3 list the M16C/29 group products and Figure 1.4.1 shows the type numbers, memory sizes and packages.

Table 1.4.1. Product List (1) -Normal-ver.

As of Jun 2004

Type No.		ROM capacity	RAM capacity	Package type	Remarks
M30290F8HP	(P)	64K + 4K byte	4K byte	80P6Q-A	Flash ROM Version
M30290FAHP	(D)	96K + 4K byte	8K byte		
M30290FCHP	(D)	128K + 4K byte	12K byte		
M30291F8HP	(P)	64K + 4K byte	4K byte	64P6Q-A	
M30291FAHP	(D)	96K + 4K byte	8K byte		
M30291FCHP	(D)	128K + 4K byte	12K byte		
M30290M8-XXXHP	(P)	64K byte	4K byte	80P6Q-A	Mask ROM Version
M30290MA-XXXHP	(P)	96K byte	8K byte		
M30290MC-XXXHP	(P)	128K byte	12K byte		
M30291M8-XXXHP	(P)	64K byte	4K byte	64P6Q-A	
M30291MA-XXXHP	(P)	96K byte	8K byte		
M30291MC-XXXHP	(P)	128K byte	12K byte		

(P) : under planning (D) : under development

Table 1.4.2. Product List (2) -T-ver.

As of Jun 2004

Type No.		ROM capacity	RAM capacity	Package type	Remarks
M30290F8THP	(P)	64K + 4K byte	4K byte	80P6Q-A	Flash ROM Version
M30290FATHP	(D)	96K + 4K byte	8K byte		
M30290FCTHP	(D)	128K + 4K byte	12K byte		
M30291F8THP	(P)	64K + 4K byte	4K byte	64P6Q-A	
M30291FATHP	(D)	96K + 4K byte	8K byte		
M30291FCTHP	(D)	128K + 4K byte	12K byte		
M30290M8T-XXXHP	(P)	64K byte	4K byte	80P6Q-A	Mask ROM Version
M30290MAT-XXXHP	(P)	96K byte	8K byte		
M30290MCT-XXXHP	(P)	128K byte	12K byte		
M30291M8T-XXXHP	(P)	64K byte	4K byte	64P6Q-A	
M30291MAT-XXXHP	(P)	96K byte	8K byte		
M30291MCT-XXXHP	(P)	128K byte	12K byte		

(P) : under planning (D) : under development

NOTES: Specification of T-ver. partly varies from the one of Normal-ver.

Table 1.4.3. Product List (3) -V-ver.

As of Jun 2004

Type No.		ROM capacity	RAM capacity	Package type	Remarks
M30290F8VHP	(P)	64K + 4K byte	4K byte	80P6Q-A	Flash ROM Version
M30290FAVHP	(D)	96K + 4K byte	8K byte		
M30290FCVHP	(D)	128K + 4K byte	12K byte		
M30291F8VHP	(P)	64K + 4K byte	4K byte	64P6Q-A	
M30291FAVHP	(D)	96K + 4K byte	8K byte		
M30291FCVHP	(D)	128K + 4K byte	12K byte		
M30290M8V-XXXHP	(P)	64K byte	4K byte	80P6Q-A	Mask ROM Version
M30290MAV-XXXHP	(P)	96K byte	8K byte		
M30290MCV-XXXHP	(P)	128K byte	12K byte		
M30291M8V-XXXHP	(P)	64K byte	4K byte	64P6Q-A	
M30291MAV-XXXHP	(P)	96K byte	8K byte		
M30291MCV-XXXHP	(P)	128K byte	12K byte		

(P) : under planning (D) : under development

NOTES: Specification of V-ver. partly varies from the one of Normal-ver.

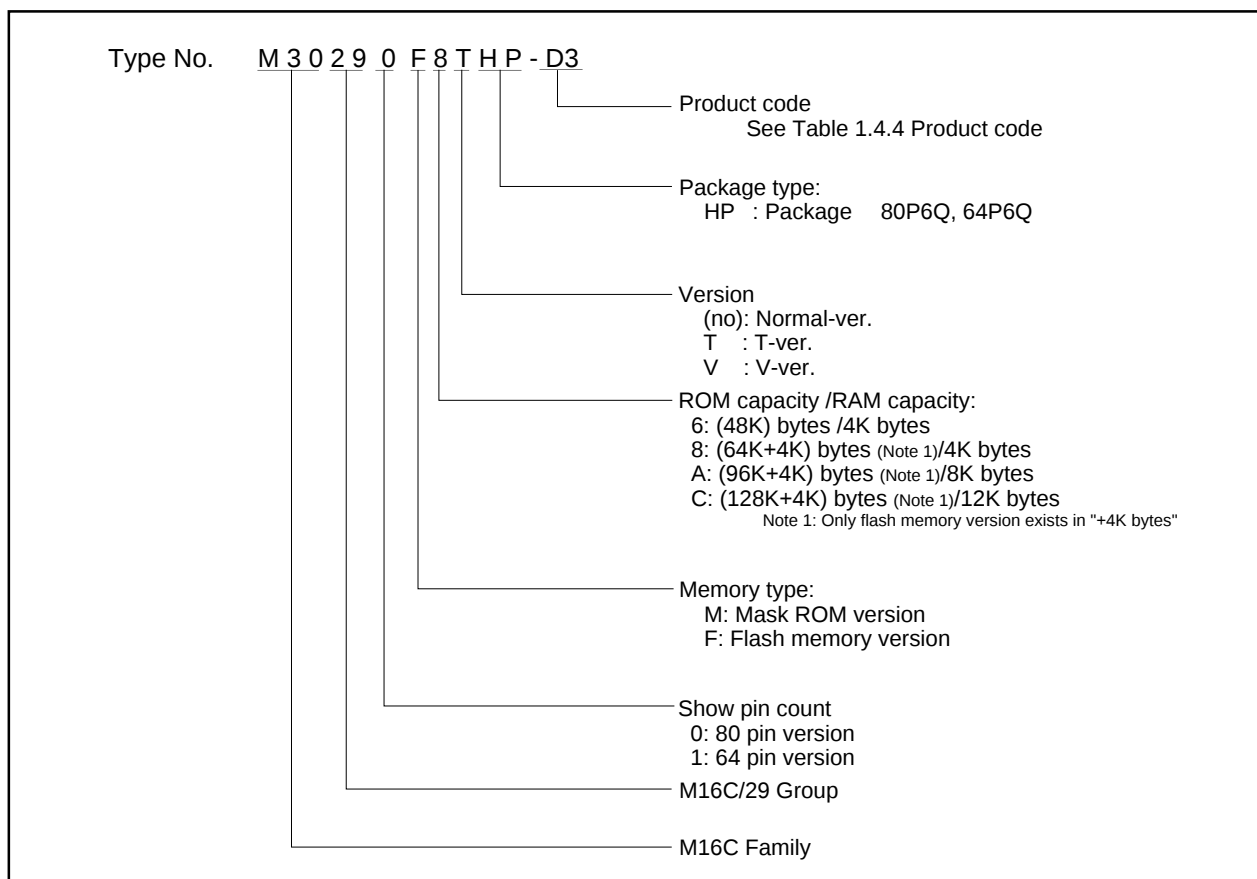
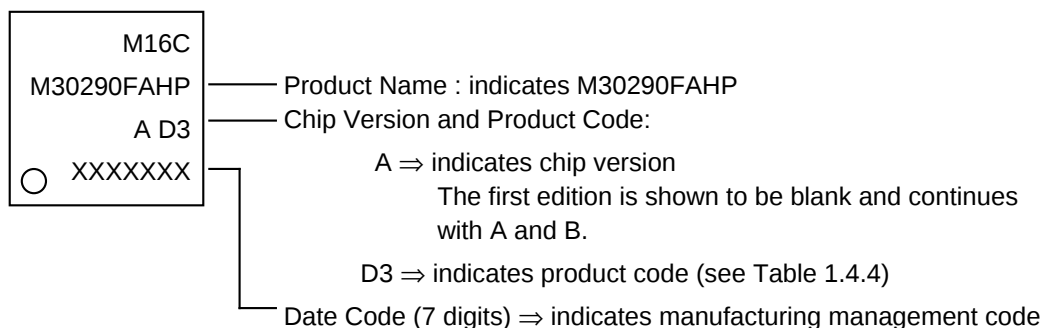


Figure 1.4.1. Type No., Memory Size, and Package

Table 1.4.4. Product code (Flash ROM Version, Normal-ver.)

Product Code	Package	Internal ROM Block (0, 1, 2, 3)		Internal ROM Block (A, B)		Microcomputer operating temperature
		E/W cycles	Temperature range	E/W cycles	Temperature range	
D3	non-LEAD free	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
D5						-20°C to 85°C
D7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
D9					-20°C to 85°C	-20°C to 85°C
U3	LEAD free	100		100	0°C to 60°C	-40°C to 85°C
U5						-20°C to 85°C
U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
U9					-20°C to 85°C	-20°C to 85°C

(1) Flash ROM Version, 80P6Q-A, Normal-ver.



(2) Flash ROM Version, 64P6Q-A, Normal-ver.

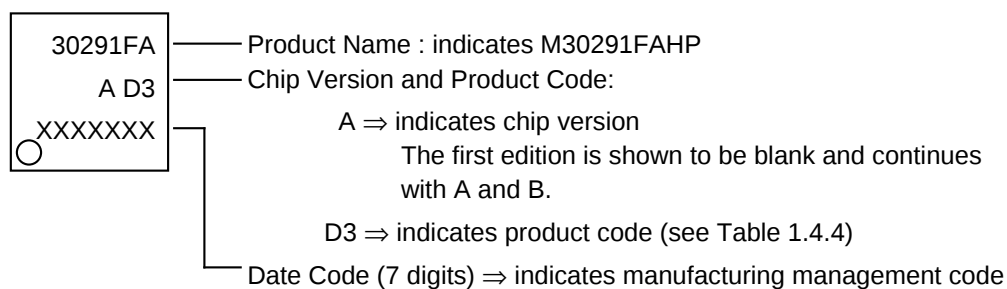


Figure 1.4.2. Marking (Top View)

1.5 Pin Configuration

Figures 1.5.1 and 1.5.2 show the pin configurations (top view).

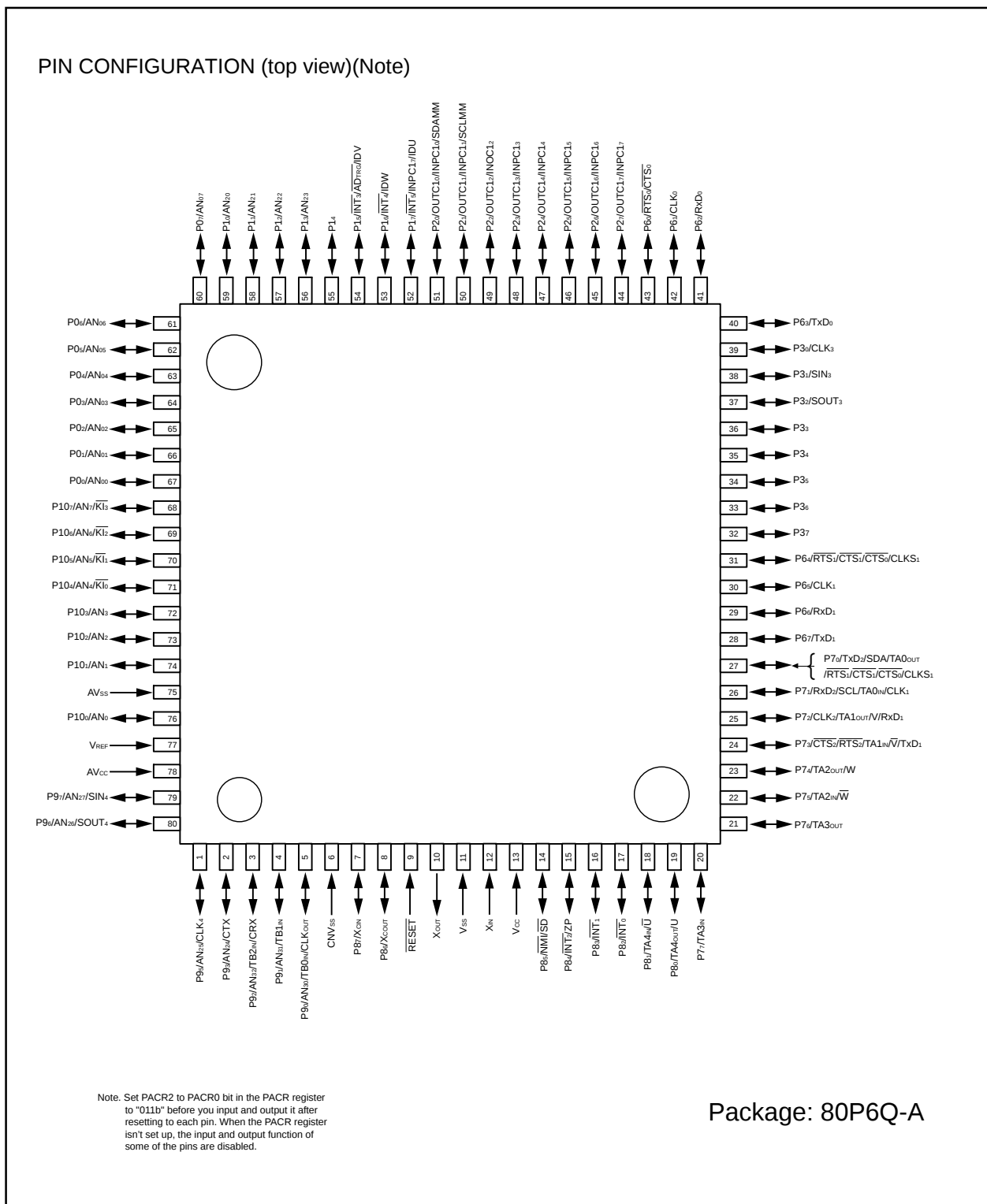


Figure 1.5.1. Pin Configuration (Top View) of M16C/29 Group, 80-pin Package

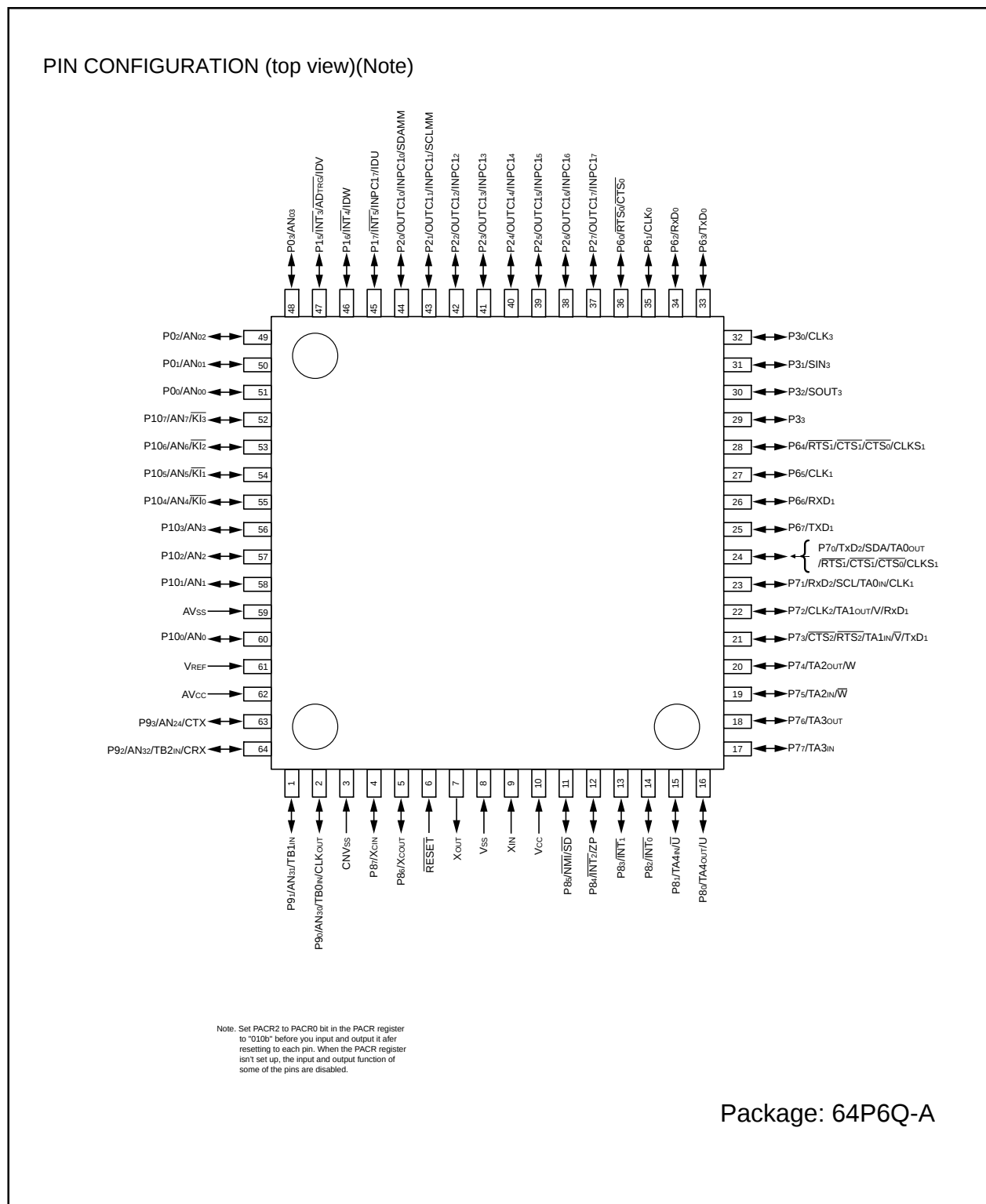


Figure 1.5.2. Pin Configuration (Top View) of M16C/29 Group, 64-pin Package

1.6 Pin Description

Table 1.6.1 and 1.6.2 describes the available pins.

Table 1.6.1 Pin Description(1)

Pin Name	Signal name	I/O type	Function
Vcc,Vss	Power supply input		Apply 0V to the Vss pin, and the following voltage to the Vcc pin. 2.7 to 5.5V (Normal-ver.) 3.0 to 5.5V (T-ver.) 4.2 to 5.5V (V-ver.)
CNVss	CNVss	Input	Connect this pin to Vss.
RESET	Reset input	Input	"L" on this input resets the microcomputer.
XIN XOUT	Clock input Clock output	Input Output	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or crystal between the XIN and the XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open. If XIN is not used (for external oscillator or external clock) connect XIN pin to Vcc and leave XOUT pin open.
AVcc	Analog power supply input		This pin is a power supply input for the A/D converter. Connect this pin to Vcc.
AVSS	Analog power supply input		This pin is a power supply input for the A/D converter. Connect this pin to Vss.
VREF	Reference Voltage input	Input	This pin is a reference voltage input for the A/D converter.
P00~P07	I/O port P0	Input/Output	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input, a pull-up register option can be selected for the entire group of four pins. Software can also select this port to function as A/D converter input pins. P04 to P07 is not in 64 pin version.
P10~P17	I/O port P1	Input/Output	This is an 8-bit I/O port equivalent to P0. Additional software selectable secondary functions are: 1) P10 to P13 can act as A/D converter input pins; 2) P15 to P17 can be configured as external interrupt pins; 3) P15 to P17 can be configured as position-data-retain function input pins, and; 4) P15 can input a trigger for the A/D converter. P10 to P14 is not in 64 pin version.
P20~P27	I/O port P2	Input/Output	This is an 8-bit I/O port equivalent to P0. Software can also select this port to perform as I/O for the Timer S (all pins), and MultiMaster I ² C Bus (P20 to P21 only).
P30~P37	I/O port P3	Input/Output	This is an 8-bit I/O port equivalent to P0. P30 to P32 also function as SIO3 I/O, as selected by software. P34 to P37 is not in 64 pin version.
P60~P67	I/O port P6	Input/Output	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as UART0 and UART1 I/O, as selected by software.

Table 1.6.2 Pin Description(2)

Pin Name	Signal name	I/O type	Function
P70~P77	I/O port P7	Input/Output	This is an 8-bit I/O port equivalent to P0. P7 can also function as I/O for timer A0 to A3, as selected by software. Additional programming options are: P70 to P73 can assume UART1 or UART2 I/O capabilities, and P72 to P75 can function as output pins for the three-phase motor control timer.
P80~P87	I/O port P8	Input/Output	This is an 8-bit I/O port equivalent to P0. Additional software selectable secondary functions are: 1) P80 and P81 can act as either I/O for Timer A4, as output pins for the three-phase motor control timer; 2) P82 to P84 can be configured as external interrupt pins. P84 can be used for Timer A Zphase function; 3) P85 can be used as $\overline{\text{NMI}}/\overline{\text{SD}}$. P85 can not be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to P85 after setting the direction register for P85 to "0" when the three-phase motor control is enabled, and; 4) P86 to P87 can serve as I/O pins for the subclock generation circuit. In this latter case, a quartz oscillator must be connected between P86 (XCOUT pin) and P87 (XCIN pin).
P90~P93, P95~P97	I/O port P9	Input/Output	This is an 7-bit I/O port equivalent to P0. Additional software selectable secondary functions are: 1) P90 to P92 can act as Timer B0 to B2 input pins; 2) P90 to P92 can act as A/D converter input pins; 3) P90 outputs a no division, divide-by-8 or divide-by-32 clock of XIN or a clock of the same frequency as XCIN as selected by program; 4) P92 and P93 can function as I/O pins for the CAN module; 5) P93, P95 to P97 can act as A/D converter input pins, and; 6) P96 to P97 can assume SI/O4 I/O. P95 to P97 is not in 64 pin version.
P100~P107	I/O port P10	Input/Output	This is an 8-bit I/O port equivalent to P0. This port can also function as A/D converter input pins, as selected by software. Furthermore, P104 to P107 can also function as input pins for the key input interrupt function.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

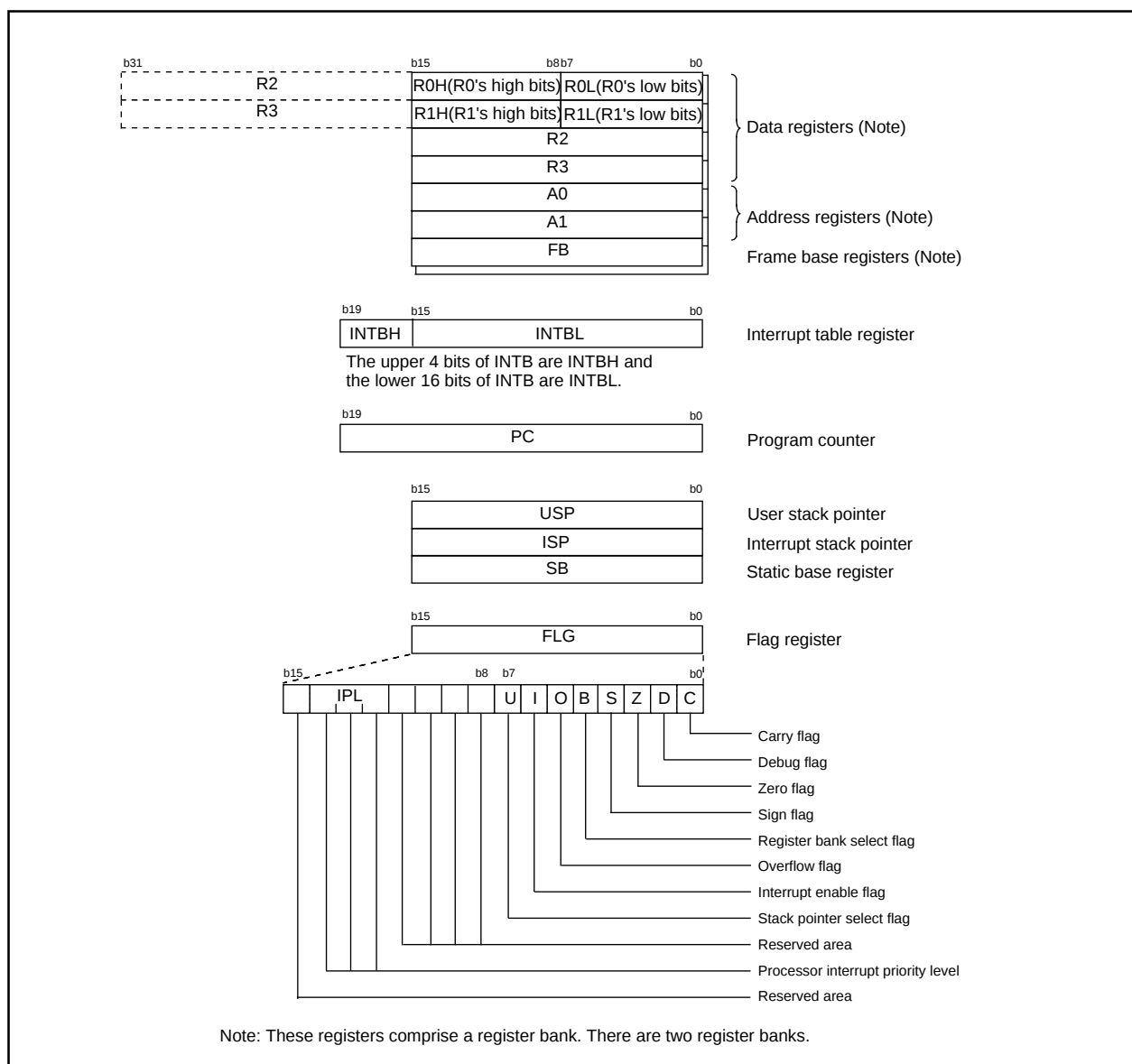


Figure 2.1. Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1".

The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of the M16C/29 group. The linear address space of 1M bytes extends from address 00000₁₆ to FFFFF₁₆. From FFFFF₁₆ down is ROM. For example, in the M30290F8HP, there are 64 Kbytes of internal ROM from F0000₁₆ to FFFFF₁₆.

The vector table for fixed interrupts, such as Reset and NMI, is mapped from FFFDC₁₆ to FFFFF₁₆. The starting address of the interrupt routine is stored here.

The address of the vector table for timer interrupts, etc., can be set as desired using the interrupt table register (INTB). See the section on interrupts for details.

From 00400₁₆ up is RAM. For example, in the M30290FAHP, 8K bytes of internal RAM is mapped to the space from 00400₁₆ to 023FF₁₆. In addition to storing data, the RAM also stores the stack used when calling subroutines and when interrupts are generated.

These devices also contain two blocks of Flash ROM as Data Flash memory to store data. These two blocks of 2K bytes are located from 0F000₁₆ to 0FFFF₁₆ on all versions.

The SFR area is mapped from 00000₁₆ to 003FF₁₆. This area accommodates the control registers for peripheral devices such as I/O ports, A/D converter, serial I/O, and timers, etc. Any part of the SFR area that is not occupied is reserved and cannot be used for other purposes.

The special page vector table is allocated to the address from FFE00₁₆ to FFFDB₁₆. This vector is used by the JMPS or JSRS instruction. For details, refer to the "M16C/60 and M16C/20 Series Software Manual".

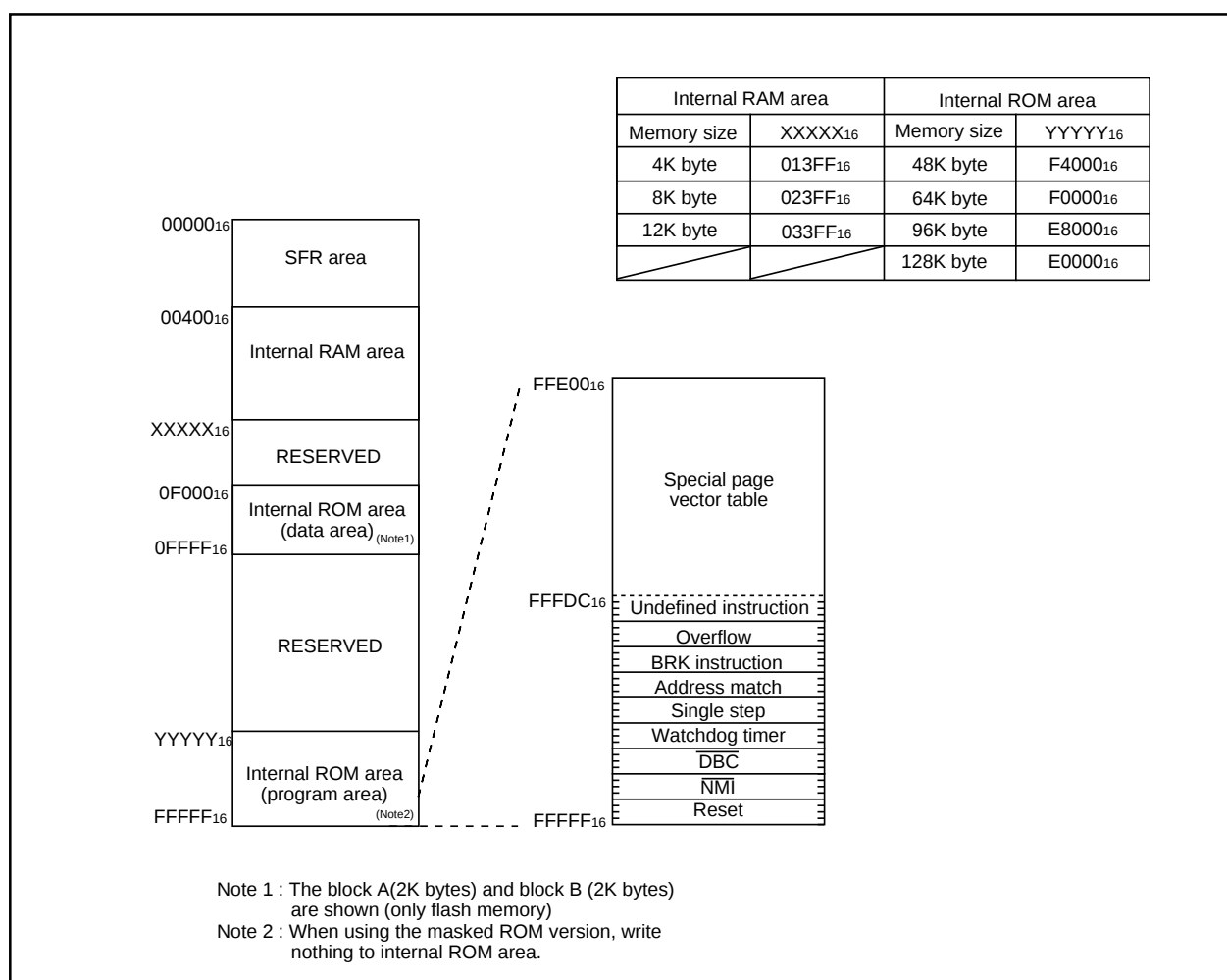


Figure 3.1. Memory Map

4. Special Function Register (SFR) Map

Address	Register	Symbol	After reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0	PM0	00 ₁₆
0005 ₁₆	Processor mode register 1	PM1	00001000 ₂
0006 ₁₆	System clock control register 0	CM0	01001000 ₂
0007 ₁₆	System clock control register 1	CM1	00100000 ₂
0008 ₁₆			
0009 ₁₆	Address match interrupt enable register	AIER	XXXXXX00 ₂
000A ₁₆	Protect register	PRCR	XX000000 ₂
000B ₁₆			
000C ₁₆	Oscillation stop detection register (Note 2)	CM2	0X000010 ₂
000D ₁₆			
000E ₁₆	Watchdog timer start register	WDTS	?? ₁₆
000F ₁₆	Watchdog timer control register	WDC	00?????? ₂ (Note3)
0010 ₁₆	Address match interrupt register 0	RMAD0	00 ₁₆
0011 ₁₆			00 ₁₆
0012 ₁₆			X0 ₁₆
0013 ₁₆			
0014 ₁₆	Address match interrupt register 1	RMAD1	00 ₁₆
0015 ₁₆			00 ₁₆
0016 ₁₆			X0 ₁₆
0017 ₁₆			
0018 ₁₆			
0019 ₁₆	Voltage detection register 1 (Note 4,5)	VCR1	00001000 ₂
001A ₁₆	Voltage detection register 2 (Note 4,5)	VCR2	00 ₁₆
001B ₁₆			
001C ₁₆	PLL control register 0	PLC0	0001X010 ₂
001D ₁₆			
001E ₁₆	Processor mode register 2	PM2	XXX00000 ₂
001F ₁₆	Voltage down detection interrupt register (Note 5)	D4INT	00 ₁₆
0020 ₁₆	DMA0 source pointer	SAR0	?? ₁₆
0021 ₁₆			?? ₁₆
0022 ₁₆			X? ₁₆
0023 ₁₆			
0024 ₁₆	DMA0 destination pointer	DAR0	?? ₁₆
0025 ₁₆			?? ₁₆
0026 ₁₆			X/ ₁₆
0027 ₁₆			
0028 ₁₆	DMA0 transfer counter	TCR0	?? ₁₆
0029 ₁₆			?? ₁₆
002A ₁₆			
002B ₁₆			
002C ₁₆	DMA0 control register	DM0CON	00000?00 ₂
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆	DMA1 source pointer	SAR1	?? ₁₆
0031 ₁₆			?? ₁₆
0032 ₁₆			X? ₁₆
0033 ₁₆			
0034 ₁₆	DMA1 destination pointer	DAR1	?? ₁₆
0035 ₁₆			?? ₁₆
0036 ₁₆			X? ₁₆
0037 ₁₆			
0038 ₁₆	DMA1 transfer counter	TCR1	?? ₁₆
0039 ₁₆			?? ₁₆
003A ₁₆			
003B ₁₆			
003C ₁₆	DMA1 control register	DM1CON	00000?00 ₂
003D ₁₆			
003E ₁₆			
003F ₁₆			

Note 1: The blank areas are reserved and cannot be used by users.

Note 2: The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.

Note 3: The WDC5 bit is "0" (cold start) immediately after power-on. It can only be set to "1" in a program.

It is set to "0" when the input voltage at the VCC pin drops to Vdet2 or less while the VC25 bit in the VCR2 register is set to "1" (RAM retention limit detection circuit enable).

Note 4: This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.

Note 5: This register can not use for T-ver. and V-ver.

X : Nothing is mapped to this bit

? : Undefined

Figure 4.1. SFR Map (1 of 11)

Address	Register	Symbol	After reset
0040 ₁₆			
0041 ₁₆	CAN0 wakeup interrupt control register	C01WKIC	XXXX?000 ₂
0042 ₁₆	CAN0 successful reception interrupt control register	C0RECIC	XXXX?000 ₂
0043 ₁₆	CAN0 successful transmission interrupt control register	C0TRMIC	XXXX?000 ₂
0044 ₁₆	INT3 interrupt control register	INT3IC	XX00?000 ₂
0045 ₁₆	ICOC 0 interrupt control register	ICOC0IC	XXXX?000 ₂
0046 ₁₆	ICOC 1 interrupt control register, I ² C-BUS interface interrupt control register 1	ICOC1IC, IICIC	XXXX?000 ₂
0047 ₁₆	ICOC base timer interrupt control register, SCL/SDA interrupt control register 2	BTIC, SCLDAIC	XXXX?000 ₂
0048 ₁₆	SI/O4 interrupt control register, INT5 interrupt control register	S4IC, INT5IC	XX00?000 ₂
0049 ₁₆	SI/O3 interrupt control register, INT4 interrupt control register	S3IC, INT4IC	XX00?000 ₂
004A ₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXX?000 ₂
004B ₁₆	DMA0 interrupt control register	DM0IC	XXXX?000 ₂
004C ₁₆	DMA1 interrupt control register	DM1IC	XXXX?000 ₂
004D ₁₆	CAN0 error interrupt control register	C01ERRIC	XXXX?000 ₂
004E ₁₆	A/D conversion interrupt control register, Key input interrupt control register (Note 2)	ADIC, KUPIC	XXXX?000 ₂
004F ₁₆	UART2 transmit interrupt control register	S2TIC	XXXX?000 ₂
0050 ₁₆	UART2 receive interrupt control register	S2RIC	XXXX?000 ₂
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	XXXX?000 ₂
0052 ₁₆	UART0 receive interrupt control register	S0RIC	XXXX?000 ₂
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	XXXX?000 ₂
0054 ₁₆	UART1 receive interrupt control register	S1RIC	XXXX?000 ₂
0055 ₁₆	TimerA0 interrupt control register	TA0IC	XXXX?000 ₂
0056 ₁₆	TimerA1 interrupt control register	TA1IC	XXXX?000 ₂
0057 ₁₆	TimerA2 interrupt control register	TA2IC	XXXX?000 ₂
0058 ₁₆	TimerA3 interrupt control register	TA3IC	XXXX?000 ₂
0059 ₁₆	TimerA4 interrupt control register	TA4IC	XXXX?000 ₂
005A ₁₆	TimerB0 interrupt control register	TB0IC	XXXX?000 ₂
005B ₁₆	TimerB1 interrupt control register	TB1IC	XXXX?000 ₂
005C ₁₆	TimerB2 interrupt control register	TB2IC	XXXX?000 ₂
005D ₁₆	INT0 interrupt control register	INT0IC	XX00?000 ₂
005E ₁₆	INT1 interrupt control register	INT1IC	XX00?000 ₂
005F ₁₆	INT2 interrupt control register	INT2IC	XX00?000 ₂
0060 ₁₆	CAN0 message box 0 : Identifier/DLC		XX?????2
0061 ₁₆			XX?????2
0062 ₁₆			?? ₁₆
0063 ₁₆			X? ₁₆
0064 ₁₆			X? ₁₆
0065 ₁₆			XX?????2
0066 ₁₆	CAN0 message box 0 : Data field		?? ₁₆
0067 ₁₆			?? ₁₆
0068 ₁₆			?? ₁₆
0069 ₁₆			?? ₁₆
006A ₁₆			?? ₁₆
006B ₁₆			?? ₁₆
006C ₁₆			?? ₁₆
006D ₁₆			?? ₁₆
006E ₁₆	CAN0 message box 0 : Time stamp		?? ₁₆
006F ₁₆			?? ₁₆
0070 ₁₆	CAN0 message box 1 : Identifier/DLC		XX?????2
0071 ₁₆			XX?????2
0072 ₁₆			?? ₁₆
0073 ₁₆			X? ₁₆
0074 ₁₆			X? ₁₆
0075 ₁₆			XX?????2
0076 ₁₆	CAN0 message box 1 : Data field		?? ₁₆
0077 ₁₆			?? ₁₆
0078 ₁₆			?? ₁₆
0079 ₁₆			?? ₁₆
007A ₁₆			?? ₁₆
007B ₁₆			?? ₁₆
007C ₁₆			?? ₁₆
007D ₁₆			?? ₁₆
007E ₁₆	CAN0 message box 1 : Time stamp		?? ₁₆
007F ₁₆			?? ₁₆

Note 1: The blank areas are reserved and cannot be used by users.

Note 2: A/D conversion interrupt control register is effective when the bit1(Interrupt source select register (address 35Eh IFSR2A) is set to "0". Key input interrupt control register is effective when the bit1 is set to "1".

X : Nothing is mapped to this bit

? : Undefined

Figure 4.2. SFR Map (2 of 11)

Address	Register	Symbol	After reset
0080 ₁₆ 0081 ₁₆ 0082 ₁₆ 0083 ₁₆ 0084 ₁₆ 0085 ₁₆	CAN0 message box 2: Identifier/DLC		XX?????? ₂ XX?????? ₂ ?? ₁₆ X? ₁₆ X? ₁₆ XX?????? ₂
0086 ₁₆ 0087 ₁₆ 0088 ₁₆ 0089 ₁₆ 008A ₁₆ 008B ₁₆ 008C ₁₆ 008D ₁₆	CAN0 message box 2 : Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
008E ₁₆ 008F ₁₆	CAN0 message box 2 : Time stamp		?? ₁₆ ?? ₁₆
0090 ₁₆ 0091 ₁₆ 0092 ₁₆ 0093 ₁₆ 0094 ₁₆ 0095 ₁₆	CAN0 message box 3 : Identifier/DLC		XX?????? ₂ XX?????? ₂ ?? ₁₆ X? ₁₆ X? ₁₆ XX?????? ₂
0096 ₁₆ 0097 ₁₆ 0098 ₁₆ 0099 ₁₆ 009A ₁₆ 009B ₁₆ 009C ₁₆ 009D ₁₆	CAN0 message box 3 : Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
009E ₁₆ 009F ₁₆	CAN0 message box 3 : Time stamp		?? ₁₆ ?? ₁₆
00A0 ₁₆ 00A1 ₁₆ 00A2 ₁₆ 00A3 ₁₆ 00A4 ₁₆ 00A5 ₁₆	CAN0 message box 4: Identifier/DLC		XX?????? ₂ XX?????? ₂ ?? ₁₆ X? ₁₆ X? ₁₆ XX?????? ₂
00A6 ₁₆ 00A7 ₁₆ 00A8 ₁₆ 00A9 ₁₆ 00AA ₁₆ 00AB ₁₆ 00AC ₁₆ 00AD ₁₆	CAN0 message box 4 : Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
00AE ₁₆ 00AF ₁₆	CAN0 message box 4 : Time stamp		?? ₁₆ ?? ₁₆
00B0 ₁₆ 00B1 ₁₆ 00B2 ₁₆ 00B3 ₁₆ 00B4 ₁₆ 00B5 ₁₆	CAN0 message box 5 : Identifier/DLC		XX?????? ₂ XX?????? ₂ ?? ₁₆ X? ₁₆ X? ₁₆ XX?????? ₂
00B6 ₁₆ 00B7 ₁₆ 00B8 ₁₆ 00B9 ₁₆ 00BA ₁₆ 00BB ₁₆ 00BC ₁₆ 00BD ₁₆	CAN0 message box 5 : Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
00BE ₁₆ 00BF ₁₆	CAN0 message box 5 : Time stamp		?? ₁₆ ?? ₁₆

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.3. SFR Map (3 of 11)

Address	Register	Symbol	After reset
00C0 ₁₆ 00C1 ₁₆ 00C2 ₁₆ 00C3 ₁₆ 00C4 ₁₆ 00C5 ₁₆	CAN0 message box 6: Identifier/DLC		XX?????2 XX?????2 ?? ₁₆ X? ₁₆ X? ₁₆ XX?????2
00C6 ₁₆ 00C7 ₁₆ 00C8 ₁₆ 00C9 ₁₆ 00CA ₁₆ 00CB ₁₆ 00CC ₁₆ 00CD ₁₆	CAN0 message box 6 : Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
00CE ₁₆ 00CF ₁₆	CAN0 message box 6 : Time stamp		?? ₁₆ ?? ₁₆
00D0 ₁₆ 00D1 ₁₆ 00D2 ₁₆ 00D3 ₁₆ 00D4 ₁₆ 00D5 ₁₆	CAN0 message box 7 : Identifier/DLC		XX?????2 XX?????2 ?? ₁₆ X? ₁₆ X? ₁₆ XX?????2
00D6 ₁₆ 00D7 ₁₆ 00D8 ₁₆ 00D9 ₁₆ 00DA ₁₆ 00DB ₁₆ 00DC ₁₆ 00DD ₁₆	CAN0 message box 7 : Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
00DE ₁₆ 00DF ₁₆	CAN0 message box 7 : Time stamp		?? ₁₆ ?? ₁₆
00E0 ₁₆ 00E1 ₁₆	CAN0 message box 8: Identifier/DLC		XX?????2 XX?????2
00E2 ₁₆ 00E3 ₁₆ 00E4 ₁₆ 00E5 ₁₆			?? ₁₆ X? ₁₆ X? ₁₆ XX?????2
00E6 ₁₆ 00E7 ₁₆ 00E8 ₁₆ 00E9 ₁₆ 00EA ₁₆ 00EB ₁₆ 00EC ₁₆ 00ED ₁₆	CAN0 message box 8: Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
00EE ₁₆ 00EF ₁₆	CAN0 message box 8 : Time stamp		?? ₁₆ ?? ₁₆
00F0 ₁₆ 00F1 ₁₆ 00F2 ₁₆ 00F3 ₁₆ 00F4 ₁₆ 00F5 ₁₆	CAN0 message box 9 : Identifier/DLC		XX?????2 XX?????2 ?? ₁₆ X? ₁₆ X? ₁₆ XX?????2
00F6 ₁₆ 00F7 ₁₆ 00F8 ₁₆ 00F9 ₁₆ 00FA ₁₆ 00FB ₁₆ 00FC ₁₆ 00FD ₁₆	CAN0 message box 9 : Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
00FE ₁₆ 00FF ₁₆	CAN0 message box 9 : Time stamp		?? ₁₆ ?? ₁₆

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.4. SFR Map (4 of 11)

Address	Register	Symbol	After reset
0100 ₁₆ 0101 ₁₆ 0102 ₁₆ 0103 ₁₆ 0104 ₁₆ 0105 ₁₆	CAN0 message box 10: Identifier/DLC		XX?????2 XX?????2 ?? ₁₆ X? ₁₆ X? ₁₆ XX?????2
0106 ₁₆ 0107 ₁₆ 0108 ₁₆ 0109 ₁₆ 010A ₁₆ 010B ₁₆ 010C ₁₆ 010D ₁₆	CAN0 message box 10 : Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
010E ₁₆ 010F ₁₆	CAN0 message box 10 : Time stamp		?? ₁₆ ?? ₁₆
0110 ₁₆ 0111 ₁₆ 0112 ₁₆ 0113 ₁₆ 0114 ₁₆ 0115 ₁₆	CAN0 message box 11 : Identifier/DLC		XX?????2 XX?????2 ?? ₁₆ X? ₁₆ X? ₁₆ XX?????2
0116 ₁₆ 0117 ₁₆ 0118 ₁₆ 0119 ₁₆ 011A ₁₆ 011B ₁₆ 011C ₁₆ 011D ₁₆	CAN0 message box 11 : Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
011E ₁₆ 011F ₁₆	CAN0 message box 11 : Time stamp		?? ₁₆ ?? ₁₆
0120 ₁₆ 0121 ₁₆ 0122 ₁₆ 0123 ₁₆ 0124 ₁₆ 0125 ₁₆	CAN0 message box 12: Identifier/DLC		XX?????2 XX?????2 ?? ₁₆ X? ₁₆ X? ₁₆ XX?????2
0126 ₁₆ 0127 ₁₆ 0128 ₁₆ 0129 ₁₆ 012A ₁₆ 012B ₁₆ 012C ₁₆ 012D ₁₆	CAN0 message box 12: Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
012E ₁₆ 012F ₁₆	CAN0 message box 12 : Time stamp		?? ₁₆ ?? ₁₆
0130 ₁₆ 0131 ₁₆ 0132 ₁₆ 0133 ₁₆ 0134 ₁₆ 0135 ₁₆	CAN0 message box 13 : Identifier/DLC		XX?????2 XX?????2 ?? ₁₆ X? ₁₆ X? ₁₆ XX?????2
0136 ₁₆ 0137 ₁₆ 0138 ₁₆ 0139 ₁₆ 013A ₁₆ 013B ₁₆ 013C ₁₆ 013D ₁₆	CAN0 message box 13 : Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
013E ₁₆ 013F ₁₆	CAN0 message box 13 : Time stamp		?? ₁₆ ?? ₁₆

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.5. SFR Map (5 of 11)

Address	Register	Symbol	After reset
0140 ₁₆ 0141 ₁₆ 0142 ₁₆ 0143 ₁₆ 0144 ₁₆ 0145 ₁₆	CAN0 message box 14: Identifier/DLC		XX?????? ₂ XX?????? ₂ ?? ₁₆ X? ₁₆ X? ₁₆ XX?????? ₂
0146 ₁₆ 0147 ₁₆ 0148 ₁₆ 0149 ₁₆ 014A ₁₆ 014B ₁₆ 014C ₁₆ 014D ₁₆	CAN0 message box 14 : Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
014E ₁₆ 014F ₁₆	CAN0 message box 14 : Time stamp		?? ₁₆ ?? ₁₆
0150 ₁₆ 0151 ₁₆ 0152 ₁₆ 0153 ₁₆ 0154 ₁₆ 0155 ₁₆	CAN0 message box 15 : Identifier/DLC		XX?????? ₂ XX?????? ₂ ?? ₁₆ X? ₁₆ X? ₁₆ XX?????? ₂
0156 ₁₆ 0157 ₁₆ 0158 ₁₆ 0159 ₁₆ 015A ₁₆ 015B ₁₆ 015C ₁₆ 015D ₁₆	CAN0 message box 15 : Data field		?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆ ?? ₁₆
015E ₁₆ 015F ₁₆	CAN0 message box 15 : Time stamp		?? ₁₆ ?? ₁₆
0160 ₁₆ 0161 ₁₆ 0162 ₁₆ 0163 ₁₆ 0164 ₁₆ 0165 ₁₆	CAN0 global mask register	COGMR	XX?????? ₂ XX?????? ₂ ?? ₁₆ X? ₁₆ XX ₁₆ XX?????? ₂
0166 ₁₆ 0167 ₁₆ 0168 ₁₆ 0169 ₁₆ 016A ₁₆ 016B ₁₆	CAN0 local mask A register	COLMAR	XX?????? ₂ XX?????? ₂ ?? ₁₆ X? ₁₆ XX ₁₆ XX?????? ₂
016C ₁₆ 016D ₁₆ 016E ₁₆ 016F ₁₆ 0170 ₁₆ 0171 ₁₆	CAN0 local mask B register	COLMBR	XX?????? ₂ XX?????? ₂ ?? ₁₆ X? ₁₆ XX ₁₆ XX?????? ₂
~			
01B3 ₁₆ 01B4 ₁₆	Flash memory control register 4 (Note 2)	FMR4	0100000X ₂
01B5 ₁₆ 01B6 ₁₆	Flash memory control register 1 (Note 2)	FMR1	000???0? ₂
01B7 ₁₆	Flash memory control register 0 (Note 2)	FMR0	01 ₁₆
~			
01FD ₁₆ 01FE ₁₆ 01FF ₁₆			

Note 1: The blank areas are reserved and cannot be used by users.
Note 2: This register is included in the flash memory version.

X :Nothing is mapped to this bit
? : Undefined

Figure 4.6. SFR Map (6 of 11)

Address	Register	Symbol	After reset
0200 ₁₆	CAN0 message control register 0	COMCTL0	00 ₁₆
0201 ₁₆	CAN0 message control register 1	COMCTL1	00 ₁₆
0202 ₁₆	CAN0 message control register 2	COMCTL2	00 ₁₆
0203 ₁₆	CAN0 message control register 3	COMCTL3	00 ₁₆
0204 ₁₆	CAN0 message control register 4	COMCTL4	00 ₁₆
0205 ₁₆	CAN0 message control register 5	COMCTL5	00 ₁₆
0206 ₁₆	CAN0 message control register 6	COMCTL6	00 ₁₆
0207 ₁₆	CAN0 message control register 7	COMCTL7	00 ₁₆
0208 ₁₆	CAN0 message control register 8	COMCTL8	00 ₁₆
0209 ₁₆	CAN0 message control register 9	COMCTL9	00 ₁₆
020A ₁₆	CAN0 message control register 10	COMCTL10	00 ₁₆
020B ₁₆	CAN0 message control register 11	COMCTL11	00 ₁₆
020C ₁₆	CAN0 message control register 12	COMCTL12	00 ₁₆
020D ₁₆	CAN0 message control register 13	COMCTL13	00 ₁₆
020E ₁₆	CAN0 message control register 14	COMCTL14	00 ₁₆
020F ₁₆	CAN0 message control register 15	COMCTL15	00 ₁₆
0210 ₁₆	CAN0 control register	COCTLR	X0000001 ₂ XX0X0000 ₂
0211 ₁₆			
0212 ₁₆	CAN0 status register	C0STR	00 ₁₆
0213 ₁₆			X0000001 ₂
0214 ₁₆	CAN0 slot status register	C0SSTR	00 ₁₆
0215 ₁₆			00 ₁₆
0216 ₁₆	CAN0 interrupt control register	C0ICR	00 ₁₆
0217 ₁₆			00 ₁₆
0218 ₁₆	CAN0 extended ID register	C0IDR	00 ₁₆
0219 ₁₆			00 ₁₆
021A ₁₆	CAN0 configuration register	C0CONR	?? ₁₆
021B ₁₆			?? ₁₆
021C ₁₆	CAN0 receive error count register	C0RECR	00 ₁₆
021D ₁₆	CAN0 transmit error count register	C0TECR	00 ₁₆
021E ₁₆	CAN0 time stamp register	C0TSR	00 ₁₆
021F ₁₆			00 ₁₆
≈			
0242 ₁₆	CAN0 acceptance filter support register	C0AFS	?? ₁₆
0243 ₁₆			?? ₁₆
≈			
025A ₁₆	Three-phase protect control register	TPRC	00 ₁₆
025B ₁₆			
025C ₁₆	On-chip oscillator control register	ROCR	00000101 ₂
025D ₁₆	Pin assignment control register	PACR	00 ₁₆
025E ₁₆	Peripheral clock select register	PCLKR	00000011 ₂
025F ₁₆	CAN0 clock select register	CCLKR	00 ₁₆
≈			
02E0 ₁₆	I ² C0 data-shift register	S00	?? ₁₆
02E1 ₁₆			
02E2 ₁₆	I ² C0 address register	S0D0	00 ₁₆
02E3 ₁₆	I ² C0 control register 0	S1D0	00 ₁₆
02E4 ₁₆	I ² C0 clock control register	S20	00 ₁₆
02E5 ₁₆	I ² C0 start/stop condition control register	S2D0	00011010 ₂
02E6 ₁₆	I ² C0 control register 1	S3D0	00110000 ₂
02E7 ₁₆	I ² C0 control register 2	S4D0	00 ₁₆
02E8 ₁₆	I ² C0 status register	S10	0001000X ₂
≈			
02FD ₁₆			
02FE ₁₆			
02FF ₁₆			

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.7. SFR Map (7 of 11)

Address	Register	Symbol	After reset
0300 ₁₆ 0301 ₁₆	Time measurement, Pulse generation register 0	G1TM0,G1PO0	?? ₁₆ ?? ₁₆
0302 ₁₆ 0303 ₁₆	Time measurement, Pulse generation register 1	G1TM1,G1PO1	?? ₁₆ ?? ₁₆
0304 ₁₆ 0305 ₁₆	Time measurement, Pulse generation register 2	G1TM2,G1PO2	?? ₁₆ ?? ₁₆
0306 ₁₆ 0307 ₁₆	Time measurement, Pulse generation register 3	G1TM3,G1PO3	?? ₁₆ ?? ₁₆
0308 ₁₆ 0309 ₁₆	Time measurement, Pulse generation register 4	G1TM4,G1PO4	?? ₁₆ ?? ₁₆
030A ₁₆ 030B ₁₆	Time measurement, Pulse generation register 5	G1TM5,G1PO5	?? ₁₆ ?? ₁₆
030C ₁₆ 030D ₁₆	Time measurement, Pulse generation register 6	G1TM6,G1PO6	?? ₁₆ ?? ₁₆
030E ₁₆ 030F ₁₆	Time measurement, Pulse generation register 7	G1TM7,G1PO7	?? ₁₆ ?? ₁₆
0310 ₁₆	Pulse generation control register 0	G1POCR0	0X00XX00 ₂
0311 ₁₆	Pulse generation control register 1	G1POCR1	0X00XX00 ₂
0312 ₁₆	Pulse generation control register 2	G1POCR2	0X00XX00 ₂
0313 ₁₆	Pulse generation control register 3	G1POCR3	0X00XX00 ₂
0314 ₁₆	Pulse generation control register 4	G1POCR4	0X00XX00 ₂
0315 ₁₆	Pulse generation control register 5	G1POCR5	0X00XX00 ₂
0316 ₁₆	Pulse generation control register 6	G1POCR6	0X00XX00 ₂
0317 ₁₆	Pulse generation control register 7	G1POCR7	0X00XX00 ₂
0318 ₁₆	Time measurement control register 0	G1TMCR0	00 ₁₆
0319 ₁₆	Time measurement control register 1	G1TMCR1	00 ₁₆
031A ₁₆	Time measurement control register 2	G1TMCR2	00 ₁₆
031B ₁₆	Time measurement control register 3	G1TMCR3	00 ₁₆
031C ₁₆	Time measurement control register 4	G1TMCR4	00 ₁₆
031D ₁₆	Time measurement control register 5	G1TMCR5	00 ₁₆
031E ₁₆	Time measurement control register 6	G1TMCR6	00 ₁₆
031F ₁₆	Time measurement control register 7	G1TMCR7	00 ₁₆
0320 ₁₆ 0321 ₁₆	Base timer register	G1BT	?? ₁₆ ?? ₁₆
0322 ₁₆	Base timer control register 0	G1BCR0	00 ₁₆
0323 ₁₆	Base timer control register 1	G1BCR1	00 ₁₆
0324 ₁₆	Time measurement prescale register 6	G1TPR6	00 ₁₆
0325 ₁₆	Time measurement prescale register 7	G1TPR7	00 ₁₆
0326 ₁₆	Function enable register	G1FE	00 ₁₆
0327 ₁₆	Function select register	G1FS	00 ₁₆
0328 ₁₆ 0329 ₁₆	Base timer reset register	G1BTRR	?? ₁₆ ?? ₁₆
032A ₁₆ 032B ₁₆	Count source division register	G1DV	00 ₁₆
032C ₁₆			
032D ₁₆			
032E ₁₆			
032F ₁₆			
0330 ₁₆	Interrupt request register	G1IR	?? ₁₆
0331 ₁₆	Interrupt enable register 0	G1IE0	00 ₁₆
0332 ₁₆	Interrupt enable register 1	G1IE1	00 ₁₆
0333 ₁₆			
0334 ₁₆			
0335 ₁₆			
0336 ₁₆			
0337 ₁₆			
0338 ₁₆			
0339 ₁₆			
033A ₁₆			
033B ₁₆			
033C ₁₆			
033D ₁₆			
033E ₁₆	NMI digital debounce register	NDDR	FF ₁₆
033F ₁₆	Port P17 digital debounce register	P17DDR	FF ₁₆

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.8. SFR Map (8 of 11)

Address	Register	Symbol	After reset
0340 ₁₆			
0341 ₁₆			
0342 ₁₆	Timer A1-1 register	TA11	?? ₁₆
0343 ₁₆			?? ₁₆
0344 ₁₆	Timer A2-1 register	TA21	?? ₁₆
0345 ₁₆			?? ₁₆
0346 ₁₆	Timer A4-1 register	TA41	?? ₁₆
0347 ₁₆			?? ₁₆
0348 ₁₆	Three phase PWM control register 0	INVC0	00 ₁₆
0349 ₁₆	Three phase PWM control register 1	INVC1	00 ₁₆
034A ₁₆	Three phase output buffer register 0	IDB0	00 ₁₆
034B ₁₆	Three phase output buffer register 1	IDB1	00 ₁₆
034C ₁₆	Dead time timer	DTT	?? ₁₆
034D ₁₆	Timer B2 Interrupt occurrence frequency set counter	ICTB2	?? ₁₆
034E ₁₆	Position - data - retain function control register	PDRF	XXXX0000 ₂
034F ₁₆			
0350 ₁₆			
0351 ₁₆			
0352 ₁₆			
0353 ₁₆			
0354 ₁₆			
0355 ₁₆			
0356 ₁₆			
0357 ₁₆			
0358 ₁₆	Port function control register	PFCR	00111111 ₂
0359 ₁₆			
035A ₁₆			
035B ₁₆			
035C ₁₆			
035D ₁₆			
035E ₁₆	Interrupt cause select register 2	IFSR2A	00XX0000 ₂
035F ₁₆	Interrupt cause select register	IFSR	00 ₁₆
0360 ₁₆	SI/O3 transmit/receive register	S3TRR	?? ₁₆
0361 ₁₆			
0362 ₁₆	SI/O3 control register	S3C	01000000 ₂
0363 ₁₆	SI/O3 bit rate register	S3BRG	?? ₁₆
0364 ₁₆	SI/O4 transmit/receive register	S4TRR	?? ₁₆
0365 ₁₆			
0366 ₁₆	SI/O4 control register	S4C	01000000 ₂
0367 ₁₆	SI/O4 bit rate register	S4BRG	?? ₁₆
0368 ₁₆			
0369 ₁₆			
036A ₁₆			
036B ₁₆			
036C ₁₆			
036D ₁₆			
036E ₁₆			
036F ₁₆			
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆	UART2 special mode register 4	U2SMR4	00 ₁₆
0375 ₁₆	UART2 special mode register 3	U2SMR3	000X0X0X ₂
0376 ₁₆	UART2 special mode register 2	U2SMR2	X0000000 ₂
0377 ₁₆	UART2 special mode register	U2SMR	X0000000 ₂
0378 ₁₆	UART2 transmit/receive mode register	U2MR	00 ₁₆
0379 ₁₆	UART2 bit rate register	U2BRG	?? ₁₆
037A ₁₆	UART2 transmit buffer register	U2TB	??????? ₂
037B ₁₆			XXXXXXX ₂
037C ₁₆	UART2 transmit/receive control register 0	U2C0	00001000 ₂
037D ₁₆	UART2 transmit/receive control register 1	U2C1	00000010 ₂
037E ₁₆	UART2 receive buffer register	U2RB	??????? ₂
037F ₁₆			?????XX ₂

Note 1 :The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.9. SFR Map (9 of 11)

Address	Register	Symbol	After reset
0380 ₁₆	Count start flag	TABSR	00 ₁₆
0381 ₁₆	Clock prescaler reset flag	CPSRF	0XXXXXX ₂
0382 ₁₆	One-shot start flag	ONSF	00 ₁₆
0383 ₁₆	Trigger select register	TRGSR	00 ₁₆
0384 ₁₆	Up-down flag	UDF	00 ₁₆
0385 ₁₆			
0386 ₁₆	Timer A0 register	TA0	?? ₁₆
0387 ₁₆			?? ₁₆
0388 ₁₆	Timer A1 register	TA1	?? ₁₆
0389 ₁₆			?? ₁₆
038A ₁₆	Timer A2 register	TA2	?? ₁₆
038B ₁₆			?? ₁₆
038C ₁₆	Timer A3 register	TA3	?? ₁₆
038D ₁₆			?? ₁₆
038E ₁₆	Timer A4 register	TA4	?? ₁₆
038F ₁₆			?? ₁₆
0390 ₁₆	Timer B0 register	TB0	?? ₁₆
0391 ₁₆			?? ₁₆
0392 ₁₆	Timer B1 register	TB1	?? ₁₆
0393 ₁₆			?? ₁₆
0394 ₁₆	Timer B2 register	TB2	?? ₁₆
0395 ₁₆			?? ₁₆
0396 ₁₆	Timer A0 mode register	TA0MR	00 ₁₆
0397 ₁₆	Timer A1 mode register	TA1MR	00 ₁₆
0398 ₁₆	Timer A2 mode register	TA2MR	00 ₁₆
0399 ₁₆	Timer A3 mode register	TA3MR	00 ₁₆
039A ₁₆	Timer A4 mode register	TA4MR	00 ₁₆
039B ₁₆	Timer B0 mode register	TB0MR	00??0000 ₂
039C ₁₆	Timer B1 mode register	TB1MR	00?X0000 ₂
039D ₁₆	Timer B2 mode register	TB2MR	00?X0000 ₂
039E ₁₆	Timer B2 special mode register	TB2SC	X0000000 ₂
039F ₁₆			
03A0 ₁₆	UART0 transmit/receive mode register	U0MR	00 ₁₆
03A1 ₁₆	UART0 bit rate register	U0BRG	?? ₁₆
03A2 ₁₆	UART0 transmit buffer register	U0TB	??????? ₂
03A3 ₁₆			XXXXXXX ₂
03A4 ₁₆	UART0 transmit/receive control register 0	U0C0	00001000 ₂
03A5 ₁₆	UART0 transmit/receive control register 1	U0C1	00000010 ₂
03A6 ₁₆	UART0 receive buffer register	U0RB	??????? ₂
03A7 ₁₆			?????XX ₂
03A8 ₁₆	UART1 transmit/receive mode register	U1MR	00 ₁₆
03A9 ₁₆	UART1 bit rate register	U1BRG	?? ₁₆
03AA ₁₆	UART1 transmit buffer register	U1TB	??????? ₂
03AB ₁₆			XXXXXXX ₂
03AC ₁₆	UART1 transmit/receive control register 0	U1C0	00001000 ₂
03AD ₁₆	UART1 transmit/receive control register 1	U1C1	00000010 ₂
03AE ₁₆	UART1 receive buffer register	U1RB	??????? ₂
03AF ₁₆			?????XX ₂
03B0 ₁₆	UART transmit/receive control register 2	UCON	X0000000 ₂
03B1 ₁₆			
03B2 ₁₆			
03B3 ₁₆			
03B4 ₁₆	CRC snoop address register	CRCSAR	?? ₁₆
03B5 ₁₆			00XXXX? ₂
03B6 ₁₆	CRC mode register	CRCMR	0XXXXX0 ₂
03B7 ₁₆			
03B8 ₁₆	DMA0 request cause select register	DM0SL	00 ₁₆
03B9 ₁₆			
03BA ₁₆	DMA1 request cause select register	DM1SL	00 ₁₆
03BB ₁₆			
03BC ₁₆	CRC data register	CRCD	?? ₁₆
03BD ₁₆			?? ₁₆
03BE ₁₆	CRC input register	CRCIN	?? ₁₆
03BF ₁₆			

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.10. SFR Map (10 of 11)

Address	Register	Symbol	After reset
03C0 ₁₆ 03C1 ₁₆	A/D register 0	AD0	???????2 XXXXXX??2
03C2 ₁₆ 03C3 ₁₆	A/D register 1	AD1	???????2 XXXXXX??2
03C4 ₁₆ 03C5 ₁₆	A/D register 2	AD2	???????2 XXXXXX??2
03C6 ₁₆ 03C7 ₁₆	A/D register 3	AD3	???????2 XXXXXX??2
03C8 ₁₆ 03C9 ₁₆	A/D register 4	AD4	???????2 XXXXXX??2
03CA ₁₆ 03CB ₁₆	A/D register 5	AD5	???????2 XXXXXX??2
03CC ₁₆ 03CD ₁₆	A/D register 6	AD6	???????2 XXXXXX??2
03CE ₁₆ 03CF ₁₆	A/D register 7	AD7	???????2 XXXXXX??2
03D0 ₁₆ 03D1 ₁₆			
03D2 ₁₆	A/D trigger control register	ADTRGCON	XXXX0000 ₂
03D3 ₁₆	A/D status register 0	ADSTAT0	00000X00 ₂
03D4 ₁₆	A/D control register 2	ADCON2	00 ₁₆
03D5 ₁₆ 03D6 ₁₆	A/D control register 0	ADCON0	00000???2
03D7 ₁₆	A/D control register 1	ADCON1	00 ₁₆
03D8 ₁₆ 03D9 ₁₆			
03DA ₁₆ 03DB ₁₆			
03DC ₁₆ 03DD ₁₆			
03DE ₁₆ 03DF ₁₆			
03E0 ₁₆	Port P0 register	P0	?? ₁₆
03E1 ₁₆	Port P1 register	P1	?? ₁₆
03E2 ₁₆	Port P0 direction register	PD0	00 ₁₆
03E3 ₁₆	Port P1 direction register	PD1	00 ₁₆
03E4 ₁₆	Port P2 register	P2	?? ₁₆
03E5 ₁₆	Port P3 register	P3	?? ₁₆
03E6 ₁₆	Port P2 direction register	PD2	00 ₁₆
03E7 ₁₆	Port P3 direction register	PD3	00 ₁₆
03E8 ₁₆ 03E9 ₁₆			
03EA ₁₆ 03EB ₁₆			
03EC ₁₆	Port P6 register	P6	?? ₁₆
03ED ₁₆	Port P7 register	P7	?? ₁₆
03EE ₁₆	Port P6 direction register	PD6	00 ₁₆
03EF ₁₆	Port P7 direction register	PD7	00 ₁₆
03F0 ₁₆	Port P8 register	P8	?? ₁₆
03F1 ₁₆	Port P9 register	P9	???X???2
03F2 ₁₆	Port P8 direction register	PD8	00 ₁₆
03F3 ₁₆	Port P9 direction register	PD9	000X0000 ₂
03F4 ₁₆	Port P10 register	P10	?? ₁₆
03F5 ₁₆ 03F6 ₁₆	Port P10 direction register	PD10	00 ₁₆
03F7 ₁₆ 03F8 ₁₆			
03F9 ₁₆ 03FA ₁₆			
03FB ₁₆			
03FC ₁₆	Pull-up control register 0	PUR0	00 ₁₆
03FD ₁₆	Pull-up control register 1	PUR1	00 ₁₆
03FE ₁₆	Pull-up control register 2	PUR2	00 ₁₆
03FF ₁₆	Port control register	PCR	00 ₁₆

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Figure 4.11. SFR Map (11 of 11)

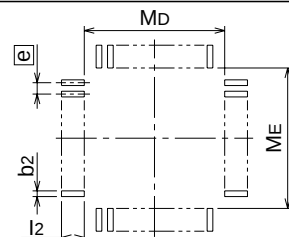
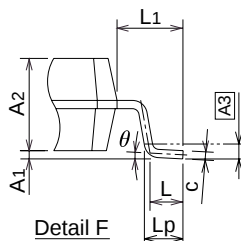
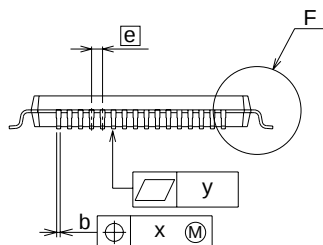
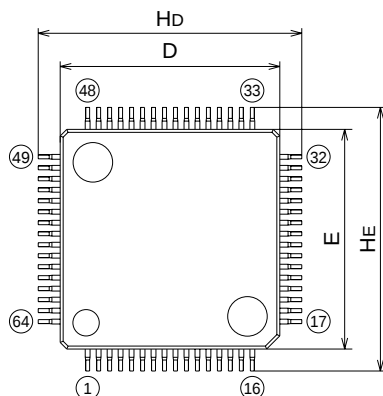
5. Package

64P6Q-A

Recommended

Plastic 64pin 10X10mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1010-0.5	—		Cu Alloy



Recommended Mount Pad

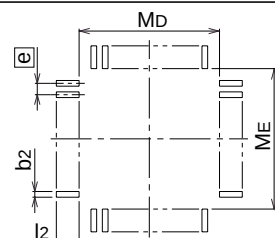
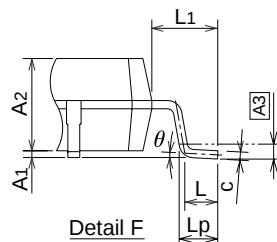
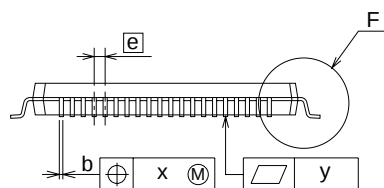
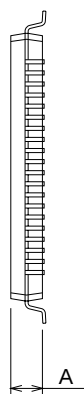
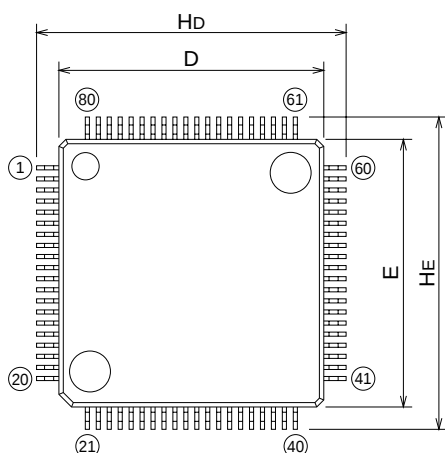
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	9.9	10.0	10.1
E	9.9	10.0	10.1
e	—	0.5	—
Hd	11.8	12.0	12.2
HE	11.8	12.0	12.2
L	0.3	0.5	0.7
L1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.08
y	—	—	0.1
theta	0°	—	10°
b2	—	0.225	—
l2	1.0	—	—
Md	—	10.4	—
ME	—	10.4	—

80P6Q-A

Recommended

Plastic 80pin 12X12mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.5	—	0.47	Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	—	0.5	—
Hd	13.8	14.0	14.2
HE	13.8	14.0	14.2
L	0.3	0.5	0.7
L1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.08
y	—	—	0.1
theta	0°	—	10°
b2	—	0.225	—
l2	0.9	—	—
Md	—	12.4	—
ME	—	12.4	—

6. Functional differences

6.1 Functional differences between Normal-ver. and T-ver./V-ver. of M16C/29 group

Item	Detailed Item	M16C/29(Normal-ver.)	M16C/29(T-ver./V-ver.)
Reset	Voltage Detection Circuit (Function of 001916, 001A16, 001F16)	Available (Power supply detection register 1, Power supply detection register 2, Power supply down detection interrupt register)	Not available (Reserved register)

Note. Refer to Hardware Manual about detail and electrical characteristics.

6.2 Functional differences between M16C/28 group and M16C/29 group (Normal-ver.)

Item	Detailed Item	M16C/28(Normal-ver.)	M16C/29(Normal-ver.)
Clock	Clock Output Function	Not available (reserved bit)	Available (Clock output function select bit)
Protect	PRC0 bit function	Enable write to CM0, CM1, CM2, POCR, PLC0, PCLKR registers	Enable write to CM0, CM1, CM2, POCR, PLC0, PCLKR, CCLKR registers
Interrupt	IFSR20 bit of IFSR2A register	Must be set to "1"	Must be set to "0"
	b1 bit of IFSR2A register	Nothing is assigned (When write, set to "0")	Interrupt request cause select bit (0:A/D conversion 1:Key input)
	b2 bit of IFSR2A register	Nothing is assigned (When write, set to "0")	Interrupt request cause select bit (0:CAN0 wakeup/error)
	Interrupr source of software interrupt number 13	Key input interrupt	CAN0 error
	Interrupr source of software interrupt number 14	A/D conversion interrupt	A/D conversion/Key input interrupt
Three-Phase Motor Control Timer	Three-phase/Port Output Switch Function (035816)	Not available (Nothing is assigned)	Available (Port function control register)
A/D Conversion	Analog Input pins	24 channels (AN30 to AN32 not available)	27 channels (AN30 to AN32 available)
	Delayed trigger mode 0	The product of the first edition and version A do not available	Available
	Delayed trigger mode 1	The product of the first edition and version A do not available	Available
CAN Module	2.0B BOSCH compliant	Not available (Related registers are not assigned)	Available (1channel)
CRC Calculation	CRC-CCITT and CRC-16	Not available (Related registers are not assigned)	Available (1 curcuit)
Pin Function	2 pin (80 pin version) 62 pin (64 pin version)	P93/AN24	P93/AN24/CTX
	3 pin (80 pin version) 64 pin (64 pin version)	P92/TB2IN	P92/AN32/TB2IN/CRX
	4 pin (80 pin version) 1 pin (64 pin version)	P91/TB1IN	P91/AN31/TB1IN
	5 pin (80 pin version) 2 pin (64 pin version)	P90/TB0IN	P90/AN30/TB0IN/CLKOUT

Note. Refer to Hardware Manual about detail and electrical characteristics.

6.3 Functional differences between M16C/28 group and M16C/29 group (T-ver./V-ver.)

Item	Detailed Item	M16C/28(T-ver./V-ver.)	M16C/29(T-ver./V-ver.)
Protect	PRC0 bit function	Enable write to CM0, CM1, CM2, POCCR, PLC0, PCLKR registers	Enable write to CM0, CM1, CM2, POCCR, PLC0, PCLKR, CCLKR registers
Interrupt	IFSR20 bit of IFSR2A register	Must be set to "1"	Must be set to "0"
	b1 bit of IFSR2A register	Nothing is assigned (When write, set to "0")	Interrupt request cause select bit (0:A/D conversion 1:Key input)
	b2 bit of IFSR2A register	Nothing is assigned (When write, set to "0")	Interrupt request cause select bit (0:CAN0 wakeup/error)
	Interrupr source of software interrupt number 13	Key input interrupt	CAN0 error
	Interrupr source of software interrupt number 14	A/D conversion interrupt	A/D conversion/Key input interrupt
CAN Module	2.0B BOSCH compliant	Not available (Related registers are not assigned)	Available (1channel)
Pin Function	2 pin (80 pin version) 62 pin (64 pin version)	P93/AN24	P93/AN24/CTX
	3 pin (80 pin version) 64 pin (64 pin version)	P92/TB2IN	P92/AN32/TB2IN/CRX

Note. Refer to Hardware Manual about detail and electrical characteristics.

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