February 2nd, 2010

Automotive Grade
AUIRS211(7,8)S
SINGLE CHANNEL DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- CMOS Schmitt-triggered inputs with pull-down (AUIRS2117) or pull-up (AUIRS2118)
- Output in phase with input (AUIRS2117) or out of Phase with input (AUIRS2118)
- Leadfree, RoHS compliant
- Automotive qualified*

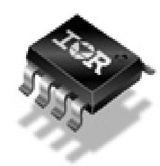
Typical Applications

- Direct/Piezo injection
- BLDC Motor Drive
- MOSFET and IGBT drivers

Product Summary

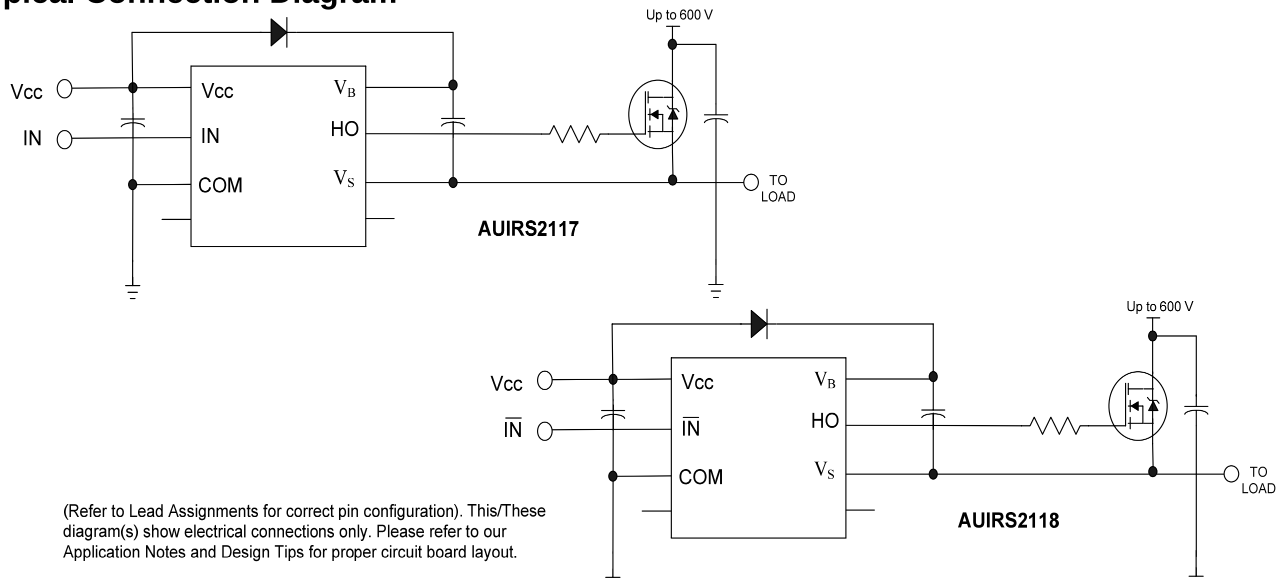
Topology	Single High Side
V_{OFFSET}	≤ 600 V
V_{OUT}	10 V – 20 V
I_{o+} & I_{o-} (typical)	290 mA & 600 mA
t_{ON} & t_{OFF} (typical)	140 ns & 140 ns

Package Options



8-Lead SOIC

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

* Qualification standards can be found on IR's web site www.irf.com

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Description

The AUIRS2117S/AUIRS2118S are high voltage, high speed power MOSFET and IGBT drivers. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high- side or low-side configuration which operates up to 600 V.

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Qualification Information†

Qualification Level		Automotive (per AEC-Q100††)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOIC8N	MSL3††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M2 (Pass +/-200V) (per AEC-Q100-003)	
	Human Body Model	Class H1B (Pass +/-1000V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (Pass +/-1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level A (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/
†† Exceptions to AEC-Q100 requirements are noted in the qualification report.
††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM lead. Stresses beyond those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	-0.3	625	V
V_S	High-side floating supply offset voltage	V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Logic supply voltage	-0.3	25	
V_{IN}	Logic input voltage	0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient (Fig. 2)	—	50	V/ns
P_D	Package power dissipation @ TA ≤ 25°C	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	—	200	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15 V differential.

Symbol	Definition	Min	Max	Units
V_B	High-side floating supply absolute voltage	V_S +10	V_S +20	V
V_S	High-side floating supply offset voltage	†	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Logic supply voltage	10	20	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

† Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to – V_{BS}.
(Please refer to the Design Tip DT97-3 for more details).

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Static Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤ 125°C with bias conditions of V_{BIAS} (V_{CC}, V_{BS}) = 15 V. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO.

Symbol	Definition		Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" input voltage	AUIRS2117	9.5	—	—	V	
		AUIRS2118					
V_{IL}	Logic "0" input voltage	AUIRS2117	—	—	6.0		
		AUIRS2118					
V_{OH}	High level output voltage, V_{BIAS} - V_O		—	0.05	0.2		I_O = 2 mA
V_{OL}	Low level output voltage, V_O†		—	0.02	0.2		
I_{LK}	Offset supply leakage current		—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current		—	50	240		V_{IN} = 0 V or V_{CC}
I_{QCC}	Quiescent V_{CC} supply current		—	70	340		
I_{IN+}	Logic "1" input bias current	AUIRS2117	—	20	40		V_{IN} = V_{CC}
		AUIRS2118					V_{IN} = 0 V
I_{IN-}	Logic "0" input bias current	AUIRS2117	—	—	5.0		V_{IN} = 0 V
		AUIRS2118					V_{IN} = V_{CC}
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold		7.6	8.6	9.6	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold		7.2	8.2	9.2		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold		7.6	8.6	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold		7.2	8.2	9.2		
I_{O+}	Output high short circuit pulsed current		200	290	—	mA	V_O = 0 V, V_{IN} = Logic "1" PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current		420	600	—		V_O = 15 V, V_{IN} = Logic "0" PW ≤ 10 µs

Dynamic Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤ 125°C with bias conditions of V_{BIAS} (V_{CC}, V_{BS}) = 15 V, C_L = 1000 pF. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	140	225	ns	V_S = 0 V
t_{off}	Turn-off propagation delay	—	140	225		V_S = 600 V
t_r	Turn-on rise time	—	75	130		
t_f	Turn-off fall time	—	25	65		

Note: Please refer to figures in Parameter Temperature Trends section

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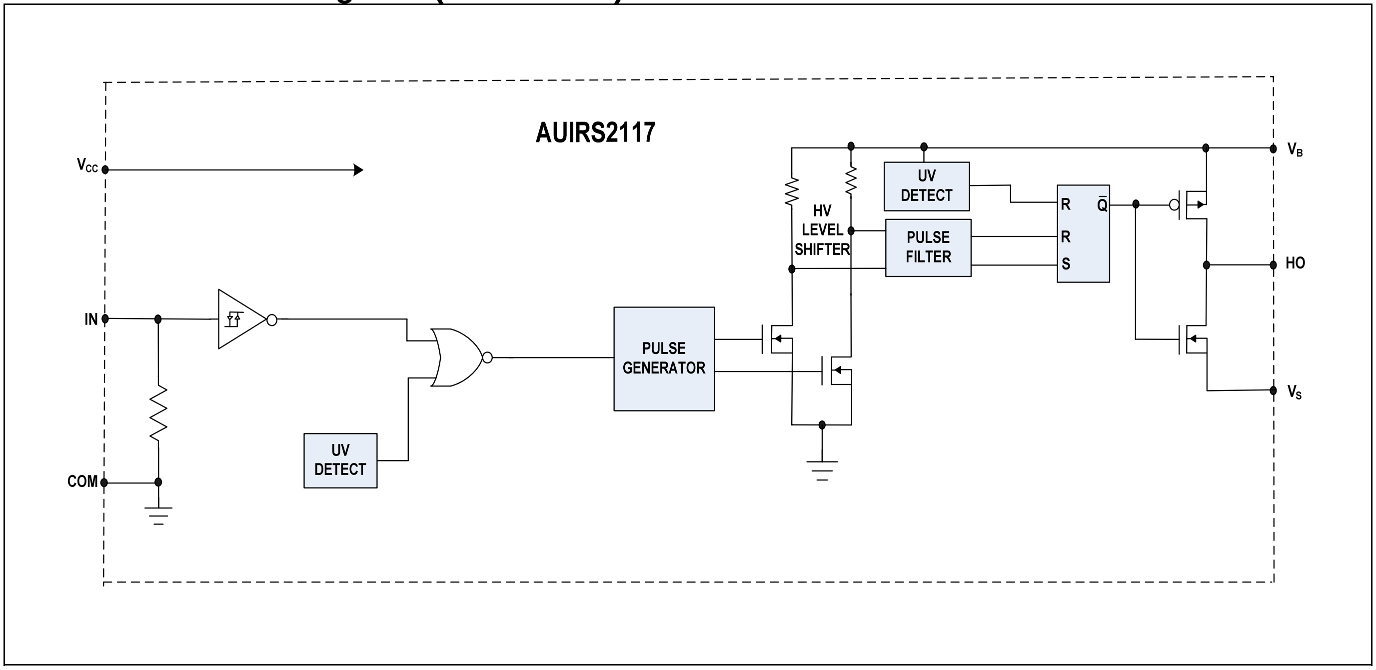
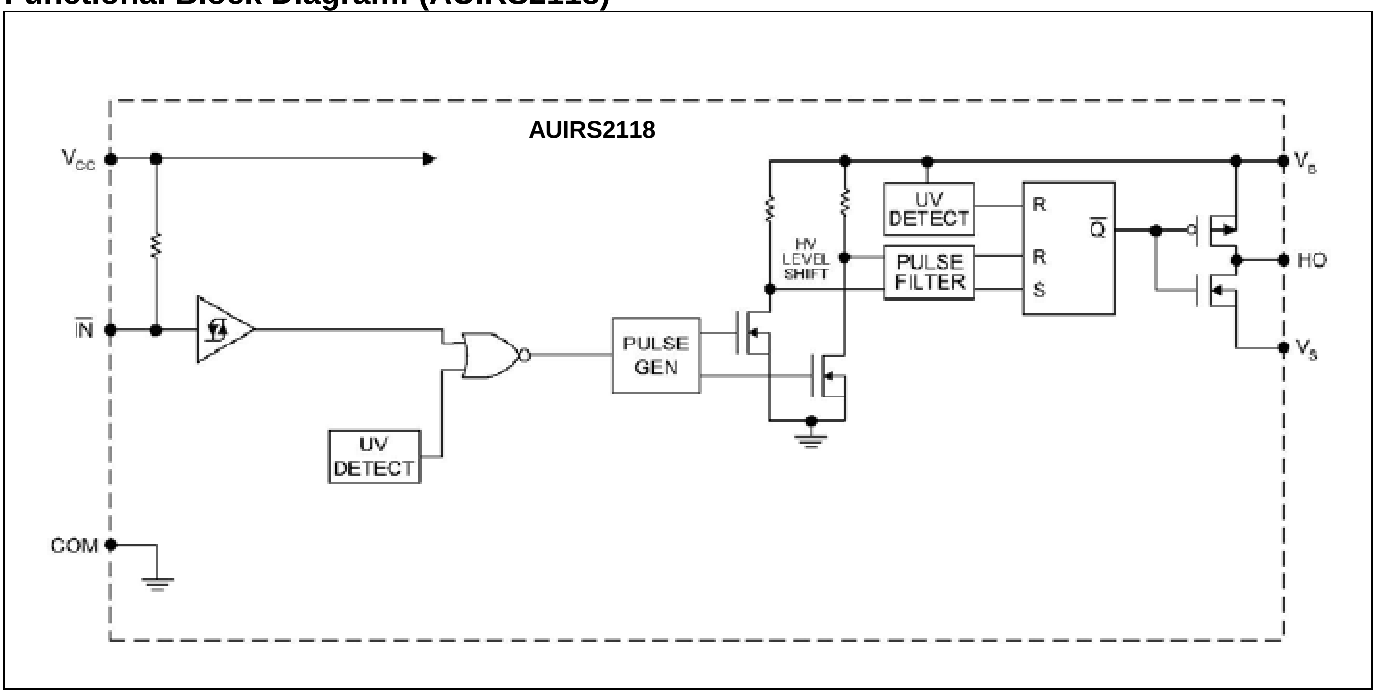
Functional Block Diagram: (AUIRS2117)



Functional Block Diagram: (AUIRS2118)



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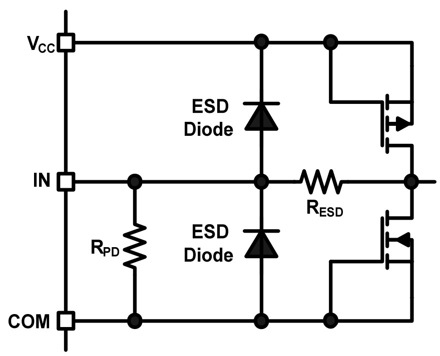
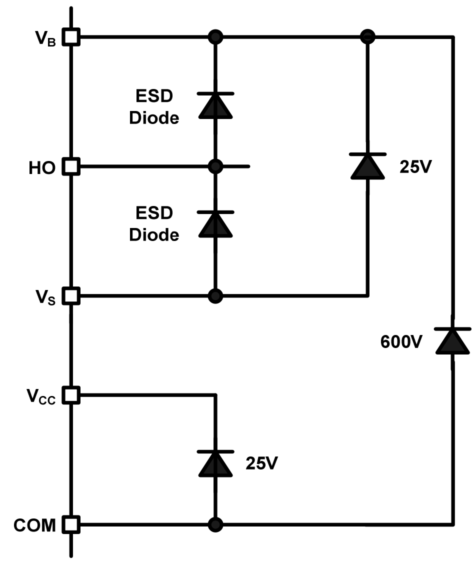
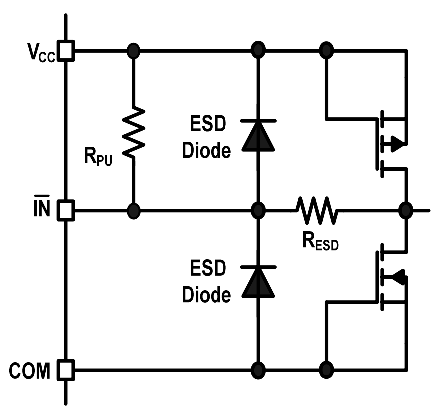
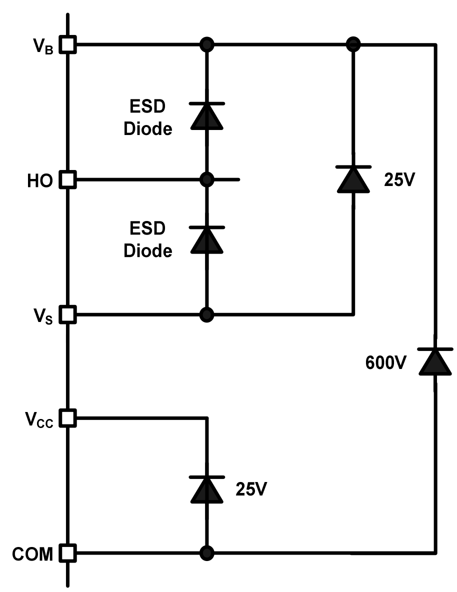
Input/Output Pin Equivalent Circuit Diagrams: AUIRS2117S





Input/Output Pin Equivalent Circuit Diagrams: AUIRS2118S





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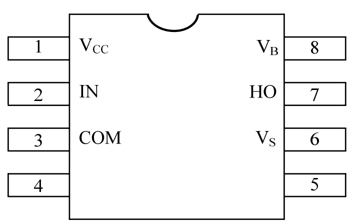
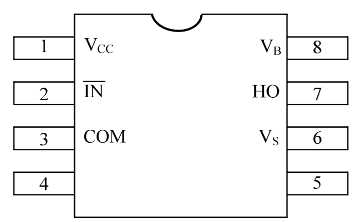
Lead Definitions

PIN	Symbol	Description
1	V_{CC}	Low-side and logic fixed supply
2	IN $\overline{IN}$	Logic input for gate driver output (HO), in phase with HO (AUIRS2117) Logic input for gate driver output (HO), out of phase with HO (AUIRS2118)
3	COM	Logic ground
4	NC	No Connection
5	NC	No Connection
6	V_S	High-side floating supply return
7	HO	High-side gate drive output
8	V_B	High-side floating supply

Lead Assignments



8 Lead SOIC



8 Lead SOIC

AUIRS2117S	AUIRS2118S
Part Number	

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Application Information and Additional Details

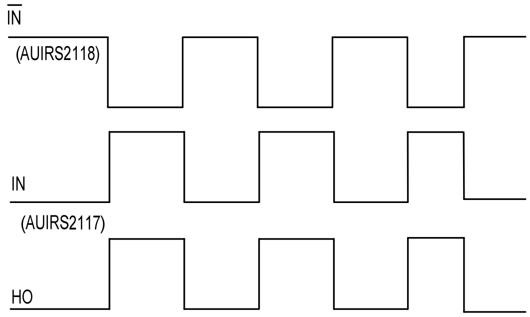

Figure 1: Input/Output Timing Diagram

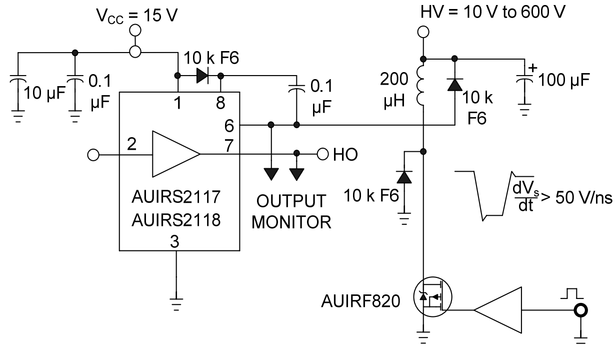

Figure 2: Floating Supply Voltage Transient Test Circuit

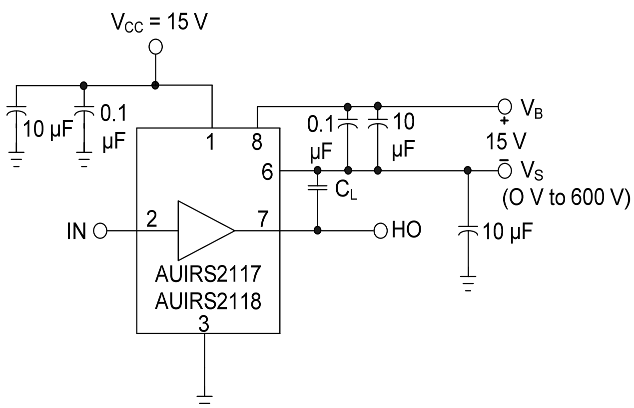

Figure 3: Switching Time Test Circuit

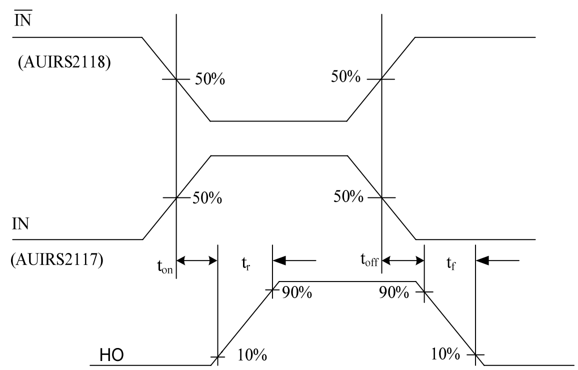

Figure 4: Switching Time Waveform Definition

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Tolerant to Negative V_S Transients

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical half bridge circuit is shown in Figure 5; here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., Q1 in Figures 6 and 7) switches off, while the current is flowing to a load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the inverter. At the same instance, the voltage node V_S swings from the positive DC bus voltage to the negative DC bus voltage.

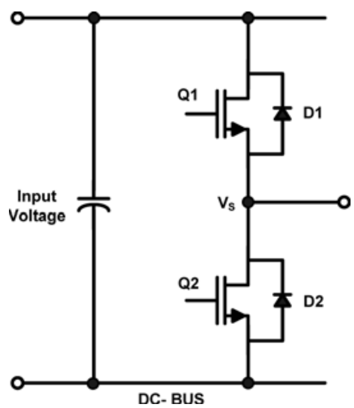

Figure 5: Half Bridge Circuit

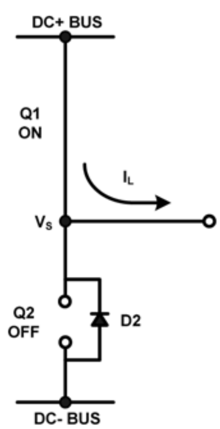

Figure 6: Q1 conducting

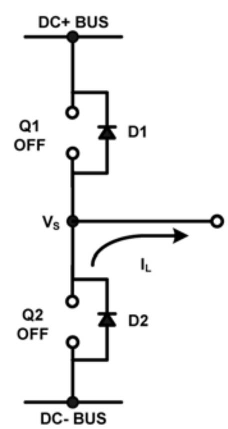

Figure 7: D2 conducting

Also when the current flows from the load back to the inverter (see Figures 8 and 9), and Q2 switches on, the current commutation occurs from D1 to Q2. At the same instance, the voltage node V_S swings from the positive DC bus voltage to the negative DC bus voltage.

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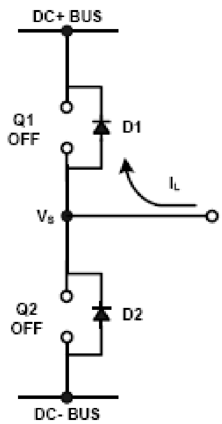

Figure 8: D1 conducting

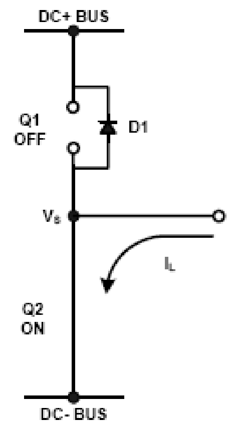

Figure 9: Q2 conducting

However, in a real inverter circuit, the V_S voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called "negative V_S transient".

The circuit shown in Figure 10 depicts a half bridge circuit with parasitic elements shown; Figures 11 and 12 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_D and L_S for each switch. When the high-side switch is on, V_S is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current can momentarily flow in the low-side freewheeling diode due to the inductive load connected to V_S (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_S and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

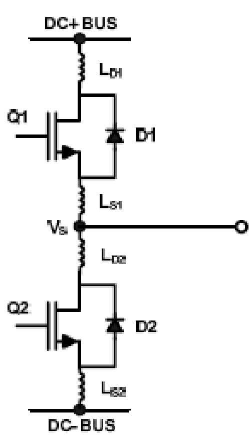

Figure 10: Parasitic Elements

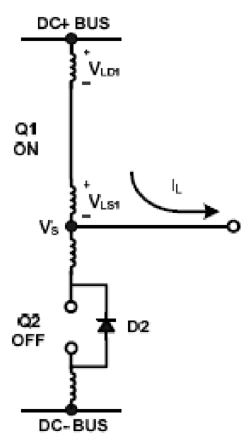

Figure 11: V_S positive

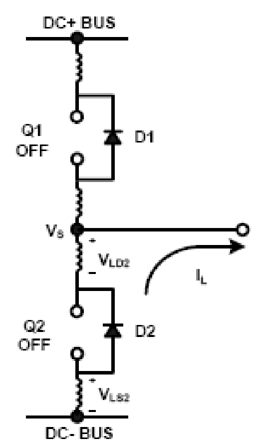

Figure 12: V_S negative

In a typical power circuit, dV/dt is typically designed to be in the range of 1-5 V/ns. The negative V_S transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

International Rectifier's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the AUIRS2117(8)s' robustness can be seen in Figure 13, where there is represented the IRS2117(8)S Safe Operating Area at V_{BS}=15V based on repetitive negative V_S spikes. A negative V_S transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside SOA.

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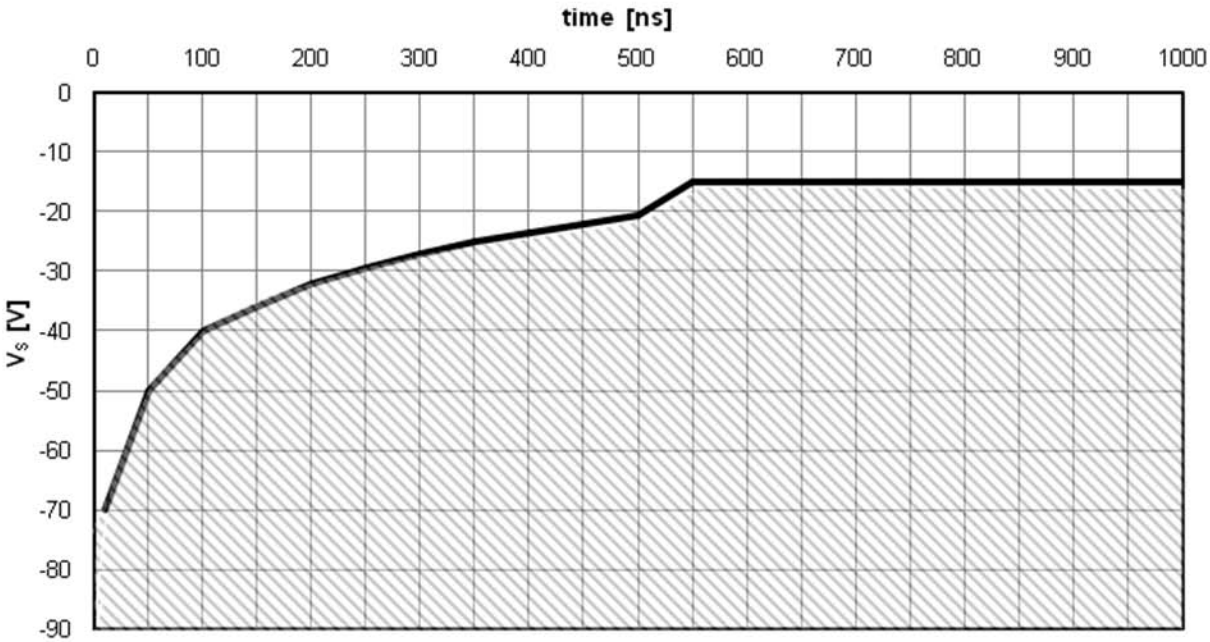

Figure 13: Negative VS transient SOA for AUIRS2117(8)S @ VBS=15V

Even though the AUIRS2117(8)S has shown the ability to handle these large negative V_S transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

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Parameter Temperature Trends

Figures 14-28 provide information on the experimental performance of the AUIRS2117(8)S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental curve.

The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

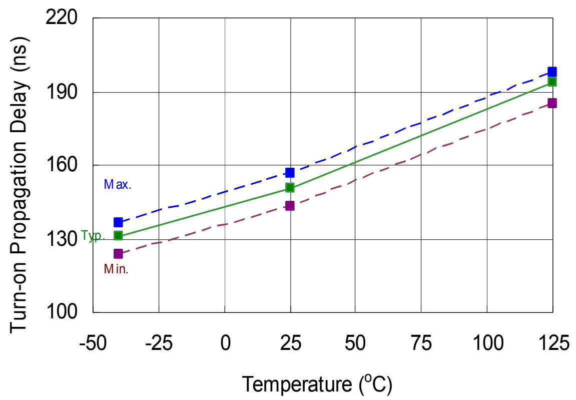

Figure 14. Turn-On Time vs. Temperature

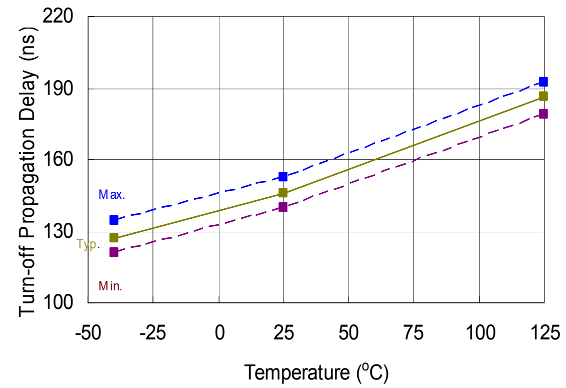

Figure 15. Turn-Off Time vs. Temperature

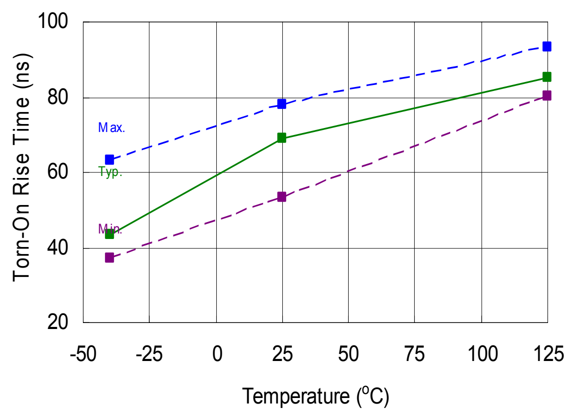

Figure 16. Turn-On Rise Time vs. Temperature

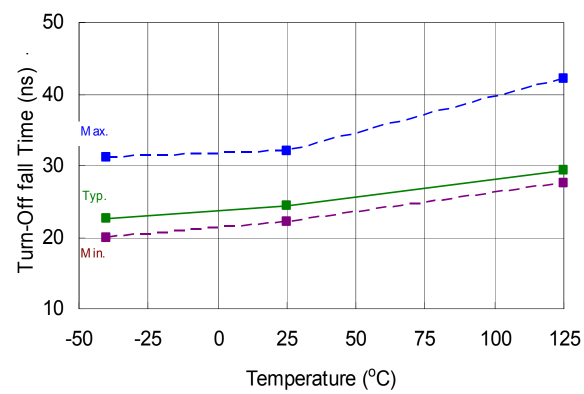

Figure 17. Turn-Off Fall Time vs. Temperature

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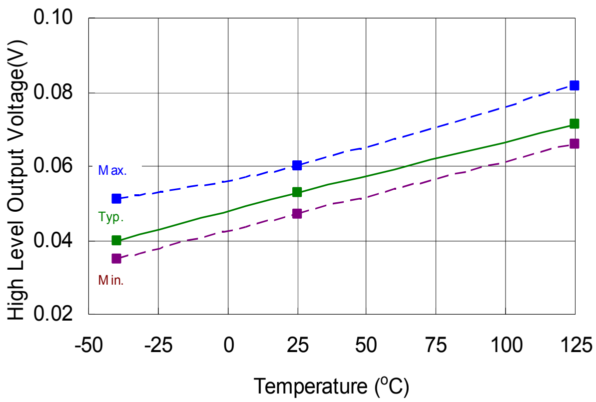

Figure 18. High Level Output Voltage vs. Temperature

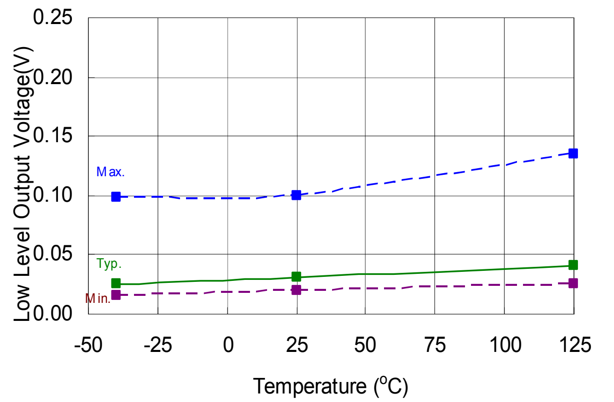

Figure 19. Low Level Output Voltage vs. Temperature

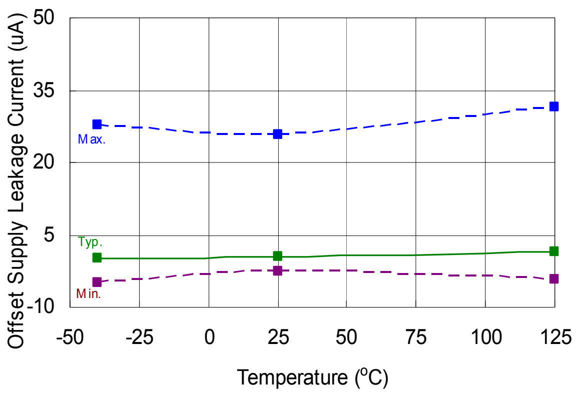

Figure 20. Offset Supply Leakage Current vs. Temperature

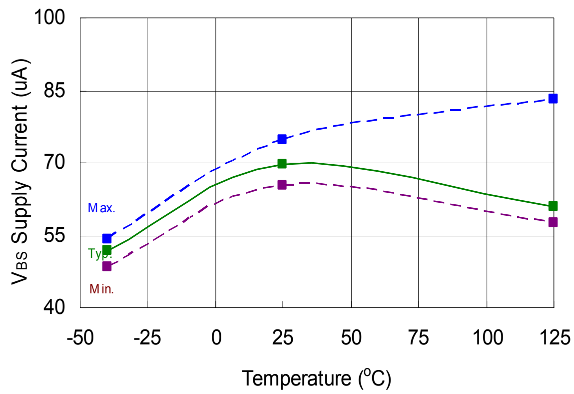

Figure 21. V_{BS} Supply Current vs. Temperature

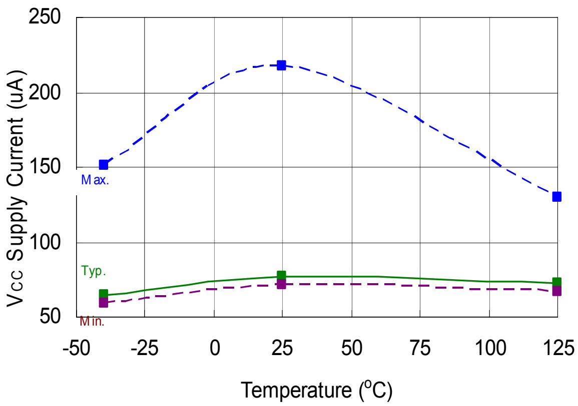

Figure 22. V_{CC} Supply Current vs. Temperature

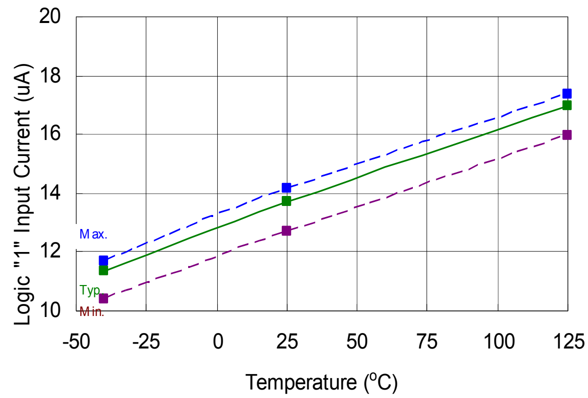

Figure 23. Logic “1” Input Current vs. Temperature

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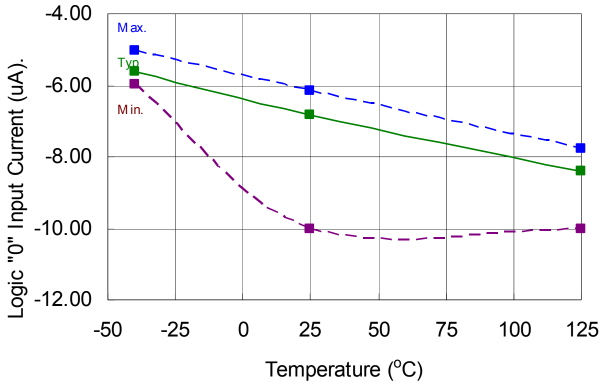

Figure 24. Logic “0” (2118 “1”) Input Current vs. Temperature

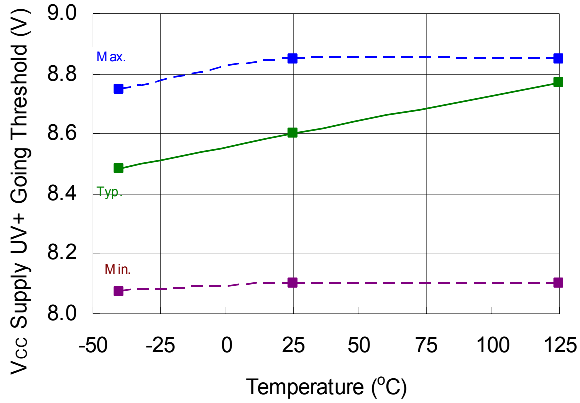

Figure 25. V_{CC} Undervoltage Threshold (+) vs. Temperature

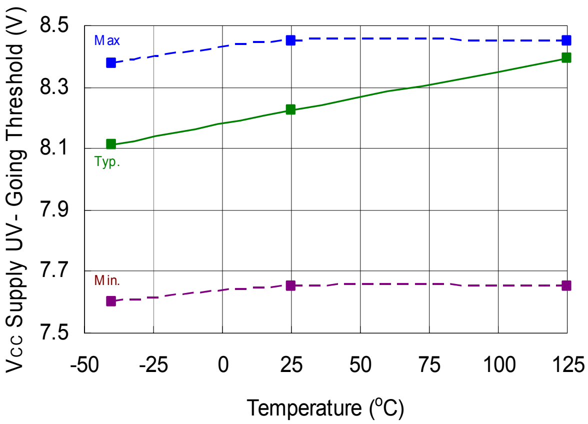

Figure 26. V_{CC} Undervoltage Threshold (-) vs. Temperature

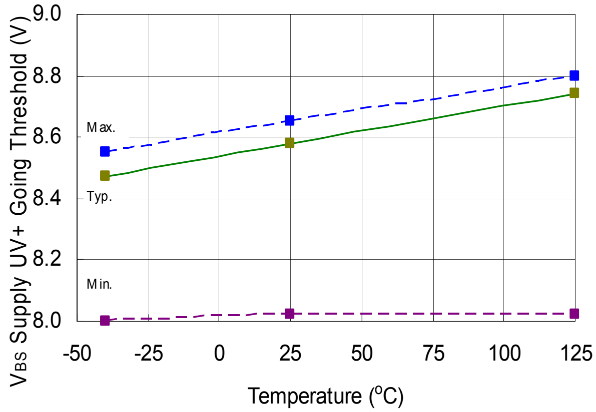

Figure 27. V_{BS} Undervoltage Threshold (+) vs. Temperature

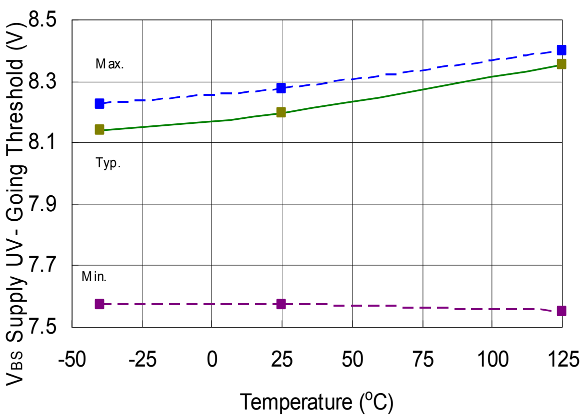

Figure 28. V_{BS} Undervoltage Threshold (-) vs. Temperature

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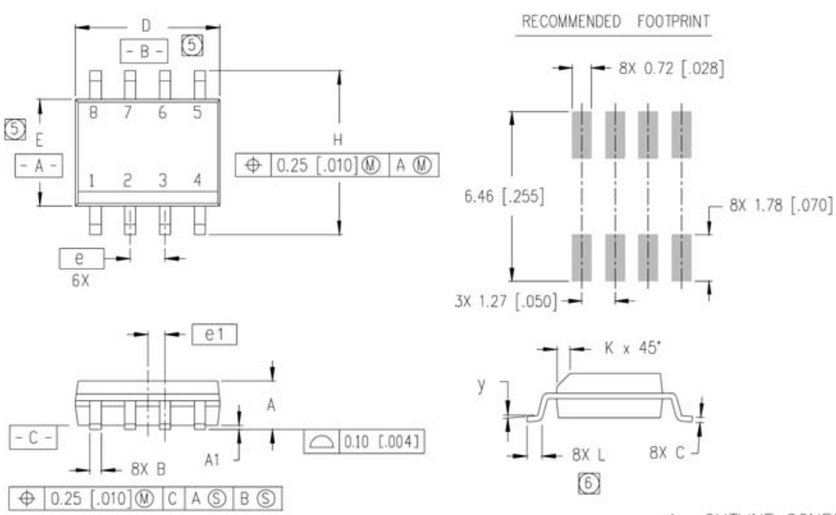
Package Details: SOIC8



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

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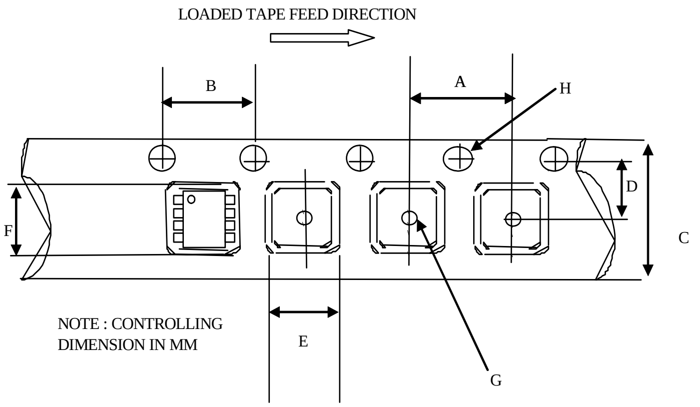
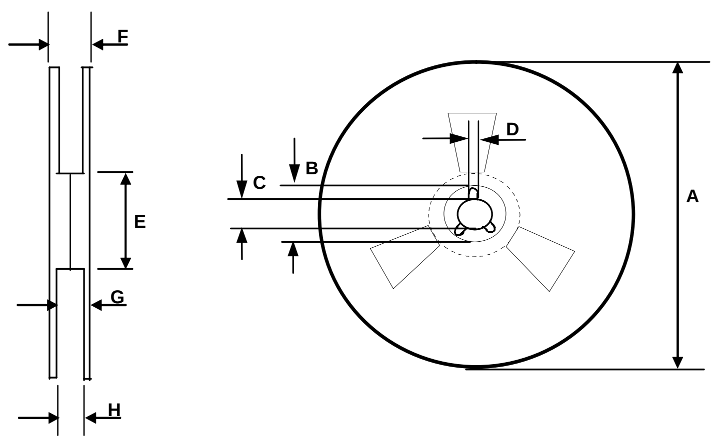
Tape and Reel Details: SOIC8



CARRIER TAPE DIMENSION FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

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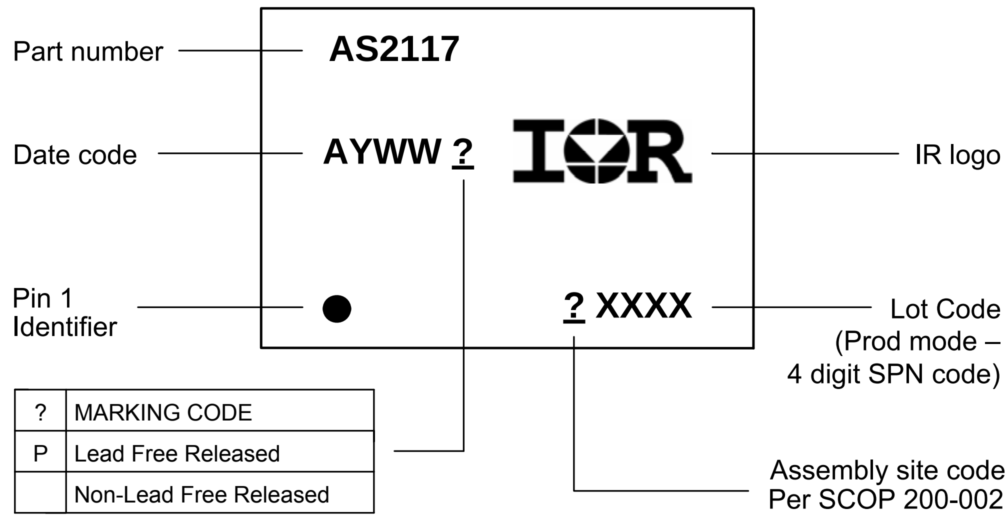
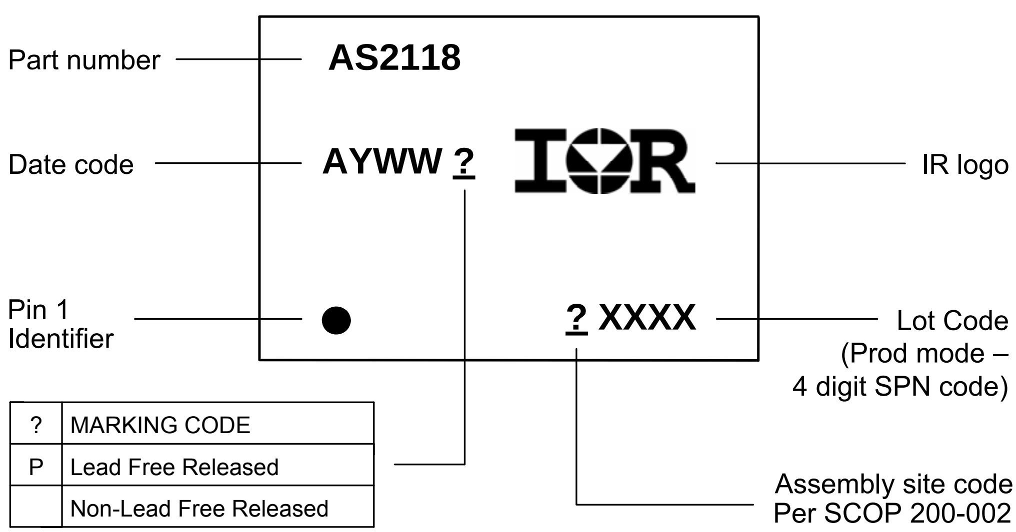
Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

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Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS2117S	SOIC8	Tube/Bulk	95	AUIRS2117S
		Tape and Reel	2500	AUIRS2117STR
AUIRS2118S	SOIC8	Tube/Bulk	95	AIRS2118S
		Tape and Reel	2500	AUIRS2118STR

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