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# KAI-16000

## 4872 (H) x 3248 (V) Interline CCD Image Sensor

### Description

The KAI-16000 is an interline transfer CCD offering 16 million pixels at up to 3 frames per second through 2 outputs. This image sensor is organized into an array of 4,872 (H) x 3,248 (V) with 7.4 micron square pixels and full 35 mm optical format. As an interline transfer CCD, the KAI-16000 includes additional features such as progressive scan readout, electronic shutter, low noise, high dynamic range, and blooming suppression. These features make the KAI-16000 the perfect sensor for applications in Industrial, Aerial, Security, and Scientific markets.

**Table 1. GENERAL SPECIFICATIONS**

| Parameter                                                                         | Typical Value                                                            |
|-----------------------------------------------------------------------------------|--------------------------------------------------------------------------|
| Architecture                                                                      | Interline CCD; Progressive Scan                                          |
| Total Number of Pixels                                                            | 4960 (H) x 3324 (V) = 16.6M                                              |
| Number of Effective Pixels                                                        | 4904 (H) x 3280 (V) = 16.1M                                              |
| Number of Active Pixels                                                           | 4872 (H) x 3248 (V) = 15.8M                                              |
| Pixel Size                                                                        | 7.4 $\mu\text{m}$ (H) x 7.4 $\mu\text{m}$ (V)                            |
| Active Image Size                                                                 | 36.1 mm (H) x 24.0 mm (V)<br>43.3 mm (diagonal),<br>35 mm Optical Format |
| Aspect Ratio                                                                      | 3:2                                                                      |
| Number of Outputs                                                                 | 1 or 2                                                                   |
| Saturation Signal                                                                 | 30,000 electrons                                                         |
| Output Sensitivity                                                                | 30 $\mu\text{V}/\text{e}^-$                                              |
| Quantum Efficiency<br>KAI-16000-AXA<br>KAI-16000-CXA (RGB)<br>KAI-16000-FXA (RGB) | 47%<br>29%, 38%, 44%<br>31%, 39%, 45%                                    |
| Read Noise ( $f = 30$ MHz)                                                        | 16 electrons                                                             |
| Dark Current                                                                      | < 0.5 nA/cm <sup>2</sup>                                                 |
| Dark Current Doubling Temperature                                                 | 7°C                                                                      |
| Dynamic Range                                                                     | 65 dB                                                                    |
| Charge Transfer Efficiency                                                        | 0.99999                                                                  |
| Blooming Suppression                                                              | > 100 X                                                                  |
| Smear                                                                             | < -80 dB                                                                 |
| Image Lag                                                                         | < 10 electrons                                                           |
| Maximum Data Rate                                                                 | 30 MHz per channel                                                       |
| Package                                                                           | 40 pin Grid Array                                                        |
| Cover Glass                                                                       | AR coated, 2 sides<br>or Clear Glass                                     |

NOTE: All parameters are specified at T = 40°C unless otherwise noted.



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**Figure 1. KAI-16000 CCD Image Sensor**

### Features

- 16 Million Pixel Resolution
- Electronic Shutter
- 35 mm Optical Format
- Progressive Scan Readout
- High Sensitivity
- Fast Frame Rate
- > 60 dB Dynamic Range

### Applications

- Industrial
- Aerial Photography
- Security
- Scientific

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# KAI-16000

## ORDERING INFORMATION

**Table 2. ORDERING INFORMATION**

| Part Number          | Description                                                                                                               | Marking Code                   |
|----------------------|---------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| KAI-16000-AAA-JR-B1* | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass with AR coating (2 sides), Grade 1                         | KAI-16000-AAA<br>Serial Number |
| KAI-16000-AAA-JR-B2* | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass with AR coating (2 sides), Grade 2                         |                                |
| KAI-16000-AAA-JR-AE* | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass with AR coating (2 sides), Engineering Grade               |                                |
| KAI-16000-AAA-JP-B1  | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, Grade 1                                                   |                                |
| KAI-16000-AAA-JP-B2  | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, Grade 2                                                   |                                |
| KAI-16000-AAA-JP-AE  | Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, Engineering Grade                                         |                                |
| KAI-16000-AAA-JD-B1  | Monochrome, No Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (2 sides), Grade 1                        |                                |
| KAI-16000-AAA-JD-B2  | Monochrome, No Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (2 sides), Grade 2                        |                                |
| KAI-16000-AAA-JD-AE  | Monochrome, No Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (2 sides), Engineering Grade              |                                |
| KAI-16000-AXA-JD-BX  | Monochrome, Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Special Grade                 | KAI-16000-AXA<br>Serial Number |
| KAI-16000-AXA-JD-B1  | Monochrome, Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Grade 1                       |                                |
| KAI-16000-AXA-JD-B2  | Monochrome, Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Grade 2                       |                                |
| KAI-16000-AXA-JD-AE  | Monochrome, Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Engineering Grade             |                                |
| KAI-16000-AXA-JR-B1* | Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass with AR coating (2 sides), Grade 1                    |                                |
| KAI-16000-AXA-JR-B2* | Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass with AR coating (2 sides), Grade 2                    |                                |
| KAI-16000-AXA-JR-AE* | Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass with AR coating (2 sides), Engineering Grade          |                                |
| KAI-16000-AXA-JP-B1  | Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass, Grade 1                                              |                                |
| KAI-16000-AXA-JP-B2  | Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass, Grade 2                                              |                                |
| KAI-16000-AXA-JP-AE  | Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass, Engineering Grade                                    |                                |
| KAI-16000-FXA-JD-B1  | Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Grade 1           | KAI-16000-FXA<br>Serial Number |
| KAI-16000-FXA-JD-B2  | Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Grade 2           |                                |
| KAI-16000-FXA-JD-AE  | Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Engineering Grade |                                |

\*Not recommended for new designs.

## KAI-16000

**Table 2. ORDERING INFORMATION**

| Part Number          | Description                                                                                                               | Marking Code                   |
|----------------------|---------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| KAI-16000-CXA-JD-B1* | Gen1 Color (Bayer RGB), Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Grade 1           | KAI-16000-CXA<br>Serial Number |
| KAI-16000-CXA-JD-B2* | Gen1 Color (Bayer RGB), Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Grade 2           |                                |
| KAI-16000-CXA-JD-AE* | Gen1 Color (Bayer RGB), Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Engineering Grade |                                |

\*Not recommended for new designs.

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at [www.onsemi.com](http://www.onsemi.com).

## DEVICE DESCRIPTION

### Architecture

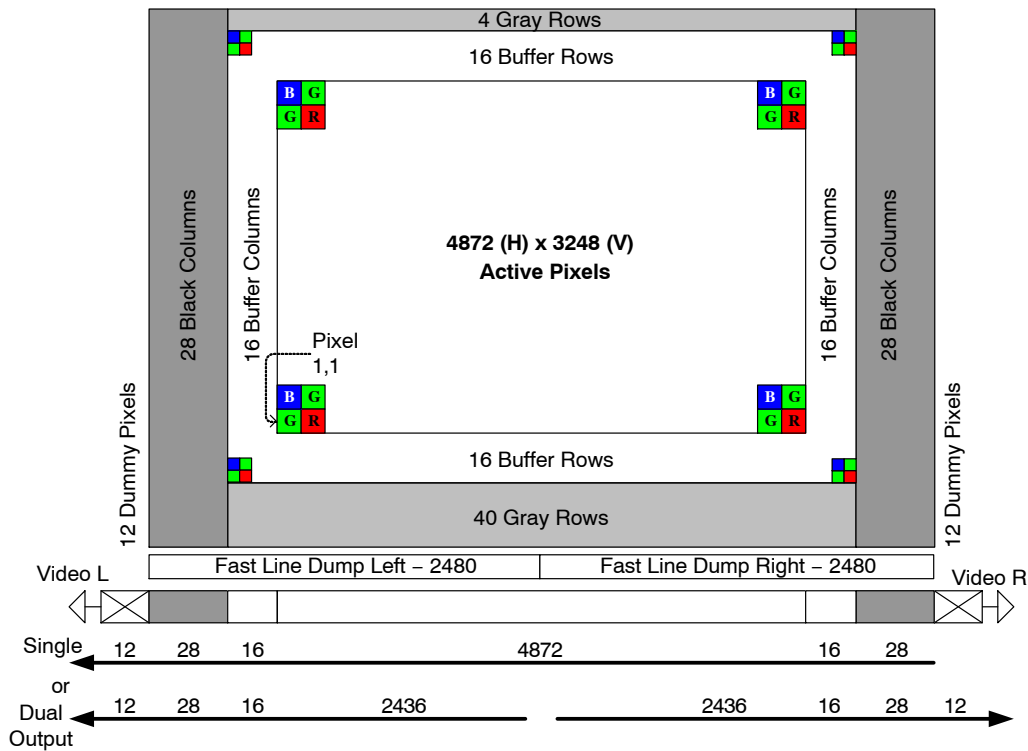


Figure 2. Sensor Architecture

There are 40 light shielded gray rows followed 3280 photoactive rows and finally 4 more light shielded gray rows. The first 16 and the last 16 photoactive rows are buffer rows giving a total of 3248 lines of image data.

In the single output mode all pixels are clocked out of the Video L output in the lower left corner of the sensor. The first 12 empty pixels of each line do not receive charge from the vertical shift register. The next 28 pixels receive charge from the left light shielded edge followed by 4904 photosensitive pixels and finally 28 more light shielded pixels from the right edge of the sensor. The first 16 and last 16 photosensitive pixels are buffer pixels giving a total of 4872 pixels of image data.

In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is

clocked out Video L and the right half of the image is clocked out Video R. For the Video L each row consists of 12 empty pixels followed by 28 light shielded pixels followed by 2452 photosensitive pixels. For the Video R each row consists of 12 empty pixels followed by 28 light shielded pixels followed by 2452 photosensitive pixels. When reconstructing the image, data from Video R will have to be reversed in a line buffer and appended to the Video L data.

The gray rows are not entirely dark and so should not be used for a dark reference level. Use the dark columns on the left or right side of the image sensor as a dark reference.

Of the dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns.

## PHYSICAL DESCRIPTION

### Pin Description and Device Orientation

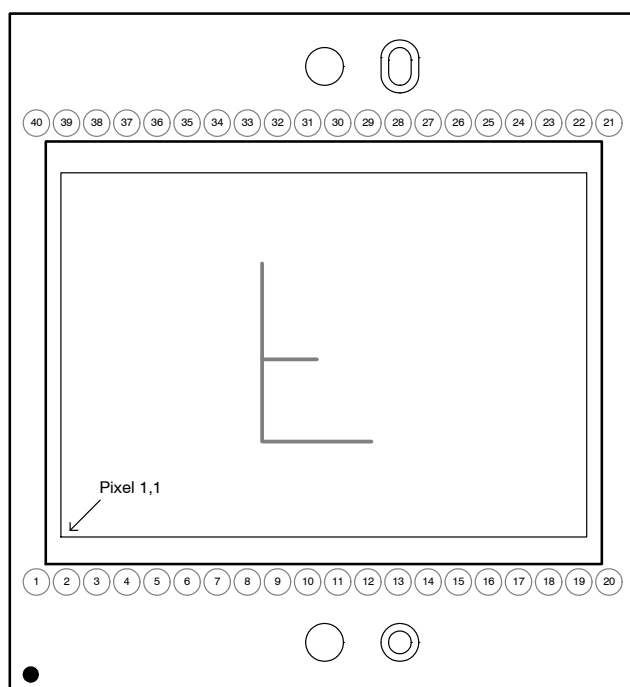


Figure 3. Package Pin Designations – Top View

Table 3. PINOUT

| Pin | Name               | Description                               |
|-----|--------------------|-------------------------------------------|
| 1   | VOU <sub>TL</sub>  | Video Output, Left                        |
| 2   | V <sub>DDL</sub>   | V <sub>DD</sub> , Left                    |
| 3   | GND                | Ground                                    |
| 4   | RESE <sub>TL</sub> | Reset Gate, Left                          |
| 5   | H <sub>LASTL</sub> | Horizontal Clock, Last Stage, Left        |
| 6   | H <sub>2BL</sub>   | Horizontal Clock, Phase 2, Barrier, Left  |
| 7   | H <sub>1BL</sub>   | Horizontal Clock, Phase 1, Barrier, Left  |
| 8   | H <sub>1SL</sub>   | Horizontal Clock, Phase 1, Storage, Left  |
| 9   | H <sub>2SL</sub>   | Horizontal Clock, Phase 2, Storage, Left  |
| 10  | ESD                | ESD Protection Disable                    |
| 11  | GND                | Ground                                    |
| 12  | H <sub>2SR</sub>   | Horizontal Clock, Phase 2, Storage, Right |
| 13  | H <sub>1SR</sub>   | Horizontal Clock, Phase 1, Storage, Right |
| 14  | H <sub>1BR</sub>   | Horizontal Clock, Phase 1, Barrier, Right |
| 15  | H <sub>2BR</sub>   | Horizontal Clock, Phase 2, Barrier, Right |
| 16  | H <sub>LASTR</sub> | Horizontal Clock, Last Stage, Right       |
| 17  | RESE <sub>TR</sub> | Reset Gate, Right                         |
| 18  | GND                | Ground                                    |
| 19  | V <sub>DDR</sub>   | V <sub>DD</sub> , Right                   |
| 20  | VOU <sub>TR</sub>  | Video Output, Right                       |

| Pin | Name             | Description                |
|-----|------------------|----------------------------|
| 40  | FDG <sub>L</sub> | Fast Line Dump Gate, Left  |
| 39  | RDL              | Reset Drain, Left          |
| 38  | SUB              | Substrate                  |
| 37  | GND              | Ground                     |
| 36  | V <sub>1</sub>   | VCCD Gate 1, Phase 2       |
| 35  | V <sub>5</sub>   | VCCD Gate 5, Phase 2       |
| 34  | V <sub>9</sub>   | VCCD Gate 9, Phase 2       |
| 33  | V <sub>3</sub>   | VCCD Gate 3, Phase 2       |
| 32  | V <sub>7</sub>   | VCCD Gate 7, Phase 2       |
| 31  | V <sub>11</sub>  | VCCD Gate 11, Phase 2      |
| 30  | V <sub>2</sub>   | VCCD Gate 2, Phase 1       |
| 29  | V <sub>6</sub>   | VCCD Gate 6, Phase 1       |
| 28  | V <sub>10</sub>  | VCCD Gate 10, Phase 1      |
| 27  | V <sub>4</sub>   | VCCD Gate 4, Phase 1       |
| 26  | V <sub>8</sub>   | VCCD Gate 8, Phase 1       |
| 25  | V <sub>12</sub>  | VCCD Gate 12, Phase 1      |
| 24  | GND              | Ground                     |
| 23  | SUB              | Substrate                  |
| 22  | RDR              | Reset Drain, Right         |
| 21  | FDG <sub>R</sub> | Fast Line Dump Gate, Right |

## IMAGING PERFORMANCE

**Table 4. TYPICAL OPERATION CONDITIONS**

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

| Description                | Condition                                                                   | Notes |
|----------------------------|-----------------------------------------------------------------------------|-------|
| Frame Time                 | 908 msec                                                                    | 1     |
| Horizontal Clock Frequency | 20 MHz                                                                      |       |
| Light Source               | Continuous red, green and blue illumination centered at 450, 530 and 650 nm | 2, 3  |
| Operation                  | Nominal operating voltages and timing                                       |       |

1. Electronic shutter is not used. Integration time equals frame time.
2. LEDs used: Blue: Nichia NLPB500, Green: Nichia NSPG500S and Red: HP HLMP-8115.
3. For monochrome sensor, only green LED used.

**Table 5. SPECIFICATIONS**

| Description                                          | Symbol            | Min.       | Nom.        | Max.        | Units                       | Sample Plan <sup>7</sup> | Temperature Tested At (°C) | Notes |
|------------------------------------------------------|-------------------|------------|-------------|-------------|-----------------------------|--------------------------|----------------------------|-------|
| Global Non-Uniformity                                |                   | n/a        | 2.5         | 5.0         | %rms                        | Die                      | 27, 40                     | 1     |
| Maximum Photoresponse Nonlinearity                   | NL                | n/a        | 2           |             | %                           | Design                   |                            | 2, 3  |
| Maximum Gain Difference Between Outputs              | ΔG                | n/a        | 10          |             | %                           | Design                   |                            | 2, 3  |
| Maximum Signal Error due to Nonlinearity Differences | ΔNL               | n/a        | 1           |             | %                           | Design                   |                            | 2, 3  |
| Horizontal CCD Charge Capacity                       | HNe               |            | 100         |             | ke <sup>-</sup>             | Design                   |                            |       |
| Vertical CCD Charge Capacity                         | VNe               |            | 50          |             | ke <sup>-</sup>             | Die                      | 27, 40                     |       |
| Photodiode Charge Capacity                           | PNe               | 28         | 30          |             | ke <sup>-</sup>             | Die                      | 27, 40                     | 4     |
| Horizontal CCD Charge Transfer Efficiency            | HCTE              | 0.99999    |             | n/a         |                             | Design                   |                            |       |
| Vertical CCD Charge Transfer Efficiency              | VCTE              | 0.99999    |             |             |                             | Design                   |                            |       |
| Photodiode Dark Current                              | l <sub>pd</sub>   | n/a<br>n/a | 40<br>0.01  | 350<br>0.1  | e/p/s<br>nA/cm <sup>2</sup> | Die                      | 40                         |       |
| Vertical CCD Dark Current                            | l <sub>vd</sub>   | n/a<br>n/a | 400<br>0.12 | 1711<br>0.5 | e/p/s<br>nA/cm <sup>2</sup> | Die                      | 40                         |       |
| Dark Current Doubling Temperature                    | ΔT                | n/a        | 7           | n/a         | °C                          | Design                   |                            |       |
| Image Lag                                            | Lag               | n/a        | <10         | 50          | e <sup>-</sup>              | Design                   |                            |       |
| Antiblooming Factor                                  | X <sub>ab</sub>   | 100        | 300         | n/a         |                             | Design                   |                            |       |
| Vertical Smear                                       | S <sub>mr</sub>   | n/a        | -80         | -75         | dB                          | Design                   |                            |       |
| Read Noise                                           | n <sub>e-T</sub>  |            | 16          |             | e <sup>-</sup> rms          | Design                   |                            | 5     |
| Dynamic Range                                        | DR                |            | 65          |             | dB                          | Design                   |                            | 5, 6  |
| Output Amplifier DC Offset                           | V <sub>odc</sub>  | 4          | 9.5         | 14          | V                           | Die                      | 27, 40                     |       |
| Output Amplifier Bandwidth                           | F <sub>-3db</sub> |            | 140         |             | MHz                         | Design                   |                            |       |
| Output Amplifier Impedance                           | R <sub>OUT</sub>  | 100        | 130         | 200         | Ω                           | Die                      | 27, 40                     |       |
| Output Amplifier Sensitivity                         | ΔV/ΔN             |            | 30          |             | μV/e <sup>-</sup>           | Design                   |                            |       |

1. Per color
2. Value is over the range of 10% to 90% of photodiode saturation.
3. Value is for the sensor operated without binning.
4. The operating value of the substrate voltage, V<sub>AB</sub>, will be marked on the shipping container for each device. The value of V<sub>ab</sub> is set such that the photodiode charge capacity is 30,000 electrons.
5. At 30 MHz
6. Uses 20LOG (PNe/ n<sub>e-T</sub>)
7. "Die" indicates a parameter that is measured on every sensor during the production testing. "Design" designates a parameter that is quantified during the design verification activity.

# KAI-16000

**Table 6. KAI-16000-AAA**

| Description                        | Symbol            | Min. | Nom. | Max. | Units | Sample Plan <sup>1</sup> | Temperature Tested At (°C) | Notes |
|------------------------------------|-------------------|------|------|------|-------|--------------------------|----------------------------|-------|
| Peak Quantum Efficiency            | QE <sub>max</sub> |      | 11   | n/a  | %     | Design                   |                            |       |
| Peak Quantum Efficiency Wavelength | λ <sub>QE</sub>   | n/a  | 500  | n/a  | nm    | Design                   |                            |       |

1. "Die" indicates a parameter that is measured on every sensor during the production testing. "Design" designates a parameter that is quantified during the design verification activity.

**Table 7. KAI-16000-AXA**

| Description                        | Symbol            | Min. | Nom. | Max. | Units | Sample Plan <sup>1</sup> | Temperature Tested At (°C) | Notes |
|------------------------------------|-------------------|------|------|------|-------|--------------------------|----------------------------|-------|
| Peak Quantum Efficiency            | QE <sub>max</sub> |      | 45   | n/a  | %     | Design                   |                            |       |
| Peak Quantum Efficiency Wavelength | λ <sub>QE</sub>   | n/a  | 500  | n/a  | nm    | Design                   |                            |       |

1. "Die" indicates a parameter that is measured on every sensor during the production testing. "Design" designates a parameter that is quantified during the design verification activity.

**Table 8. KAI-16000-FXA (Gen2)**

| Description                        | Symbol               | Min.              | Nom.              | Max.              | Units             | Sample Plan <sup>1</sup> | Temperature Tested At (°C) | Notes |
|------------------------------------|----------------------|-------------------|-------------------|-------------------|-------------------|--------------------------|----------------------------|-------|
| Peak Quantum Efficiency            | Blue<br>Green<br>Red | QE <sub>max</sub> | 45<br>39<br>31    | n/a<br>n/a<br>n/a | %                 | Design                   |                            |       |
| Peak Quantum Efficiency Wavelength | Blue<br>Green<br>Red | λ <sub>QE</sub>   | n/a<br>n/a<br>n/a | 460<br>525<br>600 | n/a<br>n/a<br>n/a | nm                       | Design                     |       |

1. "Design" designates a parameter that is quantified during the design verification activity.

**Table 9. KAI-16000-CXA (Gen1)**

| Description                        | Symbol               | Min.              | Nom.              | Max.              | Units             | Sample Plan <sup>1</sup> | Temperature Tested At (°C) | Notes |
|------------------------------------|----------------------|-------------------|-------------------|-------------------|-------------------|--------------------------|----------------------------|-------|
| Peak Quantum Efficiency            | Blue<br>Green<br>Red | QE <sub>max</sub> | 44<br>38<br>29    | n/a<br>n/a<br>n/a | %                 | Design                   |                            | 2     |
| Peak Quantum Efficiency Wavelength | Blue<br>Green<br>Red | λ <sub>QE</sub>   | n/a<br>n/a<br>n/a | 470<br>540<br>620 | n/a<br>n/a<br>n/a | nm                       | Design                     | 2     |

1. "Design" designates a parameter that is quantified during the design verification activity.

2. This color filter set configuration (Gen1) is not recommended for new designs.

NOTE: n/a = not applicable

## TYPICAL PERFORMANCE CURVES

### Monochrome with Microlens Quantum Efficiency

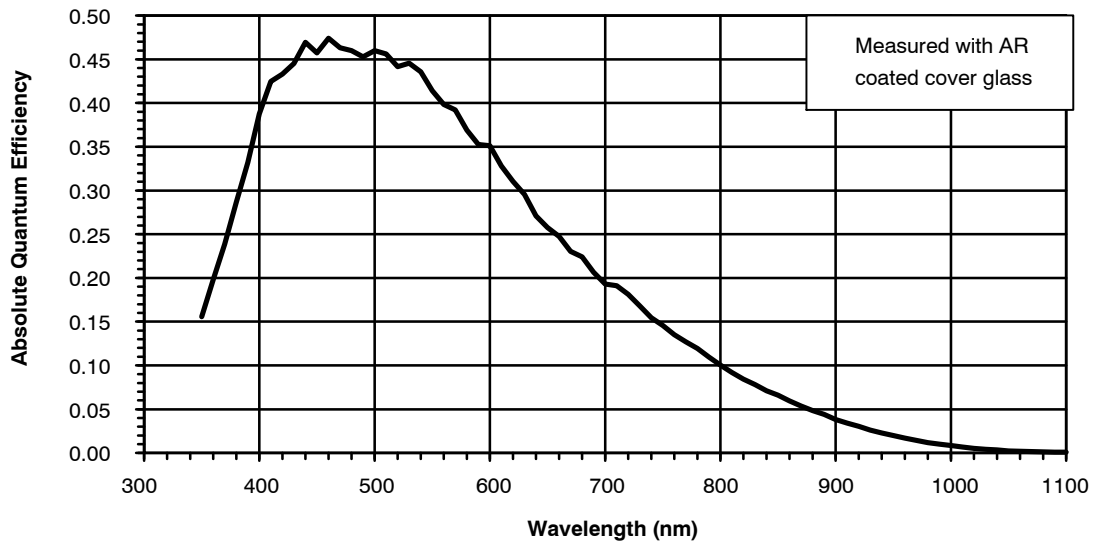


Figure 4. Monochrome with Microlens Quantum Efficiency

### Monochrome without Microlens Quantum Efficiency

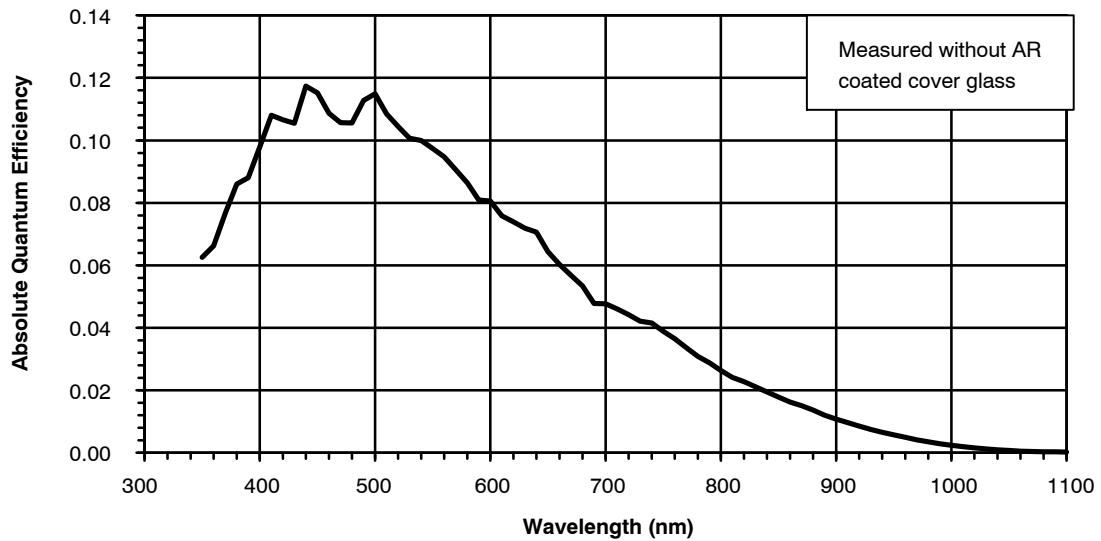


Figure 5. Monochrome without Microlens Quantum Efficiency

Color with Microlens Quantum Efficiency

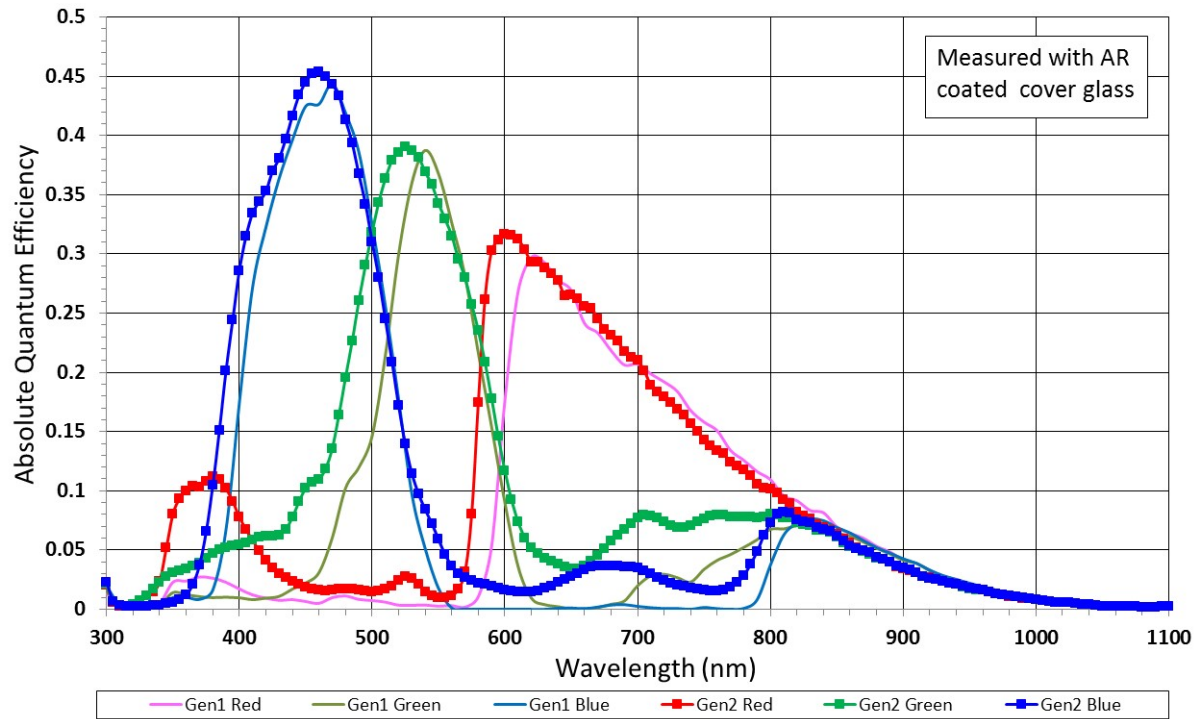


Figure 6. Color with Microlens Quantum Efficiency

### Angular Quantum Efficiency

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.

For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

### Monochrome with Microlens

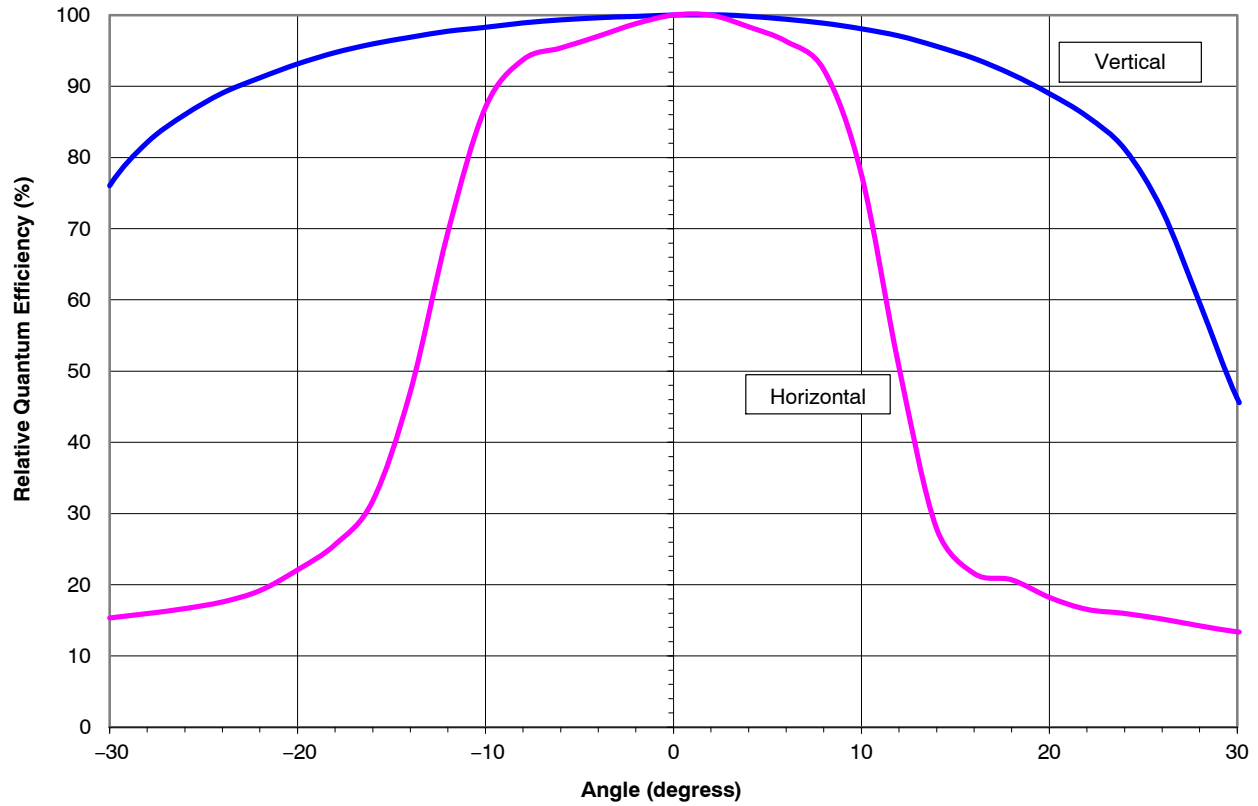


Figure 7. Monochrome with Microlens Angular Quantum Efficiency

## DEFECT DEFINITIONS

### Operational Conditions

All defect tests performed at  $t_{\text{int}} = t_{\text{frame}} = 908 \text{ msec}$

**Table 10. SPECIFICATIONS**

| Description                                | Definition                                                                                                                | Class X Monochrome<br>with Microlens Only | Class 1               | Class 2<br>Monochrome | Class 2<br>Color      | Notes |
|--------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|-----------------------|-----------------------|-----------------------|-------|
| Major dark field defective<br>bright pixel | Defect $\geq 245 \text{ mV}$                                                                                              | 150                                       | 150                   | 300                   | 300                   | 2     |
| Major bright field defective<br>dark pixel | Defect $\geq 15\%$                                                                                                        |                                           |                       |                       |                       |       |
| Minor dark field defective<br>bright pixel | Defect $\geq 126 \text{ mV}$                                                                                              | 1500                                      | 1500                  | 3000                  | 3000                  | 3     |
| Cluster defect                             | A group of 2 to "N"<br>contiguous major<br>defective pixels, but no<br>more than "W"<br>adjacent defects<br>horizontally. | 0                                         | 30<br>N = 20<br>W = 4 | 30<br>N = 20<br>W = 4 | 30<br>N = 20<br>W = 4 | 1, 2  |
| Column defect                              | A group of more than<br>10 contiguous major<br>defective pixels along<br>a single column                                  | 0                                         | 0                     | 4                     | 15                    | 1, 2  |

1. Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).

2. Tested at 27°C and 40°C.

3. Tested at 40°C.

NOTE: Class X sensors are offered strictly "as available". ON Semiconductor cannot guarantee delivery dates. Please call for availability.

### Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point

defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps.

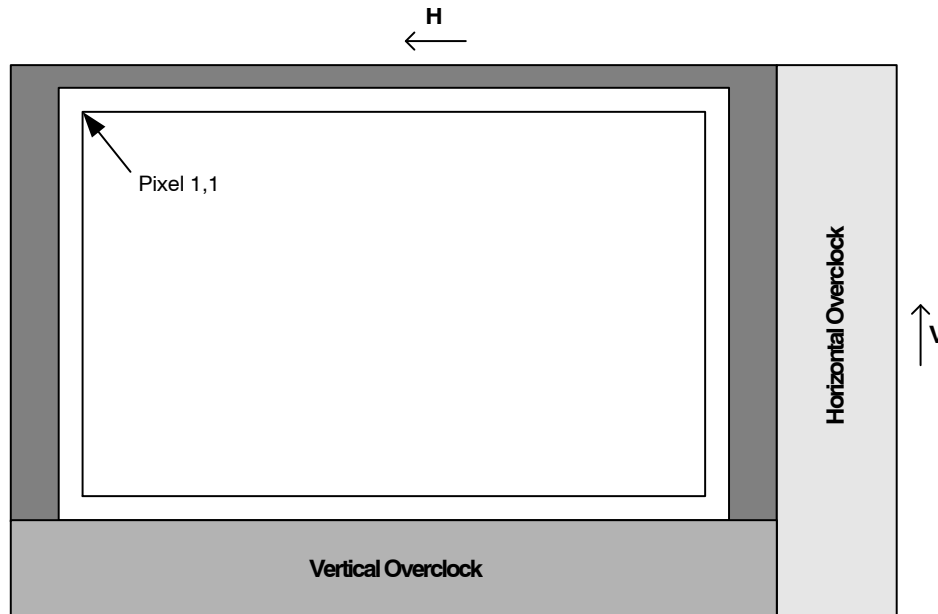
**TEST DEFINITIONS****Test Regions of Interest**

Image Area ROI: Pixel (1, 1) to Pixel (4872, 3248)

Only the active pixels are used for performance and defect tests.

**Overclocking**

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 8 for a pictorial representation of the regions.



**Figure 8. Overclock Regions of Interest**

## Tests

### *Global Non-Uniformity*

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 630 mV). Prior to this test being performed

the substrate voltage has been set such that the charge capacity of the sensor is 900 mV. Global non-uniformity is defined as

$$\text{GlobalNon-Uniformity} = 100 \times \left( \frac{\text{ActiveAreaStandardDeviation}}{\text{ActiveAreaSignal}} \right)$$

Units: %rms.

Active Area Signal = Active Area Average – Dark Column Average

### *Dark Field Defect Test*

This test is performed under dark field conditions. The sensor is partitioned into 384 sub regions of interest, each of which is 203 by 203 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the “Defect Definitions” section.

### *Bright Field Defect Test*

This test is performed with the imager illuminated to a level such that the output is at approximately 630 mV. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 900 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal \* threshold  
Bright defect threshold = Active Area Signal \* threshold

The sensor is then partitioned into 384 sub regions of interest, each of which is 203 by 203 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 630 mV
- Dark defect threshold: 630 mV \* 15% = 95 mV
- Bright defect threshold: 630 mV \* 15% = 95 mV
- Region of interest #1 selected. This region of interest is pixels 1, 1 to pixels 203, 203.
  - ♦ Median of this region of interest is found to be 630 mV.
  - ♦ Any pixel in this region of interest that is  $\geq (630 + 95 \text{ mV})$  725 mV in intensity will be marked defective.
  - ♦ Any pixel in this region of interest that is  $\leq (630 - 95 \text{ mV})$  535 mV in intensity will be marked defective.
- All remaining 384 sub regions of interest are analyzed for defective pixels in the same manner.

## OPERATION

**Table 11. ABSOLUTE MAXIMUM RATINGS**

| Description           | Symbol           | Minimum | Maximum | Units | Notes |
|-----------------------|------------------|---------|---------|-------|-------|
| Operating Temperature | T <sub>OP</sub>  | -50     | 70      | °C    | 1     |
| Humidity              | RH               | 5       | 90      | %     | 2     |
| Output Bias Current   | I <sub>out</sub> | 0.0     | -40     | mA    | 3     |
| Off-chip Load         | C <sub>L</sub>   |         | 10      | pF    |       |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Noise performance will degrade at higher temperatures.
- T = 25°C. Excessive humidity will degrade MTTF.
- Total for all outputs. Maximum current is -20 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.

**Table 12. MAXIMUM VOLTAGE RATINGS BETWEEN PINS**

| Description                                                                   | Minimum | Maximum | Units | Notes |
|-------------------------------------------------------------------------------|---------|---------|-------|-------|
| RL, RR, H1SL, H1BL, H2SL, H2BL, H1SR, H1BR, H2SR, H2BR, HLASTL, HLASTR to ESD | 0       | 17      | V     |       |
| Pin to Pin with ESD Protection                                                | -17     | 17      | V     | 1     |
| VDDL, VDDR to GND                                                             | 0       | 25      | V     |       |

- Pins with ESD protection are: RL, RR, H1SL, H1BL, H2SL, H2BL, H1SR, H1BR, H2SR, H2BR, HLASTL, and HLASTR

### Power-Up Sequence

- Substrate
- ESD Protection Disable
- All other clocks and biases

**Table 13. DC BIAS OPERATING CONDITIONS**

| Description             | Symbol           | Pins                                     | Minimum | Nominal | Maximum | Units | Maximum DC Current (mA) | Notes |
|-------------------------|------------------|------------------------------------------|---------|---------|---------|-------|-------------------------|-------|
| Reset Drain             | RD               | RDL, RDR                                 | +11.5   | +12.0   | +12.0   | V     |                         |       |
| Output Amplifier Supply | VDD              | VDDL, VDDR                               | +14.5   | +15.0   | +15.5   | V     |                         | 4     |
| Ground                  | GND              | GND                                      | 0.0     | 0.0     | 0.0     | V     |                         |       |
| Substrate               | SUB              | SUB                                      | +8.0    | VAB     | +16.0   | V     |                         | 1, 5  |
| ESD Protection Disable  | ESD              | ESD                                      | -9.25   | -9.0    | -8.75   | V     |                         | 2     |
| Output Bias Current     | I <sub>out</sub> | VOU <sub>TL</sub> ,<br>VOU <sub>TR</sub> |         | -5.0    | -10.0   | mA    |                         | 3     |

- The operating of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of Vab is set such that the photodiode charge capacity is 30,000 electrons.
- VESD must be at least 1 V more negative than H1<sub>lo</sub> and H2<sub>lo</sub> during sensor operation AND during camera power turn on.
- An output load sink must be applied to Vout to activate output amplifier.
- The maximum DC current is for one output unloaded. This is the maximum current that the first two stages of one output amplifier will draw. This value is with Vout disconnected.
- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

## AC Operating Conditions

Table 14. CLOCK LEVELS

| Description                                      | Pins                                                         | Symbol         | Minimum | Nominal | Maximum | Units | Notes |
|--------------------------------------------------|--------------------------------------------------------------|----------------|---------|---------|---------|-------|-------|
| Vertical CCD Clock High                          | V1, V3, V5, V7, V9, V11                                      | V_2hi          | +8.5    | +9.0    | +9.5    | V     |       |
| Vertical CCD Clocks Midlevel                     | V1, V2, V3, V4, V5, V6, V7, V8, V9, V10, V11, V12            | V_1mid, V_2mid | -0.2    | 0.0     | +0.2    | V     |       |
| Vertical CCD Clocks Low                          | V1, V2, V3, V4, V5, V6, V7, V8, V9, V10, V11, V12            | V_1lo, V_2lo   | -9.5    | -9.0    | -8.5    | V     |       |
| Horizontal CCD Clocks Amplitude, Phase 1 Storage | H1S $\alpha$ H1SL, H1BL, H2SL, H2BL, H1SR, H1BR, H2SR, H2BRK | H_amp          | +4.5    | +5.0    | +5.5    | V     |       |
| Horizontal CCD Clocks Low                        | H1SL, H1BL, H2SL, H2BL, H1SR, H1BR, H2SR, H2BR               | H_lo           | -5.0    | -4.5    | -4.0    | V     |       |
| Horizontal Last CCD Amplitude                    | HLASTL, HLASTR                                               | HLAST_amp      | +4.5    | +5.0    | +5.5    | V     |       |
| Horizontal Last CCD Low                          | HLASTL, HLASTR                                               | HLAST_lo       | -5.0    | -4.5    | -4.0    | V     |       |
| Reset Clock Amplitude                            | RESETL, RESETR                                               | R_amp          | +4.5    | +5.0    | +5.5    | V     |       |
| Reset Clock Low                                  | RESETL, RESETR                                               | R_lo           | -3.5    | -3.0    | -2.5    | V     |       |
| Electronic Shutter Voltage                       | SUB                                                          | Vshutter       | +44     | +48     | +52     | V     | 1     |
| Fast Dump High                                   | FDL, FDR                                                     | FD_hi          | +4.5    | +5.0    | +5.5    | V     |       |
| Fast Dump Low                                    | FDL, FDR                                                     | FD_lo          | -9.5    | -9.0    | -8.5    | V     |       |

1. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

The figure below shows the DC bias (SUB) and AC clock (Vshutter) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.

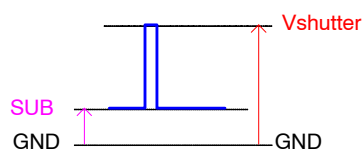


Figure 9.

**Table 15. CLOCK LINE CAPACITANCES**

| Clocks                                       | Capacitance | Units | Notes |
|----------------------------------------------|-------------|-------|-------|
| Vertical CCD Phase 1 to GND                  | 108         | nF    | 1, 3  |
| Vertical CCD Phase 2 to GND                  | 118         | nF    | 1, 4  |
| Vertical CCD Phase 1 to Vertical CCD Phase 2 | 56          | nF    | 3, 4  |
| H1S to GND                                   | 27          | pF    | 2     |
| H2S to GND                                   | 27          | pF    | 2     |
| H1B to GND                                   | 13          | pF    | 2     |
| H2B to GND                                   | 4           | pF    | 2     |
| H1S to H2B and H2S                           | 13          | pF    | 2     |
| H1B to H2B and H2S                           | 13          | pF    | 2     |
| H2S to H1B and H1S                           | 13          | pF    | 2     |
| H2B to H1B and H1S                           | 13          | pF    | 2     |
| H1LAST to GND                                | 20          | pF    | 2     |
| RESET to GND                                 | 10          | pF    |       |
| FD to GND                                    | 20          | pF    |       |

1. Gate capacitance to GND is voltage dependent. Value is for nominal VCCD clock voltages.
2. For nominal HCCD clock voltages, these values are for half of the imager (H1SL, H1BL, H2SL, H2BL and H1BINL or H1SR, H1BR, H2SR, H2BR and H1BINR).
3. Vertical CCD Phase 1: V2, V4, V6, V8, V10, V12
4. Vertical CCD Phase 2: V1, V3, V5, V7, V9, V11

## TIMING

Table 16. REQUIREMENTS AND CHARACTERISTICS

| Description                            | Symbol     | Minimum | Nominal | Maximum | Units   | Notes |
|----------------------------------------|------------|---------|---------|---------|---------|-------|
| VCCD to HCCD Delay                     | $T_{HD}$   | 4       | 6       |         | $\mu s$ |       |
| VCCD Transfer Time                     | $T_{VCCD}$ | 4       | 6       |         | $\mu s$ |       |
| HCCD to VCCD Delay                     | $T_{HL}$   |         | 50      |         | ns      |       |
| Photodiode Transfer Time               | $T_{V3rd}$ | 10      | 12      |         | $\mu s$ |       |
| VCCD Pedestal Time                     | $T_{3P}$   | 200     | 600     |         | $\mu s$ |       |
| VCCD Delay                             | $T_{3D}$   | 12      | 20      |         | $\mu s$ |       |
| VCCD Delay Before Pedestal             | $T_{DEL}$  |         | 50      |         | ns      |       |
| VCCD Delay Before 1 <sup>st</sup> Line | $T_{D1L}$  | 10      | 60      |         | $\mu s$ |       |
| Reset Pulse Time                       | $T_R$      |         | 3.25    |         | $\mu s$ |       |
| VCCD to HCCD Delay – Shutter           | $T_{HDS}$  |         | 6       |         | $\mu s$ |       |
| Shutter Pulse Time                     | $T_S$      |         | 4       |         | $\mu s$ |       |
| Shutter Pulse Delay                    | $T_{SD}$   |         | 1.5     |         | $\mu s$ |       |
| HCCD Clock Period                      | $T_H$      | 33.3    |         |         | ns      |       |
| VCCD Rise/Fall Time                    | $T_{VR}$   | 0.2     |         |         | $\mu s$ |       |
| Fast Dump Gate Leading Delay           | $T_{FDL}$  | 0.5     |         |         | $\mu s$ |       |
| Fast Dump Gate Trailing Delay          | $T_{FDT}$  | 0.5     |         |         | $\mu s$ |       |
| VCCD Line Clock Leading Edge Delay     | $T_{VL}$   | 0.2     | 0.3     | 0.4     | $\mu s$ |       |
| VCCD Line Clock Trailing Edge Delay    | $T_{VT}$   | 0.0     | 0.2     | 0.4     | $\mu s$ |       |

## Main Timing – Continuous Mode

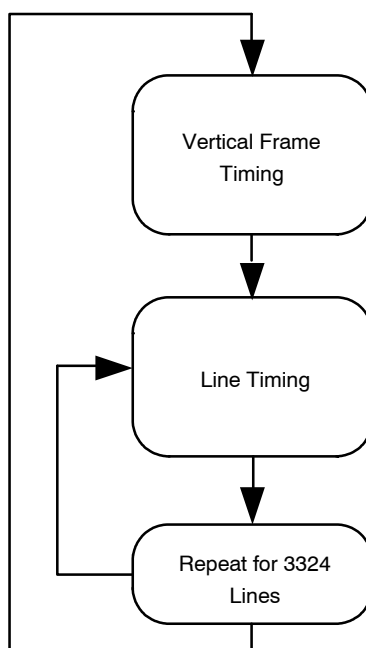


Figure 10. Main Timing – Continuous Mode

Frame Timing – Continuous Mode

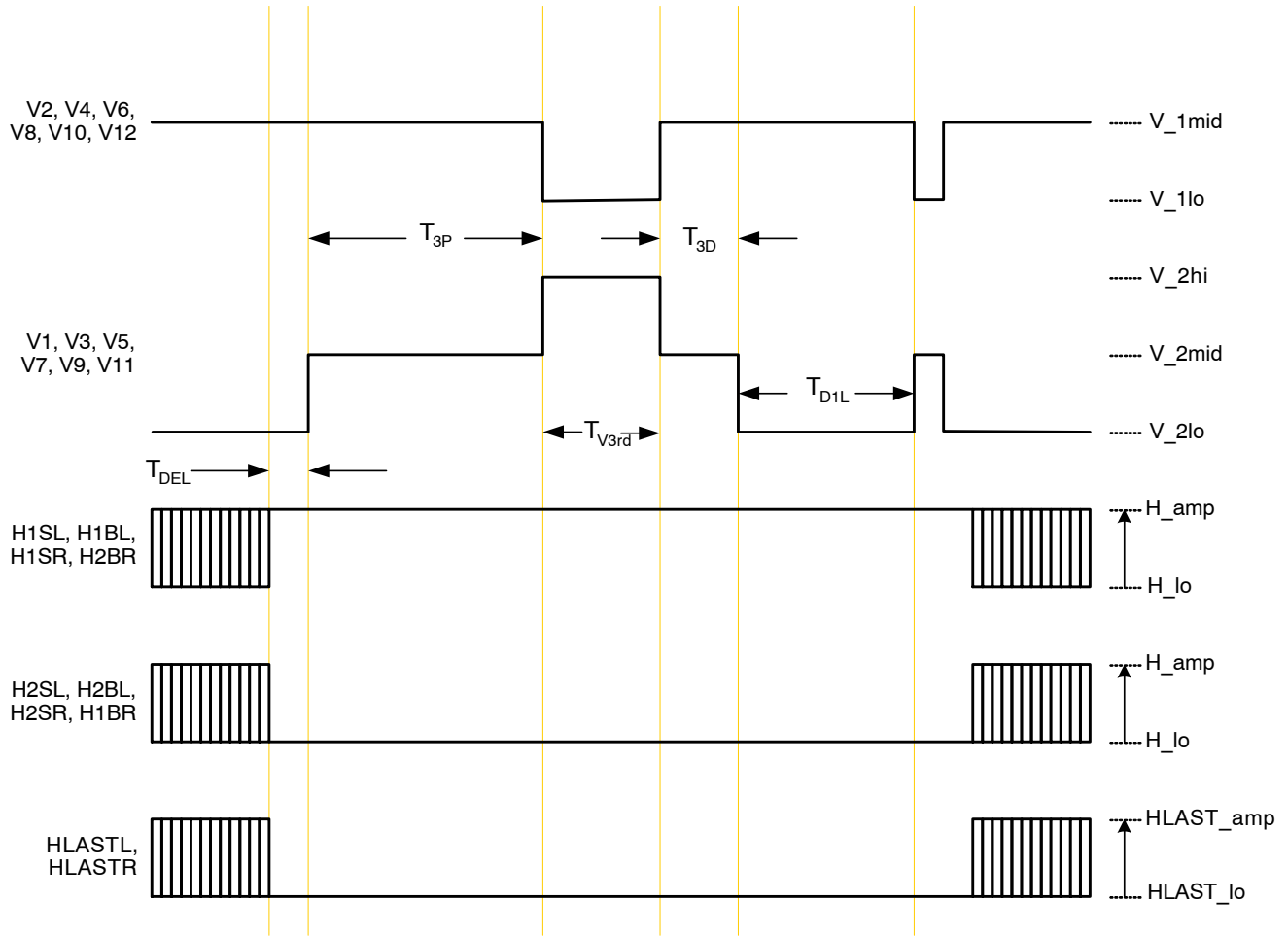


Figure 11. Framing Timing

Line Timing Continuous Mode

Line Timing Single Output

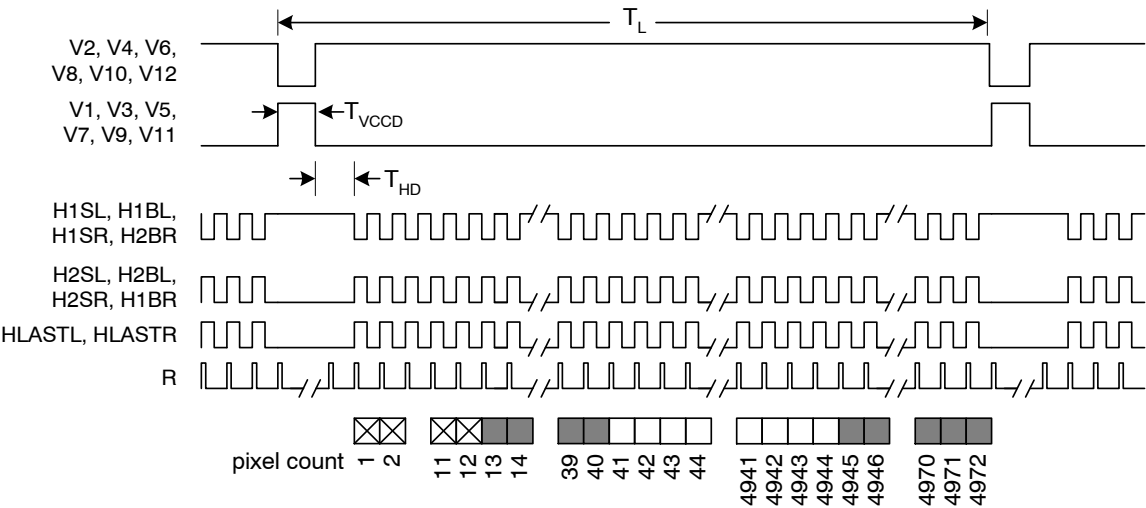


Figure 12. Line Timing Single Output

Line Timing Double Output

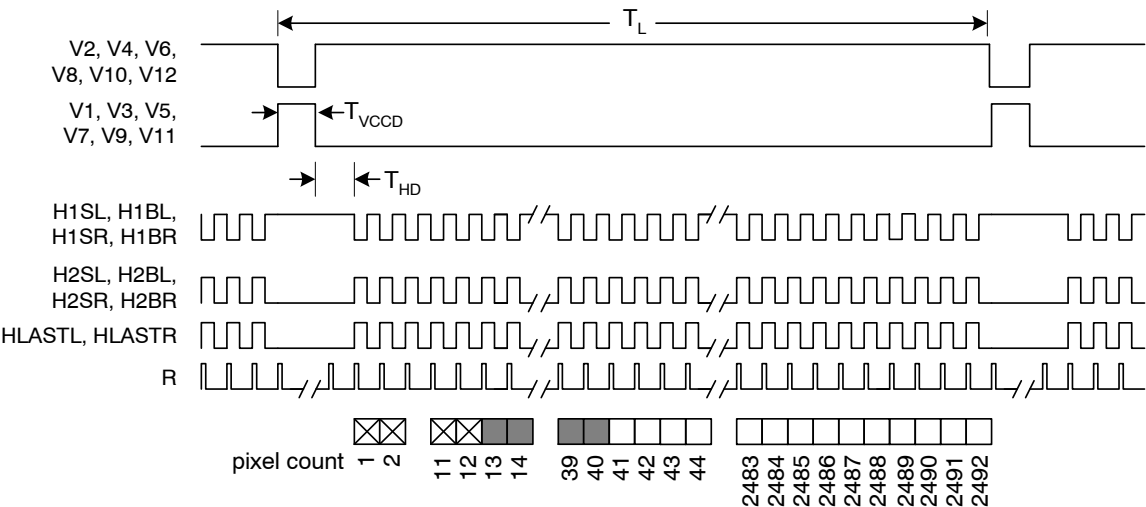


Figure 13. Line Timing Dual Output

Line Timing Detail Single Output

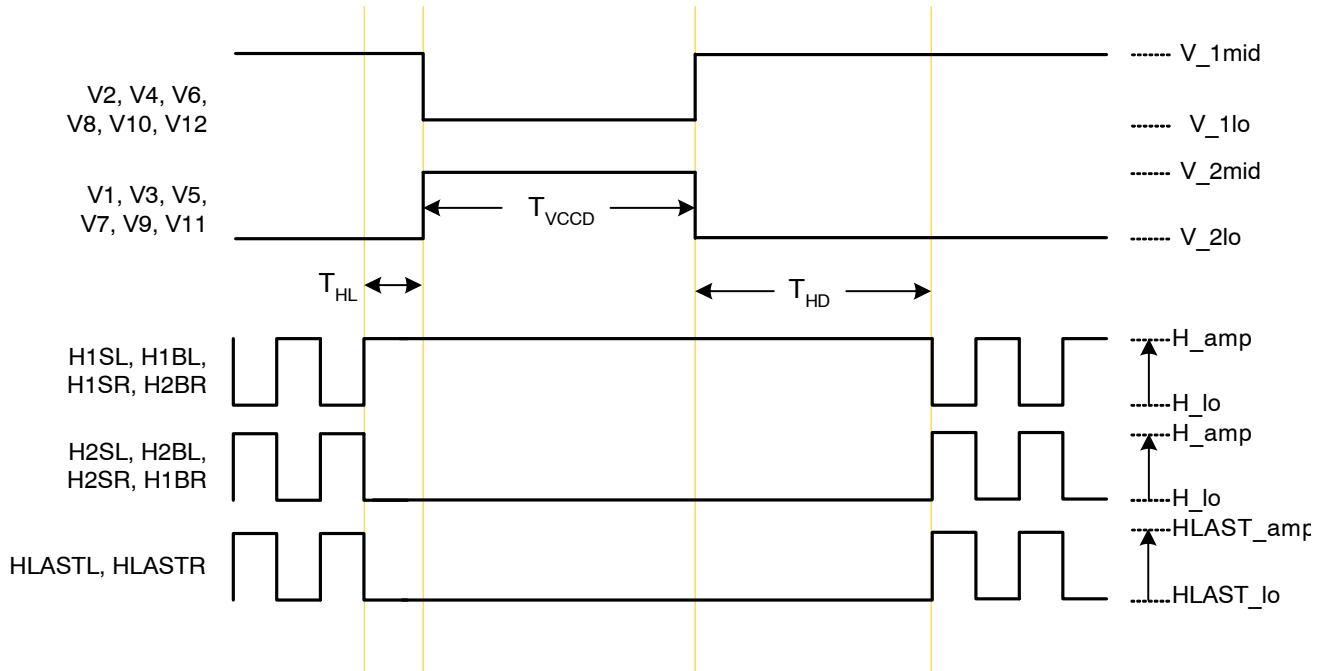


Figure 14. Line Timing Detail Single Output

Line Timing Detail Edge Alignment

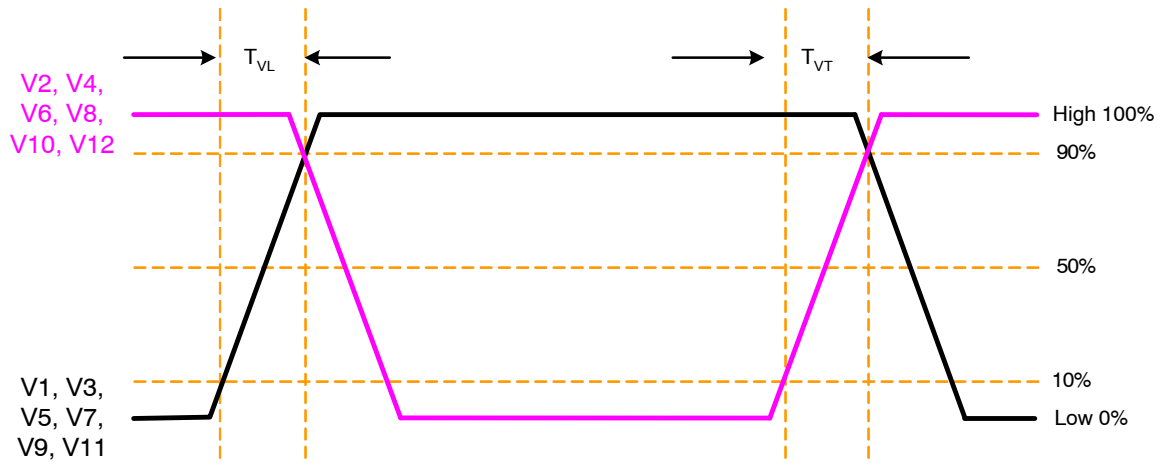


Figure 15. Line Timing Detail Edge Alignment

Pixel Timing

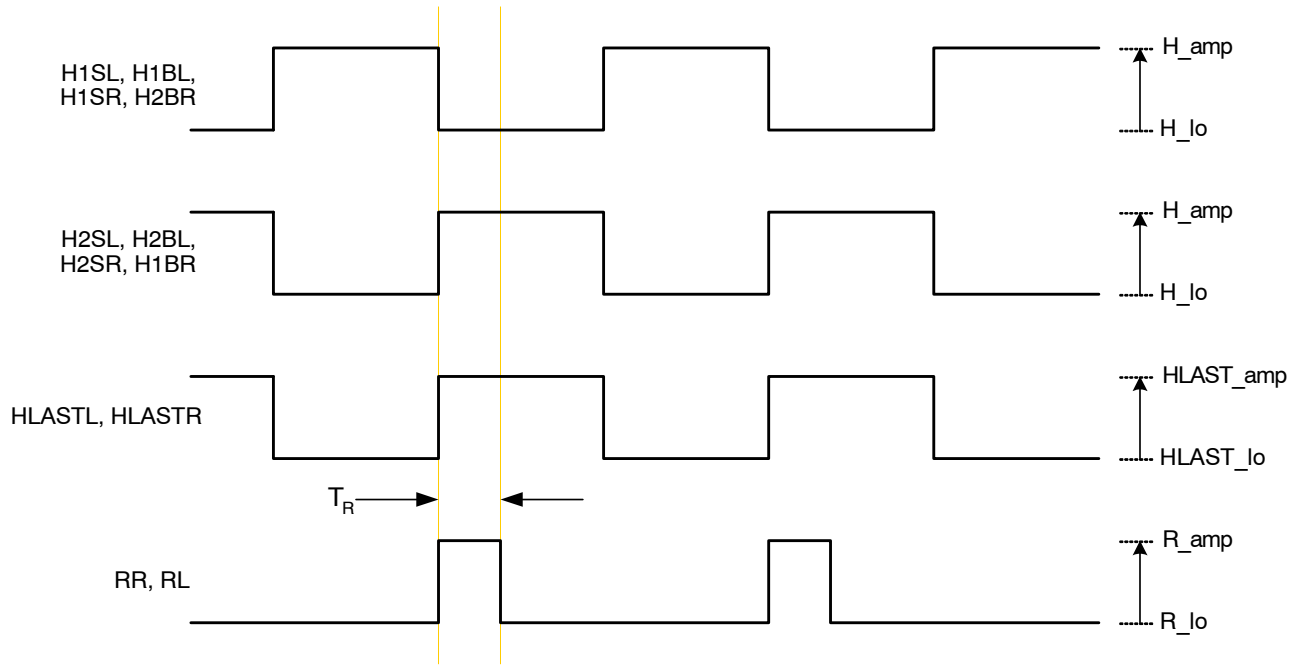


Figure 16. Pixel Timing

# Fast Line Dump Timing

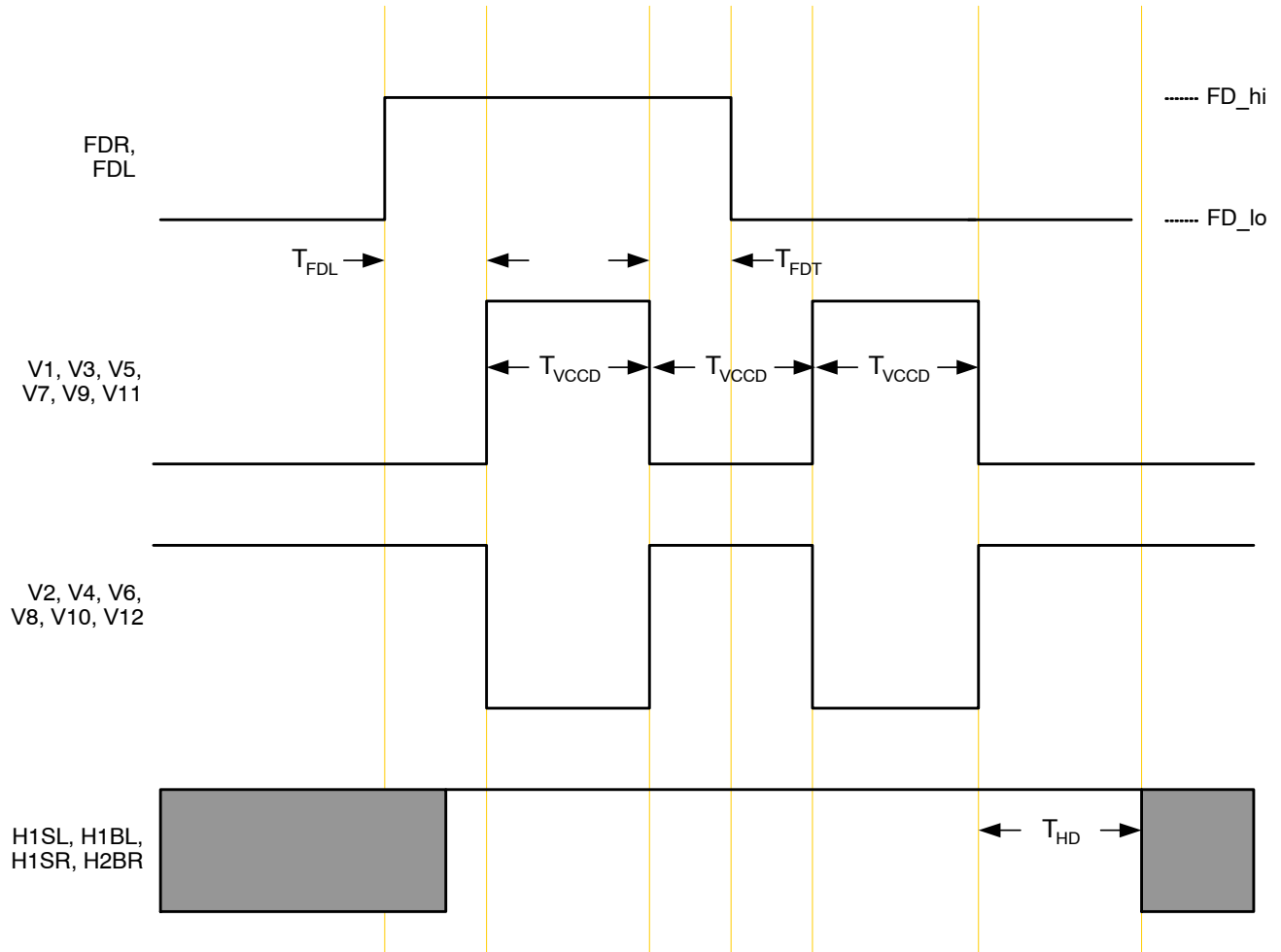


Figure 17. Fast Line Dump Timing

## Electronic Shutter Timing

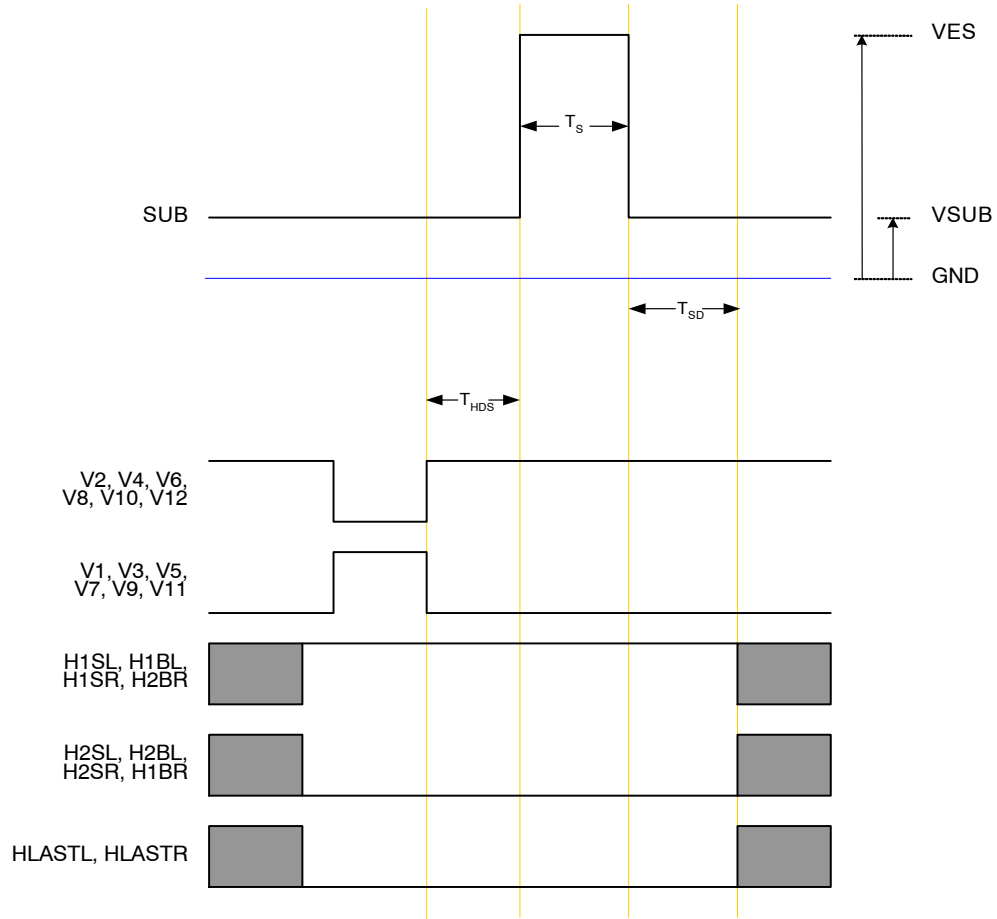


Figure 18. Electronic Shutter Timing

## Electronic Shutter Integration Time Definition

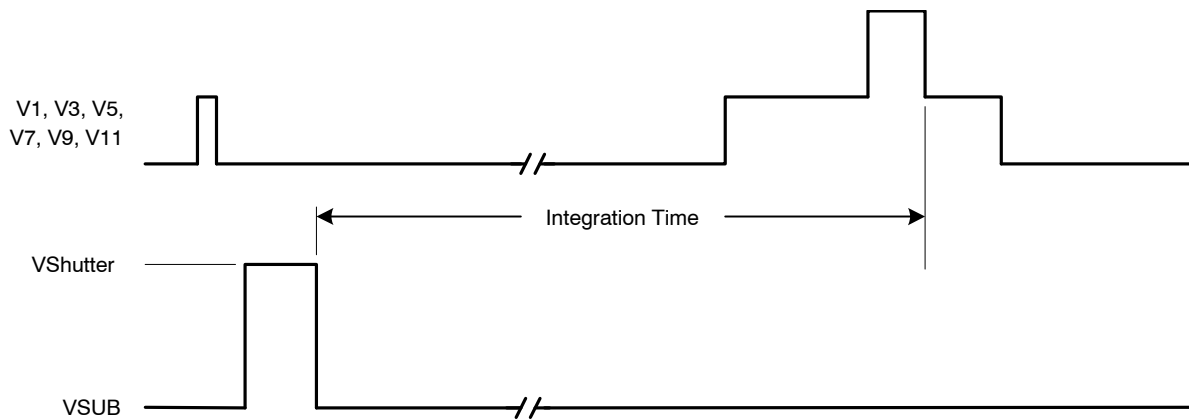


Figure 19. Integration Time Definition

## STORAGE AND HANDLING

Table 17. STORAGE CONDITIONS

| Description | Symbol | Minimum | Maximum | Units | Notes |
|-------------|--------|---------|---------|-------|-------|
| Temperature | T      | -55     | 80      | °C    | 1     |
| Humidity    | RH     | 5       | 90      | %     | 2     |

1. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
2. T = 25°C. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from [www.onsemi.com](http://www.onsemi.com).

For information on soldering recommendations, please download the *Soldering and Mounting Techniques Reference Manual* (SOLDERRM/D) from [www.onsemi.com](http://www.onsemi.com).

For quality and reliability information, please download the *Quality & Reliability Handbook* (HBD851/D) from [www.onsemi.com](http://www.onsemi.com).

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from [www.onsemi.com](http://www.onsemi.com).

For information on Standard terms and Conditions of Sale, please download [Terms and Conditions](http://www.onsemi.com) from [www.onsemi.com](http://www.onsemi.com).

## MECHANICAL DRAWINGS

## Completed Assembly

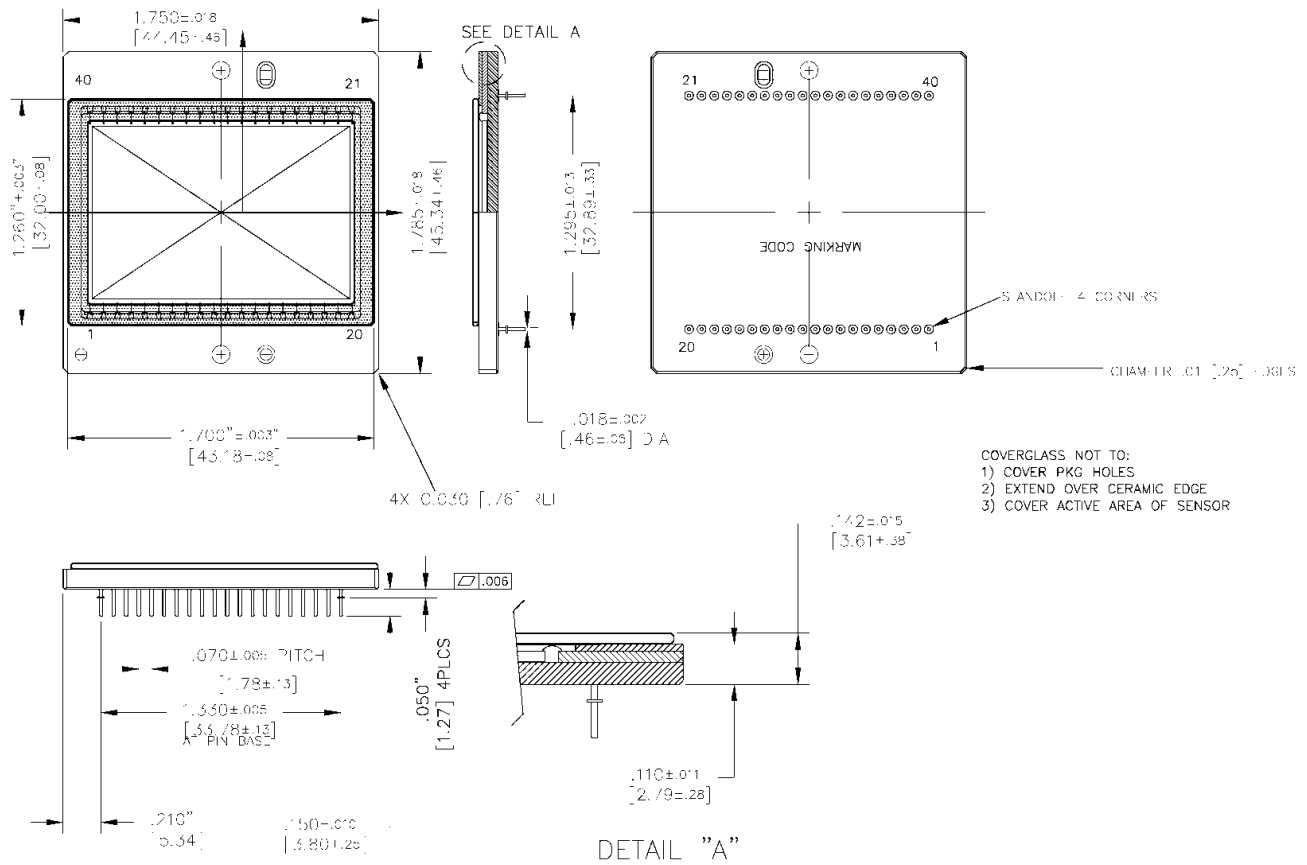


Figure 20. Completed Assembly (1 of 2)

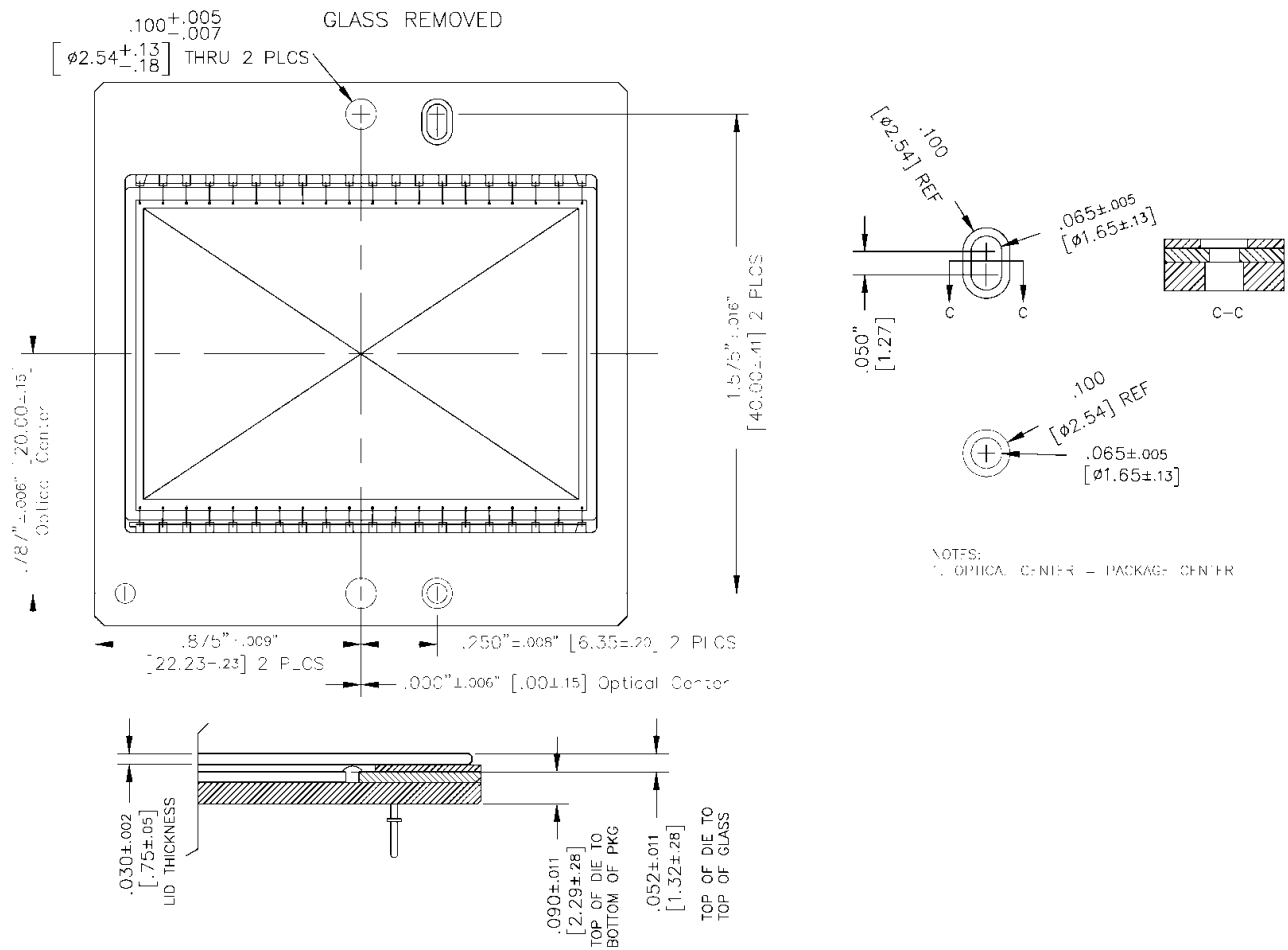
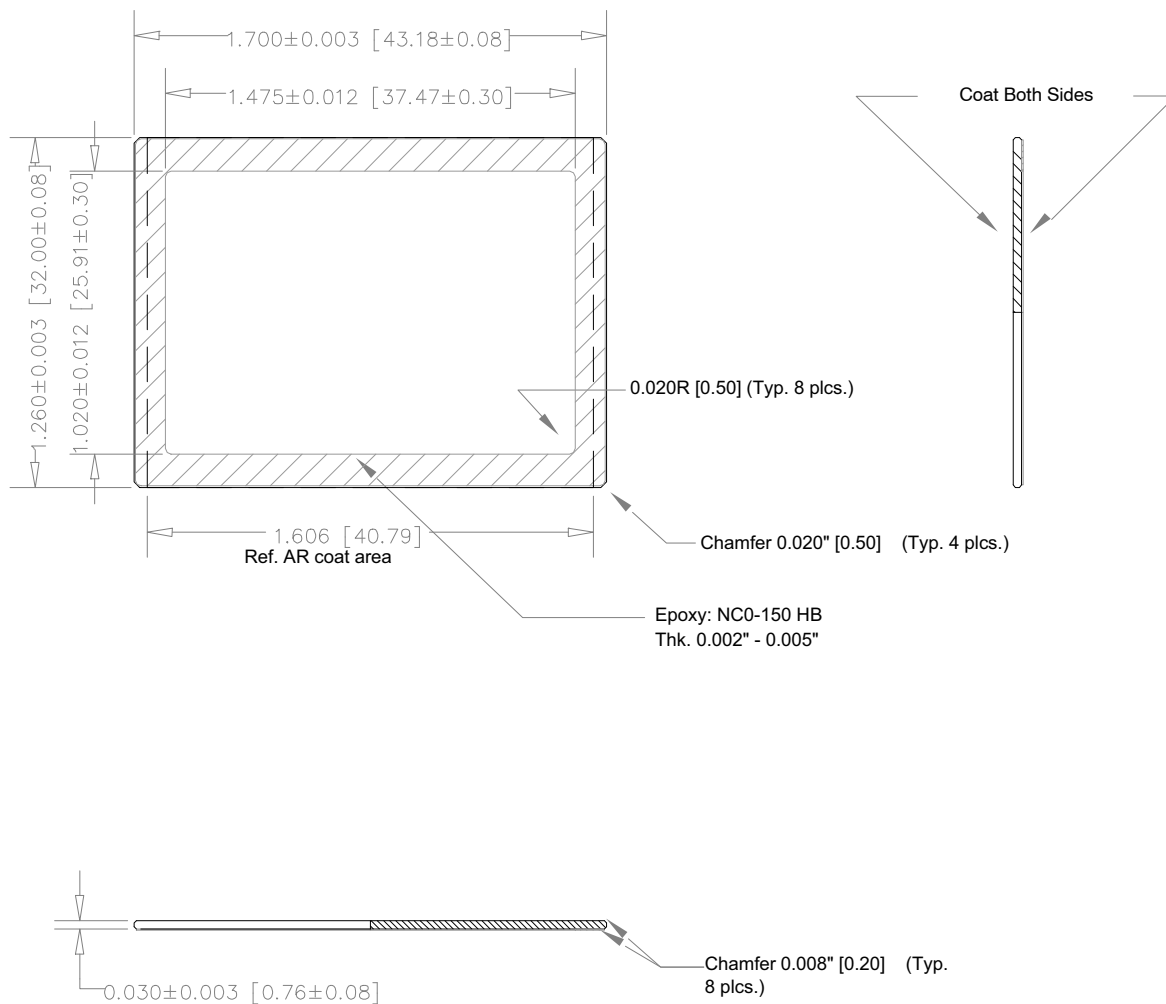


Figure 21. Completed Assembly (2 of 2)

## Cover Glass



## Notes:

## Double Sided AR Coated Glass

## 1. Multi-Layer Anti-Reflective Coating on 2 sides:

## Double Sided Reflectance:

## Range (nm)

420 - 450 nm &lt; 2%

450 - 630 nm &lt; 1%

630 - 680 nm &lt; 2%

## 2. Dust, Scratch Specification - 20 microns max.

## 3. Substrate - Schott D263T eco or equivalent

## 4. Epoxy: NCO-150HB

Thickness: 0.002" - 0.005"

## Clear Glass

## 1. Materials: Substrate - Schott D263T eco or equivalent

## 2. No epoxy

## 3. Dust, Scratch Count - 20 microns max.

## 4. Reflectance:

420 - 435 nm &lt; 10%

435 - 630 nm &lt; 10%

630 - 680 nm &lt; 10%

Figure 22. Glass Drawing

Glass Transmission

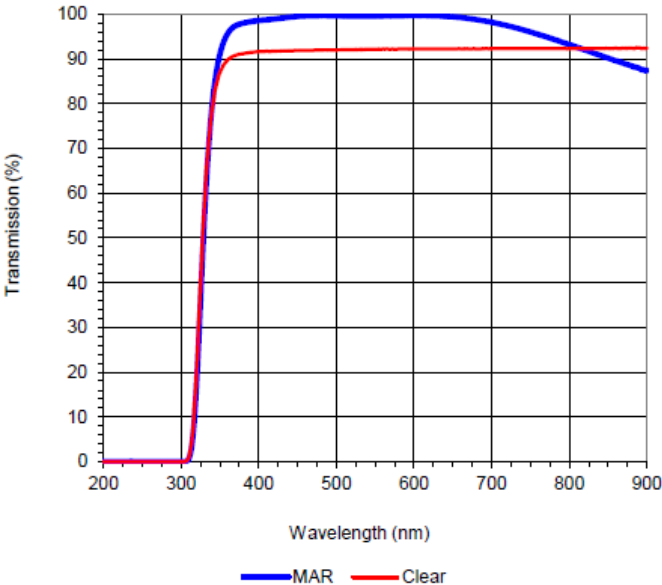


Figure 23. MAR and Clear Glass Transmission

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