Micropower Ultra-Sensitive Hall-Effect Switches

FEATURES AND BENEFITS

- AEC-Q100 automotive qualified
- Micropower operation
- Operate with north or south pole
- 2.4 to 5.5 V battery operation
- Chopper stabilized
  - □ Superior temperature stability
  - □ Extremely low switchpoint drift
  - □ Insensitive to physical stress
- High ESD protection
- Solid-state reliability
- Small size
- Easily assembly into applications due to magnetic pole independence

PACKAGES:

Not to scale

3-pin SOT23W
(suffix LH)

3-pin SIP,
matrix HD style
(suffix UA)

3-pin SIP,
chopper style
(suffix UA)

DESCRIPTION

The A3213 and A3214 integrated circuits are ultra-sensitive, pole-independent Hall-effect switches with a latched digital output. They are especially suited for operation in battery-operated, hand-held equipment such as cell and cordless telephones and palmtop computers. A 2.4 to 5.5 V operation and a unique clocking scheme reduce the average operating power requirements: the A3213 to 825 µW, the A3214 to 14 µW (typical, at 2.75 V). Except for operating duty cycle and average operating current, the A3213 and A3214 are identical.

Unlike other Hall-effect switches, either a north or south pole of sufficient strength will turn the output on; in the absence of a magnetic field, the output is off. The polarity independence and minimal power requirement allows these devices to easily replace reed switches for superior reliability and ease of manufacturing, while eliminating the requirement for signal conditioning.

Improved stability is made possible through chopper stabilization (dynamic offset cancellation), which reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress.

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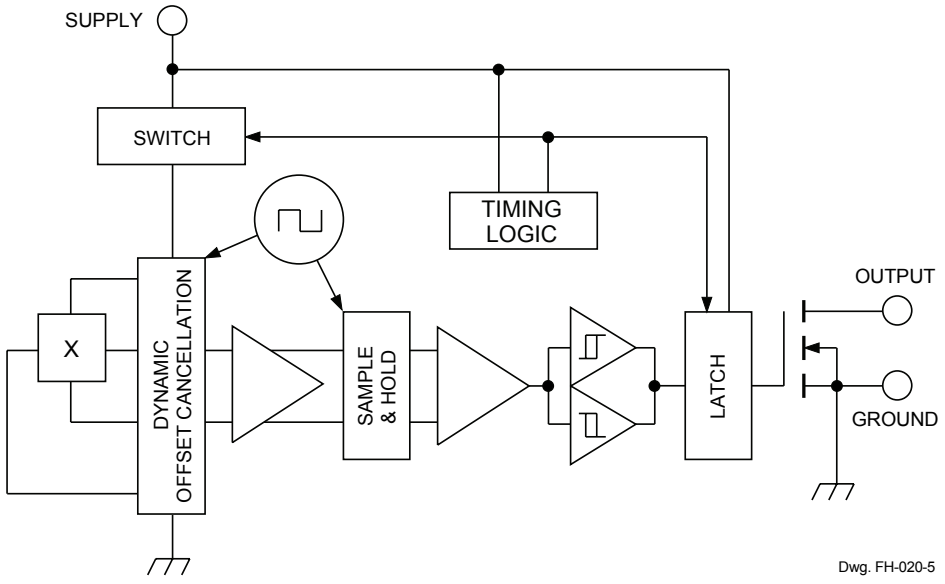


Functional Block Diagram

DESCRIPTION (continued)

These devices include, on a single silicon chip, a Hall-voltage generator, small-signal amplifier, chopper stabilization, a latch, and a MOSFET output. Advanced BiCMOS processing is used to take advantage of low-voltage and low-power requirements, component matching, very low input-offset errors, and small component geometries.

Devices are rated for operation over a temperature range of –40°C to 85°C or –40°C to 150°C. Two package styles provide a magnetically optimized package for most applications. 'LH' is a miniature low-profile surface-mount package, 'UA' is a three-lead SIP for through-hole mounting. Each package is lead (Pb) free (suffix, –T) , with a 100% matte-tin-plated leadframe.

SPECIFICATIONS

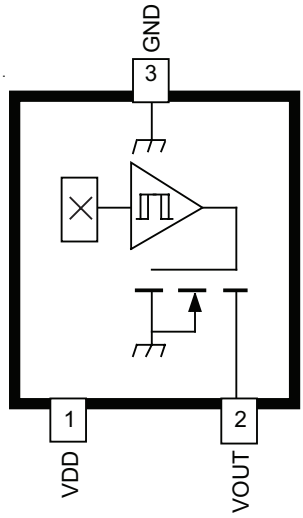
SELECTION GUIDE

Part Number	Mounting	Packing [1]	Ambient [1], T_A (°C)	DC (%)	$I_{DD(AVG)}$(typ) (µA)
A3213ELHLT-T	LH package Surface Mount	7-in. reel 3000 pieces/reel	–40 to 85	25	309
A3213ELHLX-T	LH package Surface Mount	13-in. reel 10000 pieces/reel			
A3213EUA-T [2]	UA package SIP through hole	Bulk 500 pieces/bag			
A3213LUA-T [2]	UA package SIP through hole	Bulk 500 pieces/bag	–40 to 150		
A3214ELHLT-T	LH package Surface Mount	7-in. reel 3000 pieces/reel	–40 to 85	0.10	6
A3214ELHLX-T	LH package Surface Mount	13-in. reel 10000 pieces/reel			
A3214EUA-T [2]	UA package SIP through hole	Bulk 500 pieces/bag			

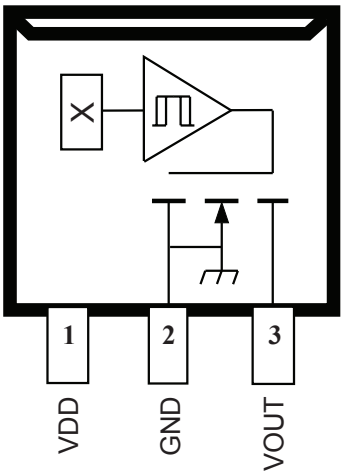
[1] Contact Allegro for additional packing and operating temperature range options.
[2] The chopper-style UA package is not for new design; the matrix HD style UA package is recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{DD}		6	V
Magnetic Flux Density	B		Unlimited	G
Output Off Voltage	V_{OUT}		6	V
Output Current	I_{OUT}		1	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range L	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C



LH Package, 3-Pin SOT23W Pinout Diagram



UA Package, 3-Pin SIP Pinout Diagram

Terminal List Table

Number		Name	Description
LH	UA		
1	1	VDD	Input power supply; tie to GND with bypass capacitor
3	2	GND	Ground
2	3	VOUT	Output signal

ELECTRICAL CHARACTERISTICS: Valid over operating voltage and temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Units
Supply Voltage Range	V_{DD}	Operating [2]	2.4	3.0	5.5	V
Output Leakage Current	I_{OFF}	V_{OUT} = 5.5 V, $B_{RPN} < B < B_{RPS}$	–	<1.0	1.0	µA
Output On Voltage	$V_{OUT(ON)}$	Output on, I_{OUT} = 1 mA, V_{DD} = 3.0 V	–	100	300	mV
Awake Time	t_{awake}		–	60	90	µs
Period	t_{period}	A3213	–	240	360	µs
		A3214, T_A = 25°C, V_{DD} = 3 V	–	60	90	ms
Duty Cycle	DC	A3213	–	25	–	%
		A3214	–	0.10	–	%
Chopping Frequency	f_C		–	340	–	kHz
Supply Current	$I_{DD(EN)}$	Chip awake (enabled)	–	–	2.0	mA
	$I_{DD(DIS)}$	Chip asleep (disabled)	–	–	8.0	µA
	$I_{DD(AVG)}$	A3213	–	309	850	µA
		A3214	–	6	22	µA

[1] Typical Data is at T_A = 25°C and V_{DD} = 3.0 V and is for design information only.
[2] Operate and release points will vary with supply voltage. B_{OPx} = operate point (output turns ON); B_{RPx} = release point (output turns OFF).

MAGNETIC CHARACTERISTICS [3]: valid over operating voltage and temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ. [5]	Max.	Units [6]
Operate Points [4]	B_{OPS}	South pole to branded side	–	42	70	G
	B_{OPN}	North pole to branded side	–70	–48	–	G
Release Points [4]	B_{RPS}	South pole to branded side	10	32	–	G
	B_{RPN}	North pole to branded side	–	–38	–10	G
Hysteresis	B_{hys}	$\lvert B_{OPx} - B_{RPx} \rvert$	–	10	–	G

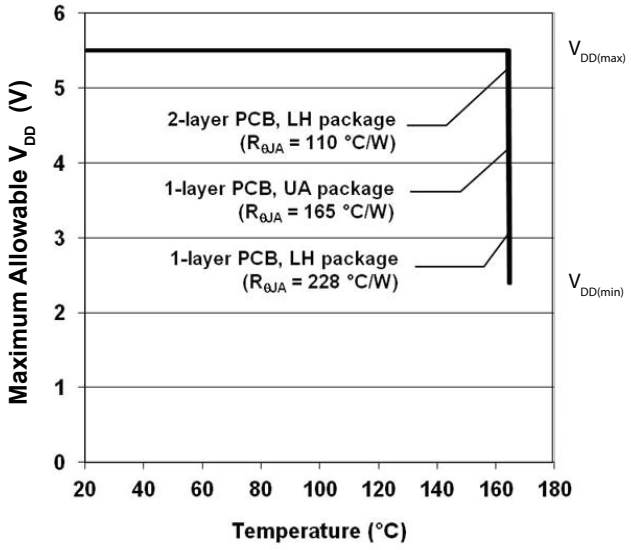
[3] As used here, negative flux densities are defined as less than zero (algebraic convention) and -50 G is less than +10 G.
[4] B_{OPx} = operate point (output turns ON); B_{RPx} = release point (output turns OFF).
[5] Typical Data is at T_A = 25°C and V_{DD} = 3.0 V and is for design information only.
[6] 1 gauss (G) is exactly equal to 0.1 millitesla (mT).

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

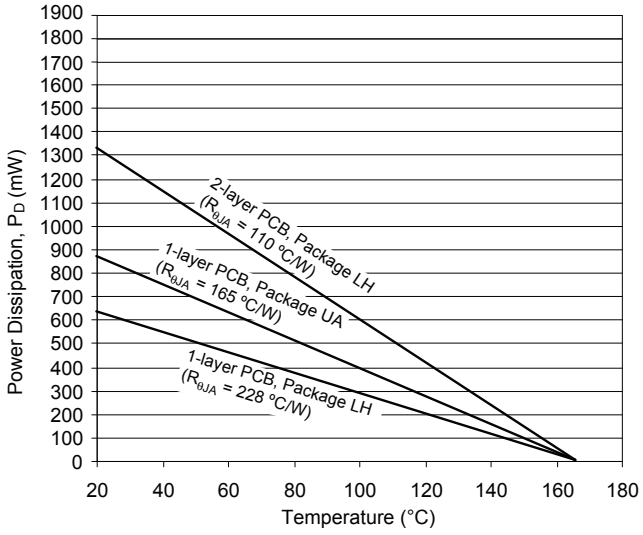
Characteristic	Symbol	Test Conditions [1]	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	°C/W
		Package LH, 2-layer PCB with 0.463 in.^{2} of copper area each side connected by thermal vias	110	°C/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W

[1] Additional thermal information available on Allegro website.

Power Derating Curve

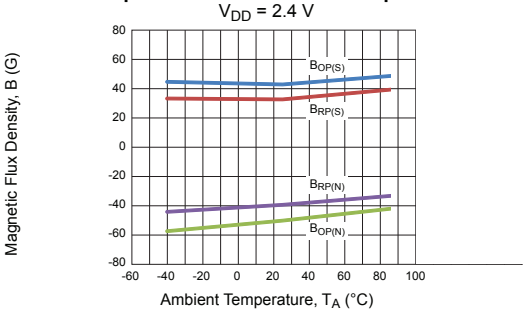


Power Dissipation versus Ambient Temperature

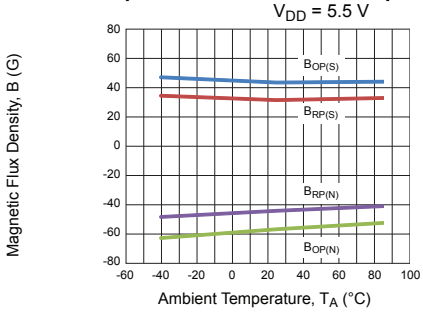


TYPICAL OPERATING CHARACTERISTICS

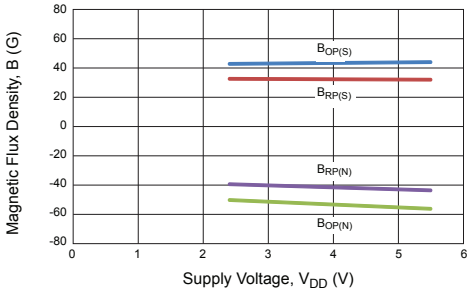
A3213 and A3214
Switchpoints versus Ambient Temperature
V_{DD} = 2.4 V



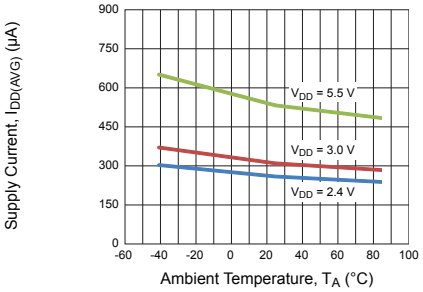
A3213 and A3214
Switchpoints versus Ambient Temperature
V_{DD} = 5.5 V



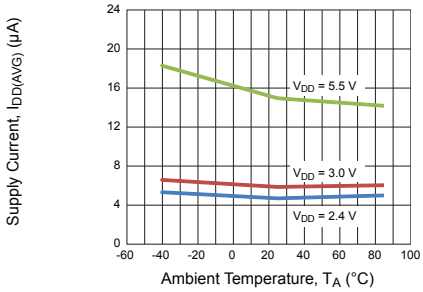
A3213 and A3214
Switchpoints versus Supply Voltage
T_A = 25°C



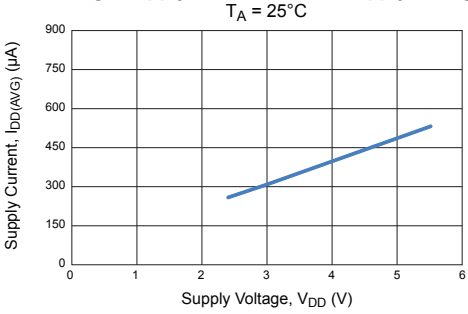
A3213
Average Supply Current versus Temperature



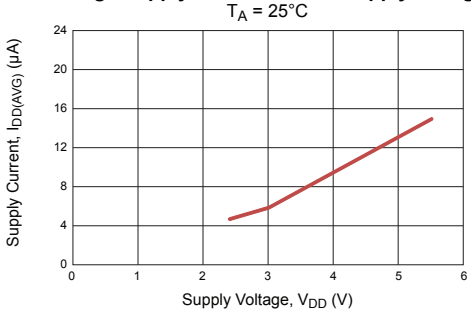
A3214
Average Supply Current versus Temperature



A3213
Average Supply Current versus Supply Voltage
T_A = 25°C



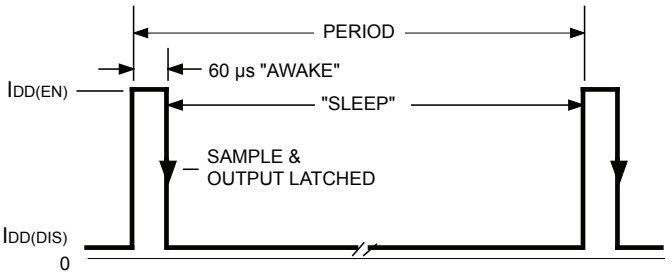
A3214
Average Supply Current versus Supply Voltage
T_A = 25°C



FUNCTIONAL DESCRIPTION

Low Average Power

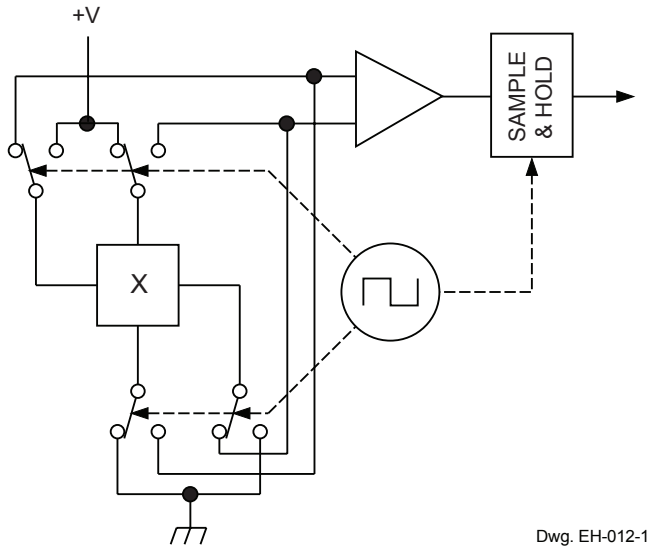
Internal timing circuitry activates the IC for 60 µs and deactivates it for the remainder of the period (240 µs (typ) for the A3213 and 60 ms (typ) for the A3214). A short "awake" time allows for stabilization prior to the sampling and data latching on the falling edge of the timing pulse. The output during the "sleep" time is latched in the last sampled state. The supply current is not affected by the output state.



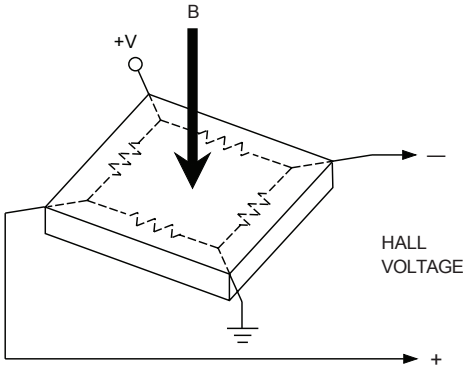
Chopper-Stabilized Technique

The Hall element can be considered as a resistor array similar to a Wheatstone bridge. A large portion of the offset is a result of the mismatching of these resistors. These devices use a dynamic offset cancellation technique, with an internal high-frequency clock to reduce the residual offset voltage of the Hall element that is normally caused by device overmolding, temperature dependencies, and thermal stress. The chopper-stabilizing technique cancels the mismatching of the resistor circuit by changing the direction of the current flowing through the Hall plate using CMOS switches and Hall voltage measurement taps, while maintaing the Hall-voltage signal that is induced by the external magnetic flux. The signal is then captured by a sample-and-hold circuit and further processed using low-offset bipolar circuitry. This technique produces devices that have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique will also slightly degrade the device output repeatability. A relatively high sampling frequency is used in order that faster signals can be processed.

More detailed descriptions of the circuit operation can be found in Technical Paper STP 97-10, *Monolithic Magnetic Hall Sensing Using Dynamic Quadrature Offset Cancellation* and Technical Paper STP 99-1, *Chopper-Stabilized Amplifiers With A Track-and-Hold Signal Demodulator*.



Dwg. EH-012-1



Dwg. AH-011-2

Operation

The output of this device switches low (turns on) when a magnetic field perpendicular to the Hall element exceeds the operate point B_{OPS} (or is less than B_{OPN}). After turn-on, the output is capable of sinking up to 1 mA and the output voltage is $V_{OUT(ON)}$. When the magnetic field is reduced below the release point B_{RPS} (or increased above B_{RPN}), the device output switches high (turns off). The difference in the magnetic operate and release points is the hysteresis (B_{hys}) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

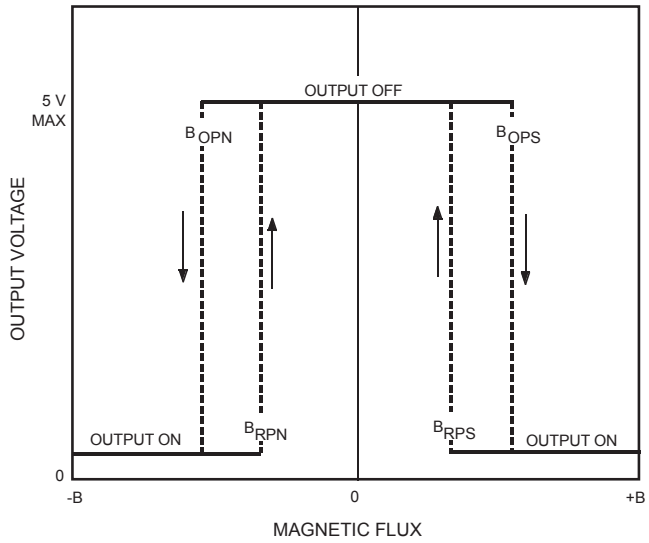
As used here, negative flux densities are defined as less than zero (algebraic convention) and -50 G is less than +10 G.

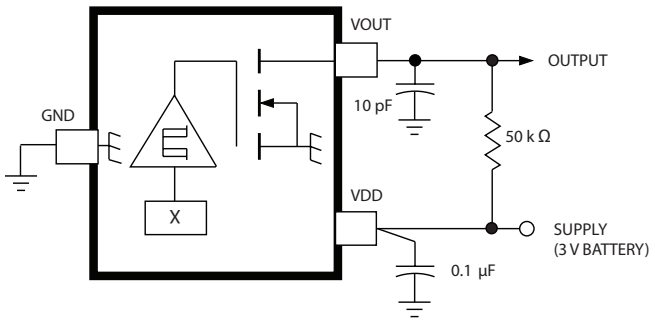
Applications

Allegro's pole-independent sensing technique allows for operation with either a north pole or south pole magnet orientation, enhancing the flexibility of the device in application assembling. The technology provides the same output polarity for either pole face.

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper-stabilization technique. This is especially true due to the relatively high impedance of battery supplies.

The simplest form of magnet that will operate these devices is a bar magnet with either pole near the branded surface of the device. Many other methods of operation are possible. Extensive applications information on magnets and Hall-effect devices is also available on the Allegro website: www.allegromicro.com.

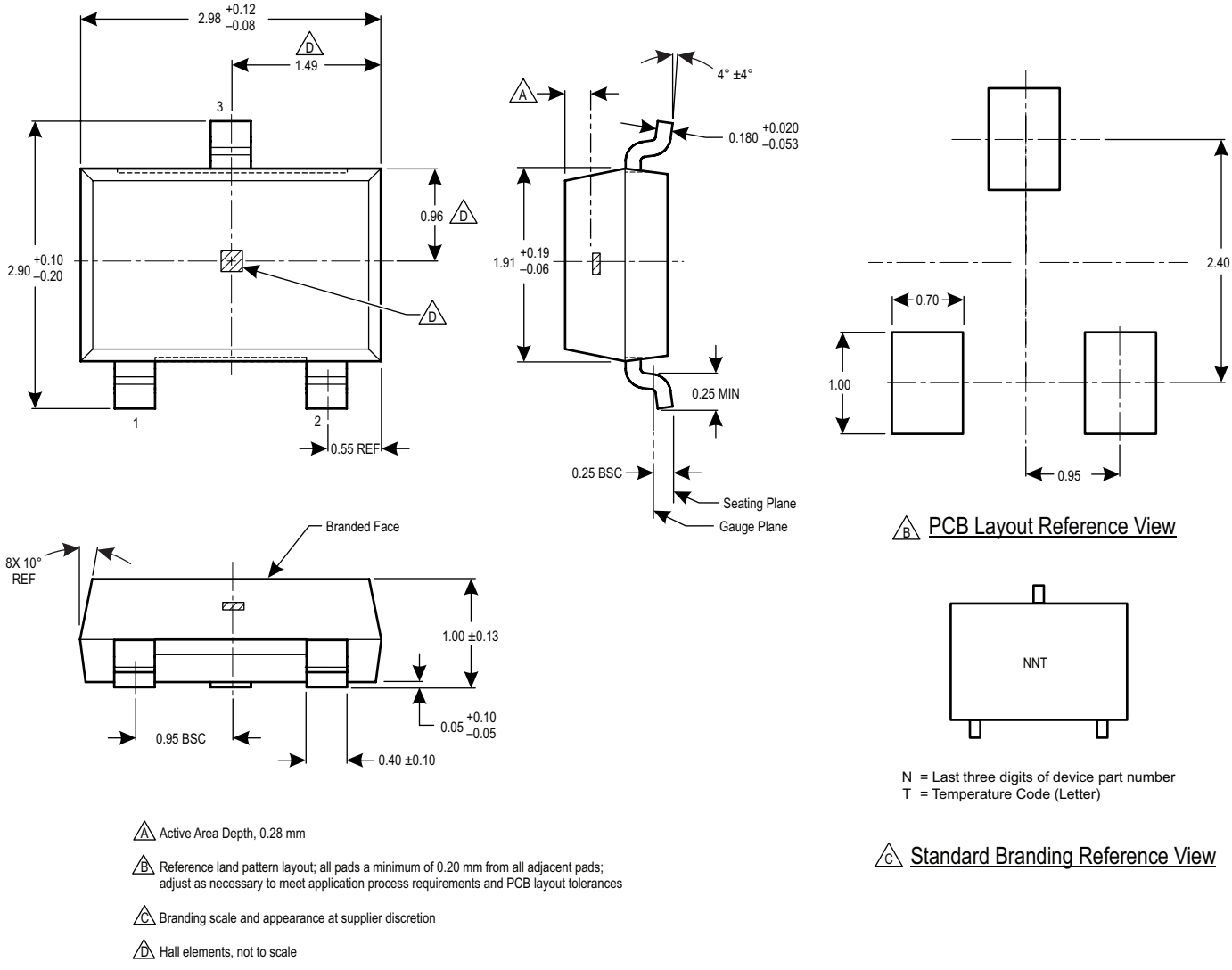




CUSTOMER PACKAGE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-2840)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Active Area Depth, 0.28 mm

B Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall elements, not to scale

Figure 1: Package LH, 3-Pin (SOT-23W)

For Reference Only – Not for Tooling Use

(Reference DWG-9049)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

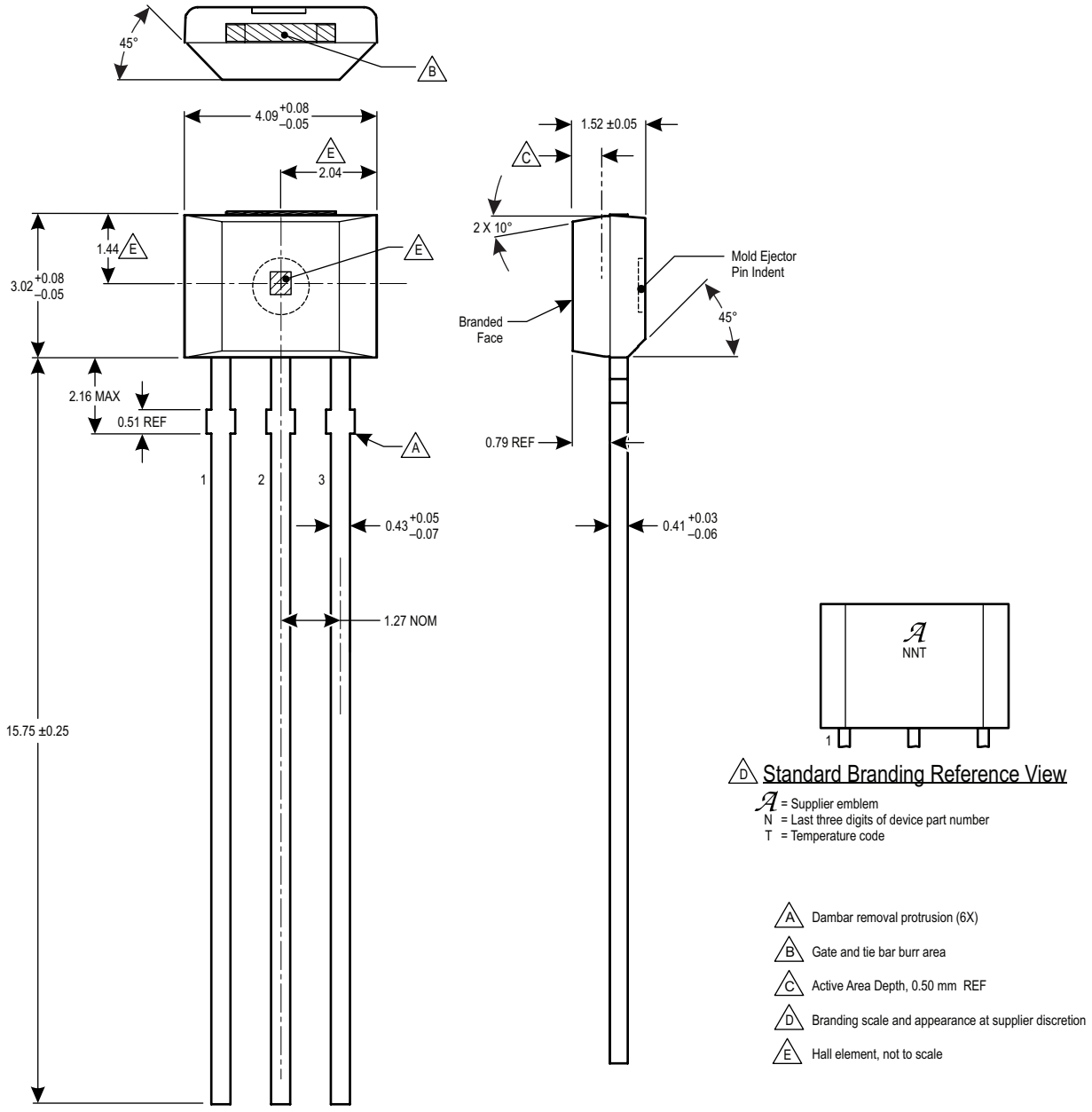


Figure 2: Package UA, 3-Pin SIP, Matrix Style

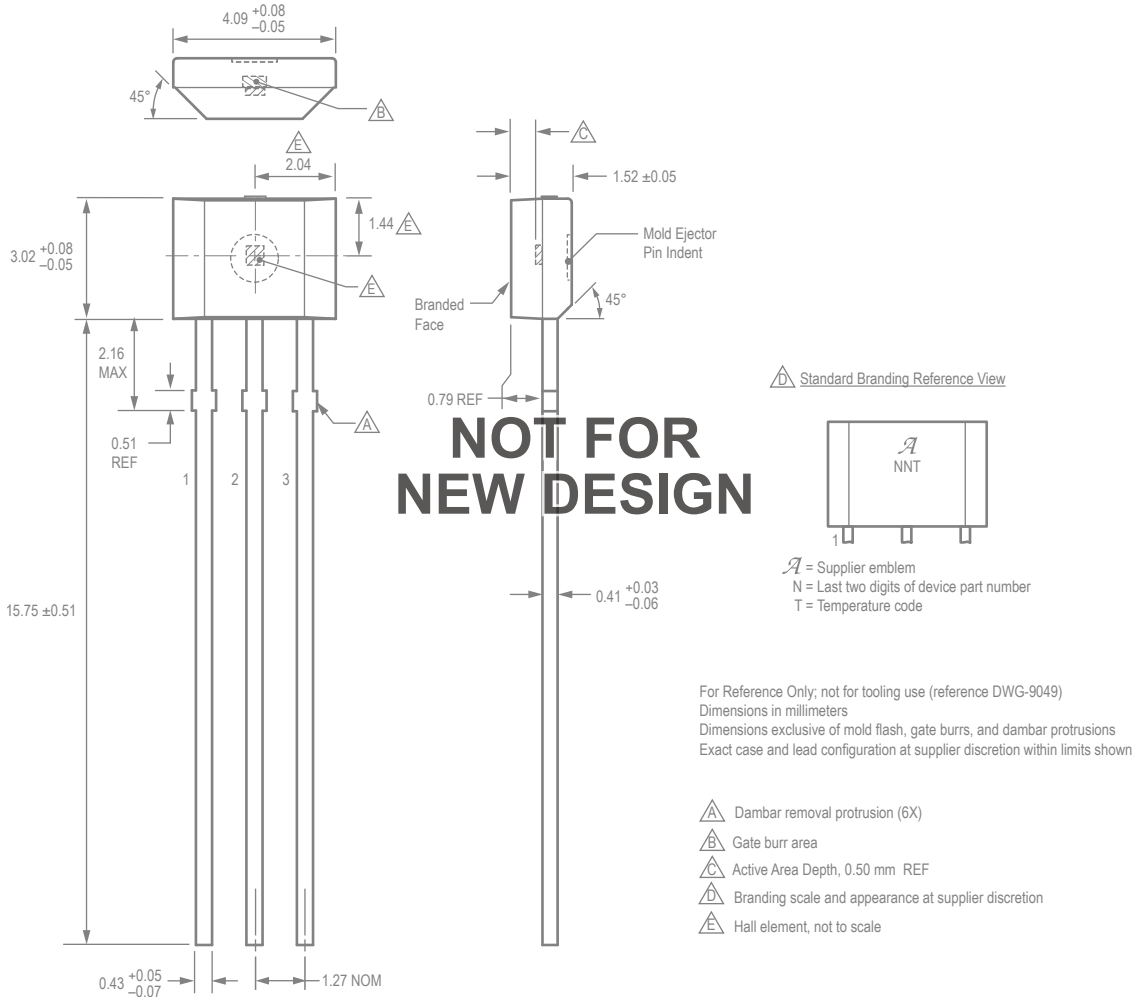


Figure 3: Package UA, 3-Pin SIP, Chopper Style

Revision History

Number	Date	Description
25	October 29, 2012	Update product selection
26	January 6, 2015	Added LX option to Selection Guide
27	September 22, 2015	Corrected LH package Active Area Depth value; added AEC-Q100 qualification under Features and Benefits
28	October 31, 2016	Chopper-style UA package designated as not for new design

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