CY7C65210, CY7C65217
CY7C65210A, CY7C65217A

USB Billboard Controller

Features

- USB 2.0-certified, Full-Speed (12 Mbps)
  - Supports native Billboard Device Class Driver
  - Integrated USB termination resistors
- CY7C65210/210A: Single-channel I^2C interface
  - Master up to 400 kHz
  - 190 bytes for each transmit and receive buffer
- CY7C65217/217A: Dual-channel UART/I^2C interface
  - UART interface
    - Supports 2 pin
    - Data rates up to 115200 bps
    - 190 bytes for each transmit and receive buffer
    - Data format: 7 or 8 data bits, 1 or 2 stop bits
    - No parity, even, odd, mark, or space parity
    - Supports parity, overrun, and framing errors
    - Supports single-channel RS-232 and RS-422 interface
  - I^2C Interface
    - Master up to 400 kHz
    - 190 bytes for each transmit and receive buffer
- General-purpose input/output (GPIO) pins:
  - CY7C65210: 9
  - CY7C65217: 7
  - CY7C65210A: 11
  - CY7C65217A: 9
- 2560 bytes flash for storing configuration parameters
- Billboard Device Class-specific descriptors
- Driver support for Billboard Device
  - Billboard Device Class is natively supported by Windows 10
- Clocking: Integrated 48-MHz clock oscillator
- Supports bus- or self-powered configurations
- USB Suspend mode for low power
- Operating voltage: 1.71 V to 5.5 V
- Operating temperature:
  - Commercial: 0 °C to 70 °C
  - Industrial: –40 °C to 85 °C
- ESD protection: 2.2-kV HBM
- RoHS-compliant package
  - 24-pin QFN (4.0 mm × 4.0 mm, 0.55 mm, 0.5-mm pitch)
- Ordering part number
  - CY7C65210-24LTXI
  - CY7C65217-24LTXI
  - CY7C65210A-24LTXI
  - CY7C65217A-24LTX

Applications

Any Type-C Device Container that supports Alternate Mode requires Billboard Device support such as:

- Dongles for Type-C
- Docking Stations
- Monitors

Functional Description

The CY7C6521x[1] is a Full-Speed USB controller, which enumerates as a Billboard Device. It integrates a voltage regulator, an oscillator, and flash memory for storing configuration parameters, offering a cost-effective solution. CY7C6521x supports bus-powered mode and enables efficient system power management with suspend and remote wake-up signals. It is available in a 24-pin QFN package.

For a complete list of related resources, click here.

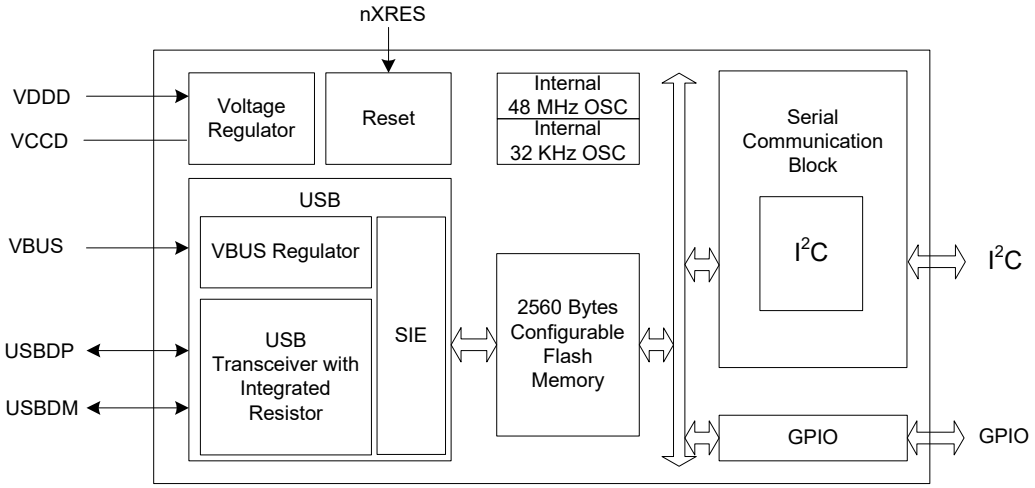
Comparison of Billboard Parts

Feature	CY7C65210	CY7C65217	CY7C65210A	CY7C65217A
Billboard Spec	1.1	1.1	1.21	1.21
Number of GPIOs	9	7	11	9
Suspend/Wakeup Support	Yes	Yes	No*	No*

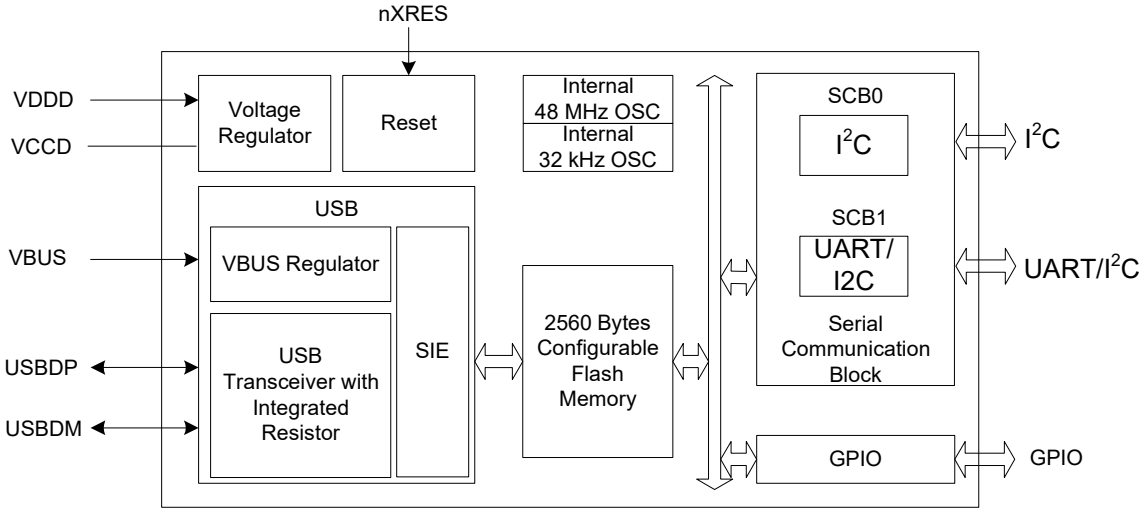
* Because these features are not relevant to Billboard, support for these features is removed.

Note
1. CY7C6521x refers to CY7C65210, CY7C65217, CY7C65210A, and CY7C65217A.

Block Diagram – CY7C65210, CY7C65210A



Block Diagram – CY7C65217, CY7C65217A



More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right device for your design, and to help you to quickly and effectively integrate the device into your design.

- Overview: USB Portfolio, USB Roadmap
- USB 2.0 Product Selectors: USB-Serial Bridge Controller, USB to UART Controller (Gen I), enCoRe II, enCoRe III, enCoRe V
- Code Examples: USB Full-Speed
- Models: IBIS

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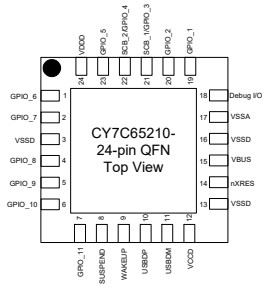
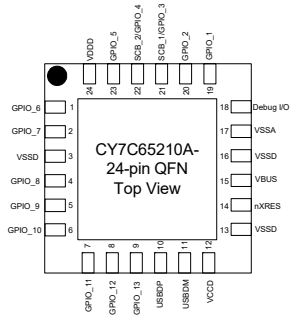
CY7C65210 and CY7C65210A Pin Description

Pin[2]	Type	Name	Default	Description	
1	GPIO	GPIO_6	Tristate	GPIO	
2	GPIO	GPIO_7	Tristate	GPIO	
3	Power	VSSD	–	Digital Ground	
4	GPIO	GPIO_8	Tristate	GPIO	
5	GPIO	GPIO_9	Tristate	GPIO	
6	GPIO	GPIO_10	Tristate	GPIO	
7	GPIO	GPIO_11	POWER#	GPIO (CY7C65210)	
	GPIO	GPIO_11	Tristate	GPIO (CY7C65210A)	
8	Output	SUSPEND	–	On CY7C65210, this pin indicates that the device in Suspend mode. Can be configured as active LOW/HIGH using the configuration utility.	
	GPIO	GPIO_12	Tristate	On CY7C65210A, this pin serves as GPIO.	
9	Input	WAKEUP	–	On CY7C65210, this pin is configured to wake up the device from Suspend mode. Can be configured as active LOW/HIGH using the configuration utility.	
	GPIO	GPIO_13	Tristate	On CY7C65210A, this pin serves as GPIO.	
10	USBIO	USBDP	–	USB Data Signal Plus, integrates termination resistor and a 1.5-kΩ pull-up resistor	
11	USBIO	USBDM	–	USB Data Signal Minus, integrates termination resistor	
12	Power	VCCD	–	This pin should be decoupled to ground using a 1-µF capacitor or by connecting a 1.8-V supply	
13	Power	VSSD	–	Digital Ground	
14	nXRES	nXRES	–	Chip reset, active low. Can be left unconnected or have a pull-up resistor connected if not used	
15	Power	VBUS	–	VBUS Supply, 3.15 V to 5.25 V	
16	Power	VSSD	–	Digital Ground	
17	Power	VSSA	–	Analog Ground	
18	Input	Debug I/O	–	Used for debug purpose. Should be left floating.	
19	GPIO	GPIO_1	Input	Can be used as wakeup source to wakeup device from Suspend mode.	
20	GPIO	GPIO_2	Tristate	GPIO	
21	SCB/GPIO	SCB_1/GPIO_3	SCL	I^2C SCL	
22	SCB/GPIO	SCB_2/GPIO_4	SDA	I^2C SDA	
23	GPIO	GPIO_5	Tristate	GPIO	
24	Power	VDDD	–	Supply to the device core and Interface, 1.71 V to 5.5 V	

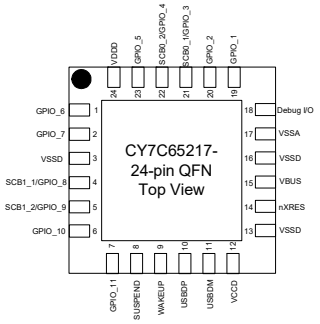




Note
2. Any pin acting as an Input pin should not be left unconnected.

CY7C65217 and CY7C65217A Pin Description

Pin[2]	Type	Name	Default	Description	
1	GPIO	GPIO_6	Tristate	GPIO	
2	GPIO	GPIO_7	Tristate	GPIO	
3	Power	VSSD	–	Digital Ground	
4	SCB/GPIO	SCB1_0/GPIO_8	RXD	UART RXD/I^{2}C SCL	
5	SCB/GPIO	SCB1_1/GPIO_9	TXD	UART TXD/I^{2}C SDA	
6	GPIO	GPIO_10	Tristate	GPIO	
7	GPIO	GPIO_11	POWER#	GPIO (CY7C65217)	
	GPIO	GPIO_11	Tristate	GPIO (CY7C65217A)	
8	Output	SUSPEND	–	On CY7C65217, this pin indicates that the device in Suspend mode. Can be configured as active LOW/HIGH using the configuration utility.	
	GPIO	GPIO_12	Tristate	GPIO	
9	Input	WAKEUP	–	On CY7C65217, this pin is configured to wake up the device from Suspend mode. Can be configured as active LOW/HIGH using the configuration utility.	
	GPIO	GPIO_13	Tristate	On CY7C65217A, this pin serves as GPIO.	
10	USBIO	USBDP	–	USB Data Signal Plus, integrates termination resistor and a 1.5-kΩ pull-up resistor	
11	USBIO	USBDM	–	USB Data Signal Minus, integrates termination resistor	
12	Power	VCCD	–	This pin should be decoupled to ground using a 1-µF capacitor or by connecting a 1.8-V supply	
13	Power	VSSD	–	Digital Ground	
14	nXRES	nXRES	–	Chip reset, active low. Can be left unconnected or have a pull-up resistor connected if not used	
15	Power	VBUS	–	VBUS Supply, 3.15 V to 5.25 V	
16	Power	VSSD	–	Digital Ground	
17	Power	VSSA	–	Analog Ground	
18	Input	Debug I/O	–	Used for debug purpose. Should be left floating.	
19	GPIO	GPIO_1	Input	Can be used as wakeup source to wakeup device from Suspend mode.	
20	GPIO	GPIO_2	Tristate	GPIO	
21	SCB/GPIO	SCB0_1/GPIO_3	SCL	SCB0 I^{2}C SCL	
22	SCB/GPIO	SCB0_2/GPIO_4	SDA	SCB0 I^{2}C SDA	
23	GPIO	GPIO_5	Tristate	GPIO	
24	Power	VDDD	–	Supply to the device core and Interface, 1.71 V to 5.5 V	



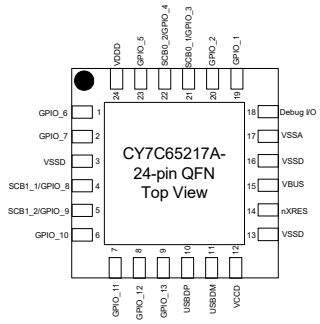


Table 1. GPIO Configuration

GPIO Configuration Option	Description
INPUT	Input GPIO
POWER#	This active low output signal is used to control power to an external logic through a switch to cut power off during an Unconfigured USB device and USB suspend. 0 - USB device in Configured state 1 - USB device in Unconfigured state or during USB suspend mode **Note:** CY7C65210A and CY7C65217A do not support POWER#.
TRISTATE	I/O Tristated (Open-Drain)
OUTPUT	Drive LOW or HIGH

Functional Overview

USB and Billboard Device Functionality

USB

CY7C6521x has a built-in USB 2.0 Full-Speed transceiver. The transceiver incorporates the internal USB series termination resistors on the USB data lines and a 1.5-kΩ pull-up resistor on USBDP.

Billboard Device Functionality

CY7C6521x is used to communicate Alternate Modes supported by a Device Container to a USB Host system. CY7C6521x sends this information through BOS descriptor and string descriptors in human-readable format. CY7C6521x supports the Billboard descriptor as part of the complete BOS descriptor. The CY7C65210/65217 supports USB Billboard Device class Rev. 1.1 while the CY7C65210A/65217A supports USB Billboard Device class Rev. 1.21. For further details on the device class, refer to the USB Billboard Device Class specification.

Serial Communication

CY7C65210 and CY7C65210A have one Serial Communication Block (SCB) whereas CY7C65217 and CY7C65217A have two SCBs that implement either UART or I^2C interface.

I^2C Interface

The I^2C interface implements full multi-master mode and supports up to 400 kHz. For further details on the protocol, refer to the NXP I^2C specification, Rev. 5.

Notes

- I^2C ports are not tolerant to higher voltages. Therefore, they cannot be hot-swapped or powered up independently when chip is not powered.
- The minimum fall time of the SCL is met (as per NXP I^2C specification Rev5) when V_{DDD} is between 1.71 V and 3.0 V. When V_{DDD} is within the range of 3.0 V to 3.6 V, it is recommended to add a 50 pF capacitor on the SCL signal.

UART Interface

Only the SCB1 interface of CY7C65217 and CY7C65217A can be configured as a UART interface.

The 2-pin UART interface (RXD and TXD) provides asynchronous serial communication with other UART devices operating at speeds of up to 115200. It supports seven or eight data bits, one or two stop bits, odd, even, mark, space, and no parity. The UART interface supports full-duplex communication with a signaling format that is compatible with the standard UART protocol. The UART pins may be interfaced to industry-standard RS-232/RS-422 transceivers to manage different voltage levels. Common UART functions, such as parity error[3] and frame error[4], are supported. The UART parameters can be set using native APIs.

GPIO Interface

CY7C65210 has nine configurable GPIOs whereas CY7C65217 has 7 configurable GPIOs. CY7C65210A has 11 configurable GPIOs whereas CY7C65217A has nine configurable GPIOs.

The configurable options are as follows:

- INPUT: Input GPIO
- POWER#: Power control
- TRISTATE: I/O tristated
- OUTPUT: Drive LOW or HIGH

Memory

CY7C6521x has a 2560-bytes configurable flash. Flash is used to store USB parameters such as VID/PID, serial number, product and manufacturer descriptors, and Billboard Device Class-specific descriptors.

System Resources

Power System

CY7C6521x supports USB Suspend mode to control power usage. CY7C6521x operates in bus-powered or self-powered modes over a range of 3.15 V to 5.5 V.

Clock System

CY7C6521x has a fully integrated clock with no external components required. The clock system is responsible for providing clocks to all subsystems.

Internal 48-MHz Oscillator

The internal 48-MHz oscillator is the primary source of internal clocking in CY7C6521x.

Internal 32-kHz Oscillator

The internal 32-kHz oscillator is primarily used to generate clocks for peripheral operation in USB Suspend mode.

Reset

The reset block provides reliable power-on reset and brings the device back to the default known state. The nXRES (active LOW) pin can be used by the external devices to reset CY7C6521x.

Suspend and Resume

The CY7C65210 and CY7C65217 device asserts the SUSPEND pin when the USB bus enters the suspend state. This helps in meeting the stringent suspend current requirement of the USB 2.0 specification, while using the device in bus-powered mode. The device resumes from the suspend state under either of the two following conditions:

1. Any activity is detected on the USB bus.
2. The WAKEUP pin is asserted to generate remote wakeup to the host.

Note

3. Parity error gets detected when UART transmitter device is configured for odd parity and UART receiver device is configured for even parity.
4. Frame error gets detected when UART transmitter device is configured for 7 bits data width and 1 stop bit, whereas UART receiver device is configured for 8 bit data width and 2 stop bits.

WAKEUP

The WAKEUP pin on CY7C65210 and CY7C65217 is used to generate the remote wakeup signal on the USB bus. The remote wakeup signal is sent only if the host enables this feature through the SET_FEATURE request. The device communicates support for the remote wakeup to the host through the configuration descriptor during the USB enumeration process.

Internal Flash Configuration

The internal flash memory can be used to store the configuration parameters provided in Table 2.

Table 2. Internal Flash Configuration for CY7C65210 and CY7C65210A

Parameter	Default Value	Description
USB Configuration		
USB Vendor ID (VID)	0x04B4	Default Cypress VID. Can be configured to customer VID.
USB Product ID (PID)	0x5210	Default Cypress PID. Can be configured to customer PID.
Manufacturer string	Cypress Semiconductor	Can be configured with any string up-to 126 characters[5].
Product string	Billboard Device	Can be configured with any string up-to 126 characters[5].
Serial string	User-defined	Can be configured with any string up-to 126 characters[5]. If the Serial string is not configured by the user, a unique serial number will be generated using the wafer die parameters.
Power mode	Bus powered	Can be configured to bus-powered or self-powered mode.
Max current draw	100 mA	Can be configured to any value from 0 to 500 mA. The configuration descriptor will be updated based on this.
Remote wakeup	Enabled	Can be disabled on CY7C65210. Remote wakeup is initiated by asserting the WAKEUP or GPIO_1 pin.
	Disabled	On CY7C65210A, this feature is removed.
bcdDevice	0x00	Can be configured with specific binary coded decimal number.
GPIO Configuration		
GPIO_1	Input	GPIO can be configured as shown in Table 1 on page 5.
GPIO_2	Tristate	
GPIO_3	I^2C SCL	
GPIO_4	I^2C SDA	
GPIO_5	Tristate	
GPIO_6	Tristate	
GPIO_7	Tristate	
GPIO_8	Tristate	
GPIO_9	Tristate	
GPIO_10	Tristate	
GPIO_11	Power#(CY7C65210)	
	Tristate(CY7C65210A)	
GPIO_12	Tristate[6]	
GPIO_13	Tristate[6]	
Billboard Device Class Descriptor Configuration		
iAdditionalInfoURL	www.cypress.com/Type-C	Can be configured with any string up-to 126 characters[5].
bNumberOfAlternateModes	0x01	Can be configured with any value from 0x01 to 0x08.
bPreferredAlternateMode	0x00	Can be configured with any value from 0x00 to 0x07.

Note
5. Maximum available configuration space for all string descriptors is 1920 bytes. Each string descriptor can be configured up to 126 characters.
6. These GPIOs are available only on CY7C65210A.

Table 2. Internal Flash Configuration for CY7C65210 and CY7C65210A *(continued)*

Parameter	Default Value	Description
VCONN Power	0x0000	Can be configured with any value from 0x0000 to 0x0006 or it can be configured with value 0x8000.
SVID	0xFF01	Can be configured to specific SVID.
bAlternateMode	0x01	Can be configured with any value from 0x01 to 0x08.
iAlternateModeString	Type-C to Display adapter. For further assistance, see http://help.vesa.org/dp-usb-type-c	Can be configured with any string up-to 126 characters[5].
dwAlternateModeVdo	0x000C00C5	Can be configured with any 4-byte value (applicable only for CY7C65210A and CY7C65217A).

Note
5. Maximum available configuration space for all string descriptors is 1920 bytes. Each string descriptor can be configured up to 126 characters.
6. These GPIOs are available only on CY7C65210A.

Table 3. Internal Flash Configuration for CY7C65217 and CY7C65217A

Parameter	Default Value	Description
USB Configuration		
USB Vendor ID (VID)	0x04B4	Default Cypress VID. Can be configured to customer VID.
USB Product ID (PID)	0x5217	Default Cypress PID. Can be configured to customer PID.
Manufacturer string	Cypress Semiconductor	Can be configured with any string up-to 126 characters[7].
Product string	Billboard Device	Can be configured with any string up-to 126 characters[7].
Serial string	User-defined	Can be configured with any string up-to 126 characters[7]. If the Serial string is not configured by the user then a unique serial number will be generated using the wafer die parameters.
Power mode	Bus powered	Can be configured to bus-powered or self-powered mode.
Max current draw	100 mA	Can be configured to any value from 0 to 500 mA. The configuration descriptor will be updated based on this.
Remote wakeup	Enabled	Can be disabled on CY7C65217. Remote wakeup is initiated by asserting the WAKEUP or GPIO_1 pin.
	Disabled	On CY7C65217A, this feature is removed.
bcdDevice	0x00	Can be configured with specific binary coded decimal number.
GPIO Configuration		
GPIO_1	Input	GPIO can be configured as shown in Table 1 on page 5.
GPIO_2	Tristate	
GPIO_3	SCB0 I^2C SCL	
GPIO_4	SCB0 I^2C SDA	
GPIO_5	Tristate	
GPIO_6	Tristate	
GPIO_7	Tristate	
GPIO_8	SCB1 UART RXD	
GPIO_9	SCB1 UART TXD	
GPIO_10	Tristate	
GPIO_11	Power#(CY7C65217)	
	Tristate(CY7C65217A)	
GPIO_12	Tristate[8]	
GPIO_13	Tristate[8]	
Billboard Device Class Descriptor Configuration		
iAdditionalInfoURL	www.cypress.com/Type-C	Can be configured with any string up-to 126 characters[7].
bNumberOfAlternateModes	0x01	Can be configured with any value from 0x01 to 0x08.
bPreferredAlternateMode	0x00	Can be configured with any value from 0x00 to 0x07.
VCONN Power	0x0000	Can be configured with any value from 0x0000 to 0x0006 or it can be configured with value 0x8000.
SVID	0xFF01	Can be configured to specific SVID.
bAlternateMode	0x01	Can be configured with any value from 0x01 to 0x08.
iAlternateModeString	Type-C to Display adapter. For further assistance, see http://help.vesa.org/dp-usb-type-c	Can be configured with any string up-to 126 characters[7].
dwAlternateModeVdo	0x000C00C5	Can be configured with any 4-byte value (applicable only for CY7C65210A and CY7C65217A).

Note
7. Maximum available configuration space for all string descriptors is 1920 bytes. Each string descriptor can be configured up to 126 characters.
8. These GPIOs are available only on CY7C65217A.

Electrical Specifications

Absolute Maximum Ratings

Exceeding maximum ratings[9] may shorten the useful life of the device.

Storage temperature ..... –55 °C to +100 °C

Ambient temperature with power supplied (Industrial) ..... –40 °C to +85 °C

Supply voltage to ground potential
V_{DDD} ..... 6.0 V
V_{BUS} ..... 6.0 V
V_{CCD} ..... 1.95 V
V_{GPIO} ..... V_{DDD} + 0.5 V

Static discharge voltage ESD protection levels:

■ 2.2-kV HBM per JESD22-A114

Latch-up current ..... 140 mA

Current per GPIO ..... 25 mA

Operating Conditions

T_A (ambient temperature under bias)
Commercial ..... 0 °C to 70 °C
Industrial ..... –40 °C to +85 °C

V_{BUS} supply voltage ..... 3.15 V to 5.50 V

V_{DDD} supply voltage ..... 1.71 V to 5.50 V

V_{CCD} supply voltage ..... 1.71 V to 1.89 V

Device-Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C, T_J ≤ 100 °C, and 1.71 V to 5.50 V, except where noted.

Table 4. DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{BUS}	V_{BUS} supply voltage	3.15	3.30	3.45	V	Set and configure the correct voltage range using a configuration utility for V_{BUS}. Default 5 V.
		4.35	5.00	5.5	V	
V_{DDD}	V_{DDD} supply voltage	1.71	1.80	1.89	V	Used to set I/O and core voltage. Set and configure the correct voltage range using a configuration utility for V_{DDD}. Default 3.3 V.
		2.0	3.3	5.5	V	
V_{CCD}	Output voltage (for core logic)	–	1.80	–	V	Do not use this supply to drive the external device. • 1.71 V ≤ V_{DDD} ≤ 1.89 V: Short the V_{CCD} pin with the V_{DDD} pin • V_{DDD} > 2 V – Connect a 1-µF capacitor (Cefc) between the V_{CCD} pin and ground
Cefc	External regulator voltage bypass	1.00	1.30	1.60	µF	X5R ceramic or better.
I_{DD1}	Operating supply current	–	20	–	mA	USB 2.0 FS, UART at 1-Mbps single channel, no GPIO switching.
I_{DD2}	USB Suspend supply current	–	5	–	µA	Does not include current through a pull-up resistor on USBDP.

Note
9. Usage above the Absolute Maximum conditions may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 5. AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Fall Time_FS	FS USB Fall Time	–	7.815	–	ns	90% to 10% of full swing, 50-pF load
Rise Time_FS	FS USB Rise Time	–	8.367	–	ns	10% to 90% of full swing, 50-pF load
TRFM_FS	FS Rise/Fall Matching	–	107.024	–	%	–
VCRS_FS	FS Crossover Voltage	–	1.797	–	V	–
TDJ1	FS Driver Jitter (next)	–	–0.339	–	ns	–
TDJ2	FS Driver Jitter (paired)	–	–0.285	–	ns	–
TFDEOP	FS Differential to EOP Skew	–	–0.076	–	ns	–
F1	Frequency	47.04	48	48.96	MHz	Non-USB mode
F2		47.88	48	48.12	MHz	USB mode
Zout	USB driver output impedance	28	–	44	Ω	–
Twakeup	Wakeup from USB Suspend mode	–	25	–	µs	–

GPIO

Table 6. GPIO DC Specification

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}[10]	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
V_{IH}[10]	LVTTL input, V_{DDD}< 2.7 V	0.7 × V_{DDD}	–	–	V	–
V_{IL}	LVTTL input, V_{DDD} < 2.7V	–	–	0.3 × V_{DDD}	V	–
V_{IH}[10]	LVTTL input, V_{DDD} ≥ 2.7V	2	–	–	V	–
V_{IL}	LVTTL input, V_{DDD} ≥ 2.7V	–	–	0.8	V	–
V_{OH}	CMOS output voltage HIGH level	V_{DDD} – 0.4	–	–	V	I_{OH} = 4 mA, V_{DDD} = 5 V +/- 10%
V_{OH}	CMOS output voltage HIGH level	V_{DDD} – 0.6	–	–	V	I_{OH} = 4 mA, V_{DDD} = 3.3 V +/- 10%
V_{OH}	CMOS output voltage HIGH level	V_{DDD} – 0.5	–	–	V	I_{OH} = 1 mA, V_{DDD} = 1.8 V +/- 5%
V_{OL}	CMOS output voltage LOW level	–	–	0.4	V	I_{OL} = 8 mA, V_{DDD} = 5 V +/- 10%
V_{OL}	CMOS output voltage LOW level	–	–	0.6	V	I_{OL} = 8 mA, V_{DDD} = 3.3 V +/- 10%
V_{OL}	CMOS output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA, V_{DDD} = 1.8 V +/- 5%
Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	–
Rpulldown	Pull-down resistor	3.5	5.6	8.5	kΩ	–
I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0 V
C_{IN}	Input capacitance	–	–	7	pF	–
Vhysttl	Input hysteresis LVTTL; V_{DDD} > 2.7 V	25	40	C	mV	–
Vhyscmos	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	–

Note
10. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 7. GPIO AC Specification

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{RiseFast1}$	Rise Time in Fast mode	2	–	12	ns	V_{DDD} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{FallFast1}$	Fall Time in Fast mode	2	–	12	ns	V_{DDD} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{RiseSlow1}$	Rise Time in Slow mode	10	–	60	ns	V_{DDD} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{FallSlow1}$	Fall Time in Slow mode	10	–	60	ns	V_{DDD} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{RiseFast2}$	Rise Time in Fast mode	2	–	20	ns	V_{DDD} = 1.8 V, Cload = 25 pF
$T_{FallFast2}$	Fall Time in Fast mode	20	–	100	ns	V_{DDD} = 1.8 V, Cload = 25 pF
$T_{RiseSlow2}$	Rise Time in Slow mode	2	–	20	ns	V_{DDD} = 1.8 V, Cload = 25 pF
$T_{FallSlow2}$	Fall Time in Slow mode	20	–	100	ns	V_{DDD} = 1.8 V, Cload = 25 pF

nXRES

Table 8. nXRES DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	–
V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	–
Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	–
C_{IN}	Input capacitance	–	5	–	pF	–
Vhysxres	Input voltage hysteresis	–	100	–	mV	–

Table 9. nXRES AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Tresetwidth	Reset pulse width	1	–	–	µs	–

Table 10. UART AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{UART}	UART bit rate	0.3	–	3000	kbps	Single SCB: TX + RX Dual SCB: TX or RX

I²C Specifications

Table 11. I²C AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{I2C}	I²C frequency	1	–	400	KHz	–

Flash Memory Specifications

Table 12. Flash Memory Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Fend	Flash endurance	100K	–	–	cycles	–
Fret	Flash retention. $T_A \leq 85$ °C, 10 K program/erase cycles	10	–	–	years	–

Application Schematic

Figure 1 shows the application schematic for CY7C65210. Refer to the CY7C65210 and CY7C65210A Pin Description on page 4 for signal details.

Figure 1. CY7C65210 Application Schematic

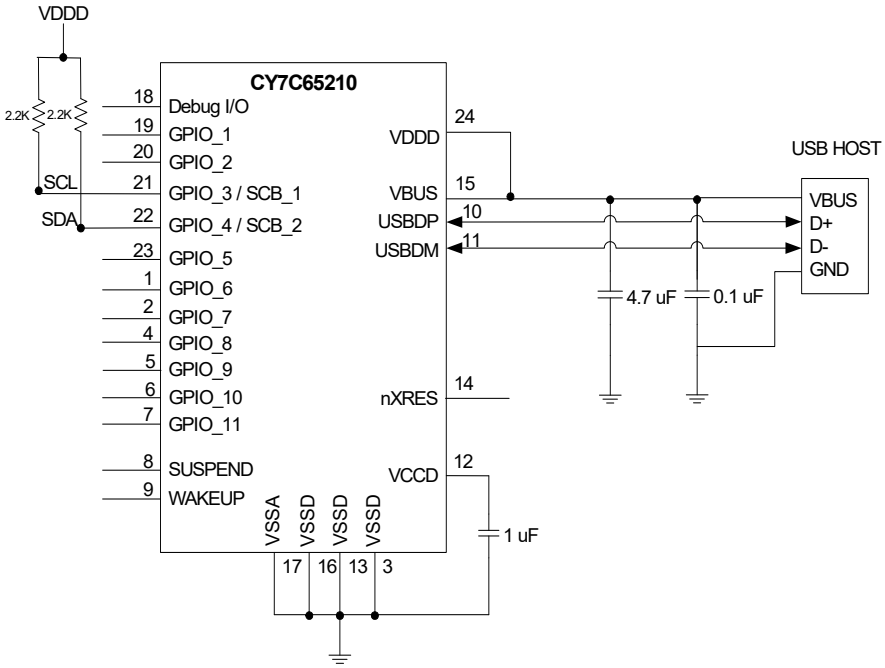


Figure 2 shows the application schematic for CY7C65210A. Refer to the CY7C65210 and CY7C65210A Pin Description on page 4 for signal details.

Figure 2. CY7C65210A Application Schematic

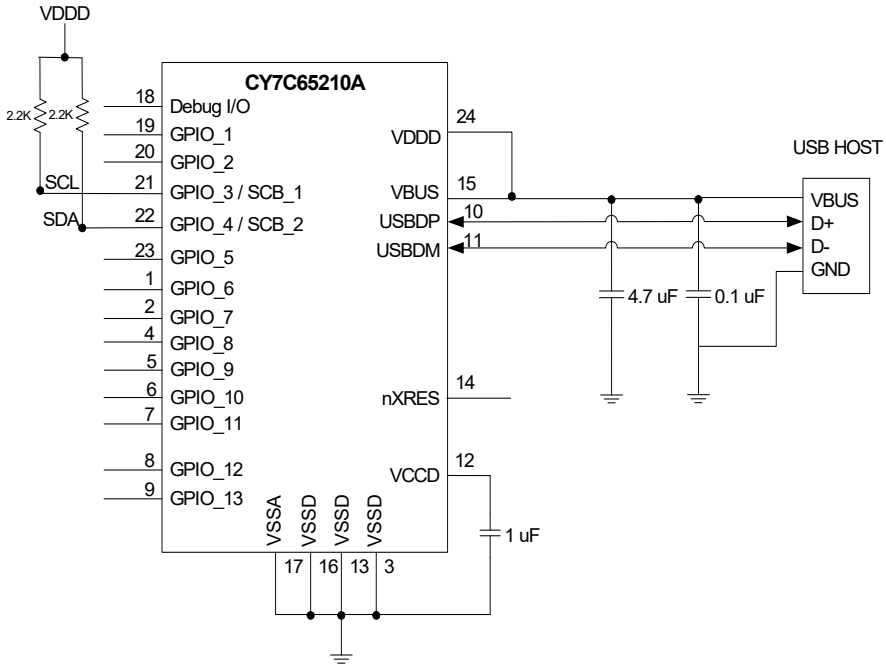


Figure 3 shows the application schematic for CY7C65217. Refer to the CY7C65217 and CY7C65217A Pin Description on page 5 for signal details.

Figure 3. CY7C65217 Application Schematic

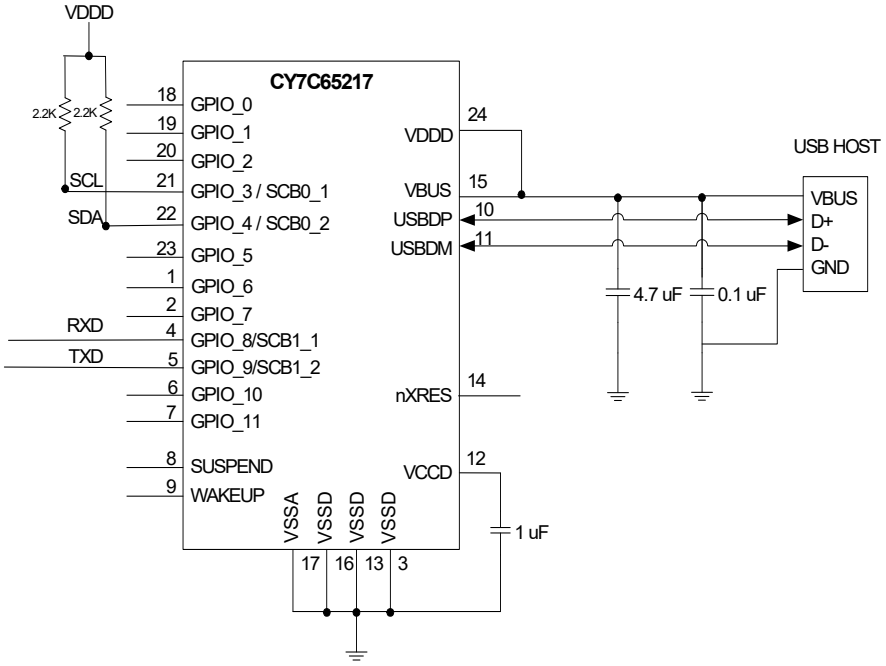
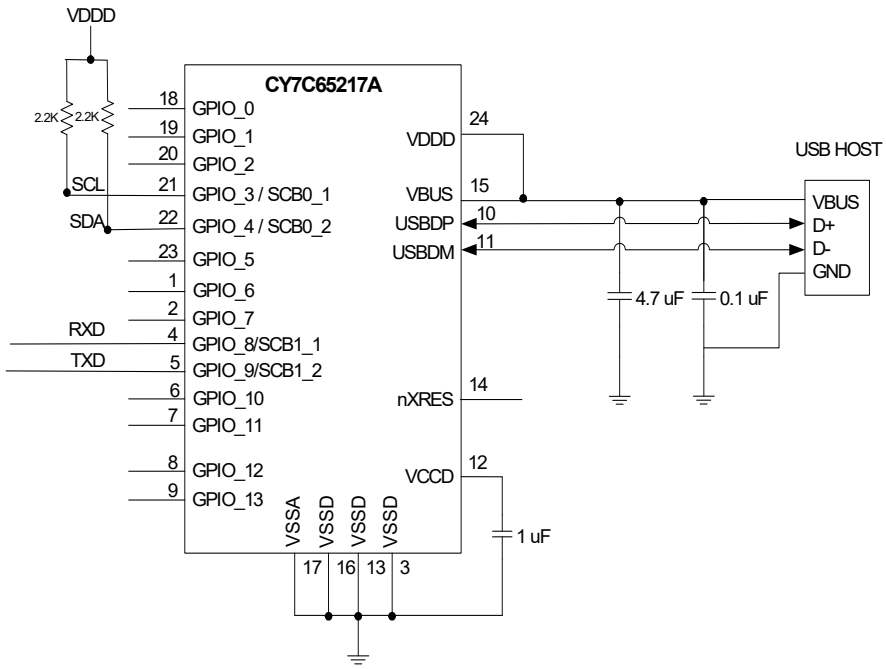


Figure 4 shows the application schematic for CY7C65217A. Refer to the CY7C65217 and CY7C65217A Pin Description on page 5 for signal details.

Figure 4. CY7C65217A Application Schematic



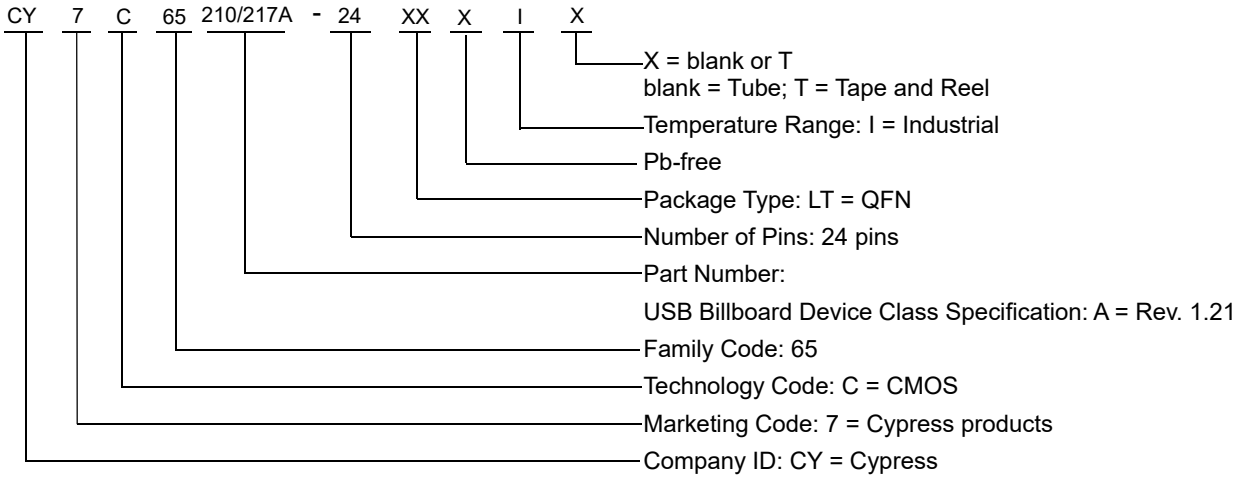
Ordering Information

Table 13 lists the key package features and ordering codes of CY7C65210, CY7C65217, CY7C65210A, and CY7C65217A. For more information, contact your local sales representative.

Table 13. Key Features and Ordering Information

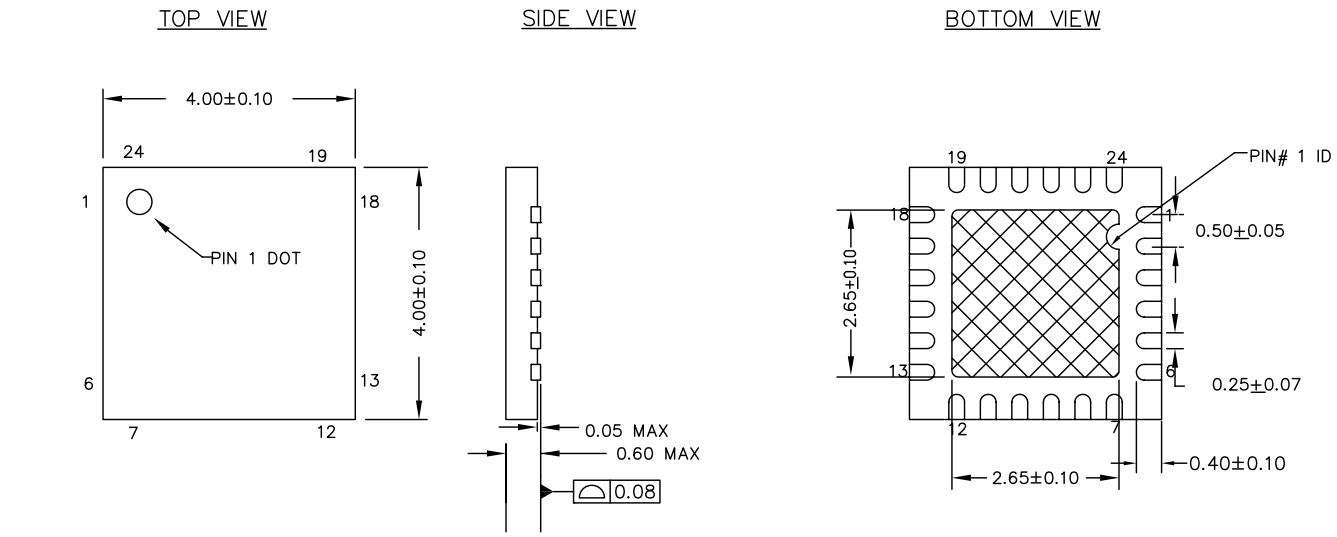
Part Number	Package	Temperature Range
CY7C65210-24LTXI	24-pin QFN (4.00 × 4.00 × 0.55 mm, 0.5 mm pitch) (Pb-free)	Industrial
CY7C65210-24LTXIT	24-pin QFN (4.00 × 4.00 × 0.55 mm, 0.5 mm pitch) (Pb-free) – Tape and Reel	Industrial
CY7C65210A-24LTXI	24-pin QFN (4.00 × 4.00 × 0.55 mm, 0.5 mm pitch) (Pb-free)	Industrial
CY7C65210A-24LTXIT	24-pin QFN (4.00 × 4.00 × 0.55 mm, 0.5 mm pitch) (Pb-free) – Tape and Reel	Industrial
CY7C65217-24LTXI	24-pin QFN (4.00 × 4.00 × 0.55 mm, 0.5 mm pitch) (Pb-free)	Industrial
CY7C65217-24LTXIT	24-pin QFN (4.00 × 4.00 × 0.55 mm, 0.5 mm pitch) (Pb-free) – Tape and Reel	Industrial
CY7C65217A-24LTXI	24-pin QFN (4.00 × 4.00 × 0.55 mm, 0.5 mm pitch) (Pb-free)	Industrial
CY7C65217A-24LTXIT	24-pin QFN (4.00 × 4.00 × 0.55 mm, 0.5 mm pitch) (Pb-free)	Industrial

Ordering Code Definitions



Package Information

Figure 5. 24-pin QFN 4 mm × 4 mm × 0.55 mm LQ24A 2.65 × 2.65 EPAD (Sawn)



NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

Table 14. Package Characteristics

Parameter	Description	Min	Typ	Max	Units
T_A	Operating ambient temperature	–40	25	85	°C
THJ	Package θ_{JA}	–	18.4	–	°C/W

Table 15. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
24-pin QFN	260 °C	30 seconds

Table 16. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
24-pin QFN	MSL 3

Acronyms

Table 17. Acronyms Used in this Document

Acronym	Description
BOS	binary device object store
ESD	electrostatic discharge
GPIO	general purpose input/output
HBM	human-body model
I^2C	inter-integrated circuit
MCU	microcontroller unit
OSC	oscillator
PID	product identification
SCB	serial communication block
SCL	I^2C serial clock
SDA	I^2C serial data
SIE	serial interface engine
SVID	standard or vendor ID
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VID	vendor identification

Document Conventions

Units of Measure

Table 18. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
DMIPS	Dhrystone million instructions per second
kΩ	kilo-ohm
KB	kilobyte
kHz	kilohertz
kV	kilovolt
Mbps	megabits per second
MHz	megahertz
mm	millimeter
V	volt

Document History Page

Document Title: CY7C65210, CY7C65217, CY7C65210A, CY7C65217A USB Billboard Controller Document Number: 001-97082				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4715309	MVTA	04/10/2015	New datasheet.
*A	4839996	MVTA	07/22/2015	Updated Features, CY7C65210 and CY7C65210A Pin Description, GPIO Interface, and Memory. Updated Table 2. Updated Figure 5 (spec 001-13937 *E to *F) in Package Information.
*B	4881560	MVTA	08/13/2015	Added a note in Functional Description. Added Block Diagram – CY7C65217, CY7C65217A. Added CY7C65217 and CY7C65217A Pin Description. Added UART Interface. Added Figure 3 and Table 3. Updated Features, Serial Communication, GPIO Interface, Ordering Information. Updated Table 2 and Table 17. Updated CY7C65210 references to CY7C6521x.
*C	5310895	MVTA	06/16/2016	Removed support for Windows and Linux drivers in Features. Updated CY7C65217 and CY7C65217A Pin Description. Updated GPIO Configuration and Functional Overview. Updated GPIO_8 and GPIO_9 in Internal Flash Configuration for CY7C65217 and CY7C65217A. Added UART AC Specifications. Updated CY7C65217 Application Schematic.
*D	5768506	AESATMP8	06/09/2017	Updated logo and Copyright.
*E	5920593	UMSH	10/13/2017	Updated datasheet for new part numbers. Updated USB and Billboard Device Functionality, CY7C65210 and CY7C65210A Pin Description, CY7C65217 and CY7C65217A Pin Description, and Ordering Information. Added Figure 2 and Figure 4. Updated Table 1 through Table 3.

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