CMOS 8–Bit Microcontrollers

TMP90CH02P/TMP90CH02M

TMP90CH03P/TMP90CH03M

1. Outline and Characteristics

The TMP90CH02 is a high-speed advanced 8-bit microcontroller applicable to a variety of equipment.

With its 8-bit CPU, ROM, RAM, timer/event counter and general-purpose serial interface integrated into a single CMOS chip, the TMP90CH02 allows the expansion of external memories for programs (up to 48K byte). The TMP90CH03 is the same as the TMP90CH02 bit without the ROM.

The TMP90CH02P/H03P is in a DIP ppackage.

The TMP90CH02M/H03M is in a SOP (Small Outline Package).

The characteristics of the TMP90CH02 include:

(1) Powerful instructions: 163 basic instructions, including Multiplication, division, 16-bit arithmetic operations, bit manipulation instructions

(2) Minimum instruction executing time: 250ns (at 16MHz oscillation frequency)

(3) Internal ROM: 16K byte (the TMP90CH03 does not have a built in ROM)

(4) Internal RAM: 512 byte

(5) Memory expansion
External memory: 48K byte

(6) General-purpose serial interface (1 channel)
Asynchronous mode, I/O interface mode

(7) 8-bit timers (4 channels): (1 external clock input)

(8) Port with zero cross detection circuit (1 input)

(9) Input/Output ports (90CH02: 32 pins, 90CH03: 6 pins)

(10) Interrupt function: 8 internal interrupts and 3 external interrupts

(11) Micro Direct Memory Access (DMA) function (4 channels)

(12) Watchdog timer

(13) Standby function (4 HALT modes)

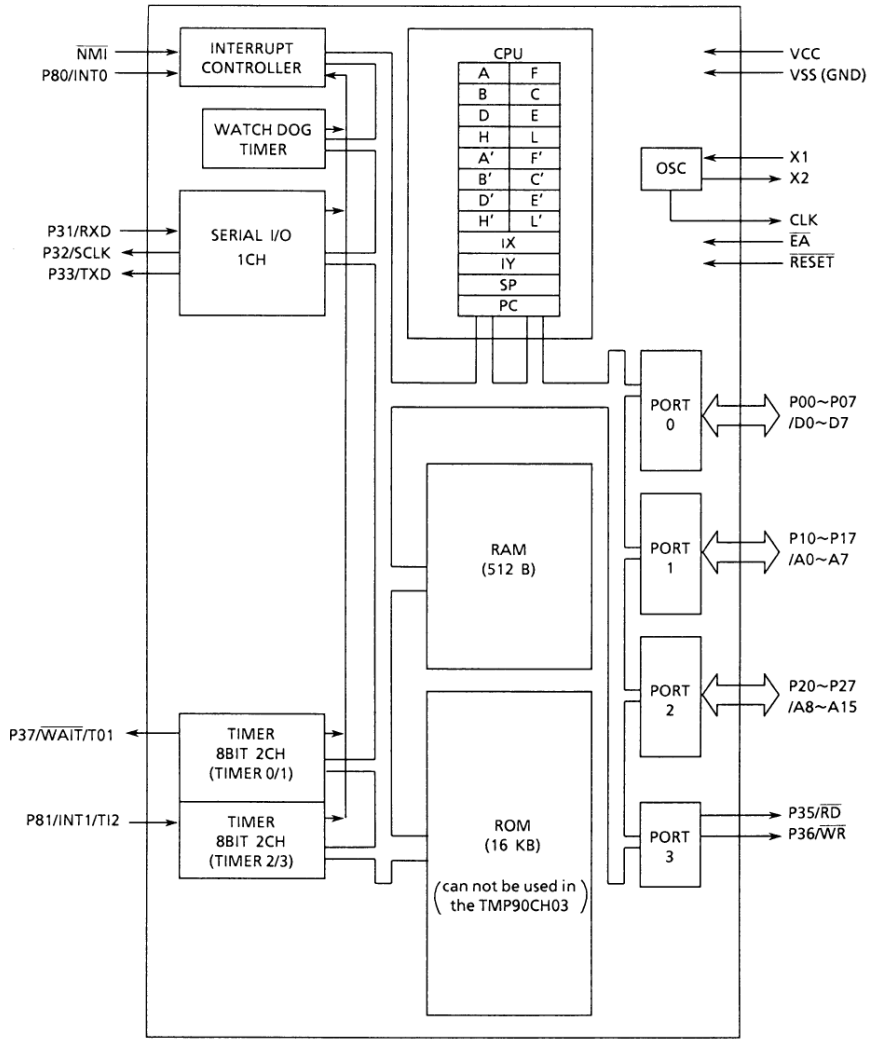


Figure 1. TMP90CH02 Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1 (1) shows pin assignment of the TMP90CH02/CH03.

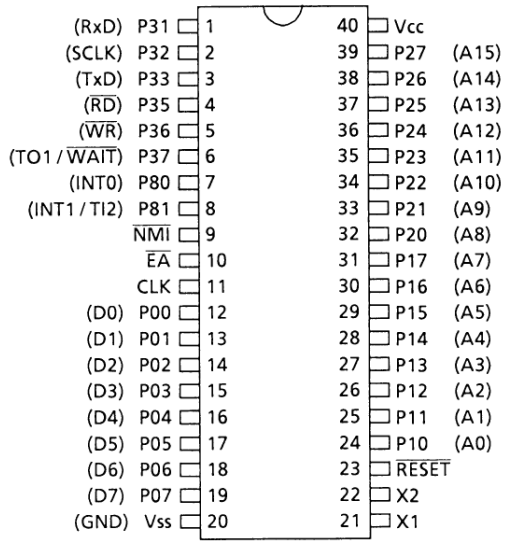


Figure 2.1 (1). Pin Assignment (Shrink Dual Inline Package)

2.2 Pin Names and Functions

The names of input/output pins and their functions are summarized in Table 2.2.

Table 2.2 Pin Names and Functions (1/1)

Pin Name	No. of Pins	I/O 3 states	Function
P00 ~ P07 /D0 ~ D7	8	I/O	Port 0: 8-bit I/O port that allows selection of input/output on byte basis
		3 states	Data Bus: Also functions as 8-bit bidirectional data bus for external memory (For CH03, fixed to databus)
P10 ~ P17 /A0 ~ A7	8	I/O	Port 1: 8-bit I/O port that allows selection on byte basis
		Output	Addrress Bus: The lower 8 bits address bus for external memory (For CH03, fixed to address bus)
P20 ~ P27 /A8 ~ A 15	8	I/O	Port 2: 8-bit I/O port that allows selection on byte basis
		Output	Addrress Bus: The uppper 8 bits address bus for external memory (For CH03, fixed to address bus)
P31 /RxD	1	Input	Port 31: 1-bit input port
			Receives serial data
P32 /TxD /$\overline{\text{RTS}}$ /SCLK	1	Output	Port 32: 1-bit output port
			Serial clock output
P33 /TxD	1	Output	Port 33: 1-bit output port
			Transmits serial data
P35 /$\overline{\text{RD}}$	1	Output	Port 35: 1-bit output port
			Read: Generates strobe signal for reading external memory
P36 /$\overline{\text{WR}}$	1	Output	Port 36: 1-bit output port
			Writes: Generates strobe signal for writing external memory
P37 /$\overline{\text{WAIT}}$	1	Input	Port 37: 1-bit input port
			Wait: Input pin for connecting slow speed memory or peripheral LSI
P80 /INTO	1	Input	Port 80: 1-bit input port
			Interrupt request pin 0: Interrupt request pin (Level/rising edge is programmable) 
P81 /INT1 /TI4	1	Input	Port 81: 1-bit input port
			Interrupt request pin 1: Interrupt request pin (Rising/falling edge is programmable) 
			Timer input 4: Counter/capture trigger signal for Timer 4
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Falling edge interrupt request pin 
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is Pulled up internally during resetting.
$\overline{\text{EA}}$	1	Input	External access: Connects with GND pin in the TMP90C802A using internal ROM, and with GND pin in the TMP90C803A with no internal ROM.
$\overline{\text{RESET}}$	1	Input	Reset: Initializes the TMP 90CH02/CH03. (Built-in pull-up resistor)
X1/X2	2	Input/ Output	Pin for quartz crystal or ceramic resonator (1 ~ 16MHz)
V_{CC}	1	–	Power supply (+5V)
V_{SS} (GND)	1	–	Ground (0V)

3. Operation

The following explains the TMP90CH02 functions and basic operations. The CPU functions and internal I/O functions of the TMP90CH02 are the same as the TMP90C840A.

Refer to the “TMP90C840A” section concerning functions which are not explained the following.

3.1 CPU

The TMP90CH02 has an internal high-performance 8-bit CPU.

Refer to the book TLCS Series CPU Core Architecture concerning CPU operation.

3.2 Memory Map

The TMP90CH02 supports a program memory of up to 64K bytes.

The program memory may be assigned to the address space from 00000H to 0FFFFH, while the data memory can be allocated to any address from 0000H to FFFFH.

(1) Internal ROM

The TMP90CH02 internally contains a 16K byte ROM. The address space from 0000H to 3FFFH is provided to the ROM. The CPU starts executing a program from 0000H by resetting.

The addresses from 0010H to 007FH in this internal ROM area are used for the entry area for the interrupt processing.

The TMP90CH03 does not have a built-in ROM; therefore, the address space 0000H ~ 3 FFFH is used as external memory space.

(2) Internal RAM

The TMP90CH02 also contains a 512-byte RAM, which is allocated to the address space FDC0H ~ FFBFH. The CPU allows the access to whole RAM area (FF00H ~ FFBFH, 192 bytes) by a short operation code (opcode) in the “direct addressing mode”.

The addresses from FF30H ~ FF7FH in this RAM area can be used as parameter area for micro DMA processing (and for any other purposes when the micro DMA function is not used).

(3) Internal I/O

The TMP90CH02 provides a 48-byte address space as an internal I/O area, whose addressess range from FFC0H to FFEFH. This I/O area can be accessed by the CPU using a short opcode in the “direct addressing mode”.

Figure 3.2 is a memory map indicating the areas accessible by the CPU in the respective addressing mode.

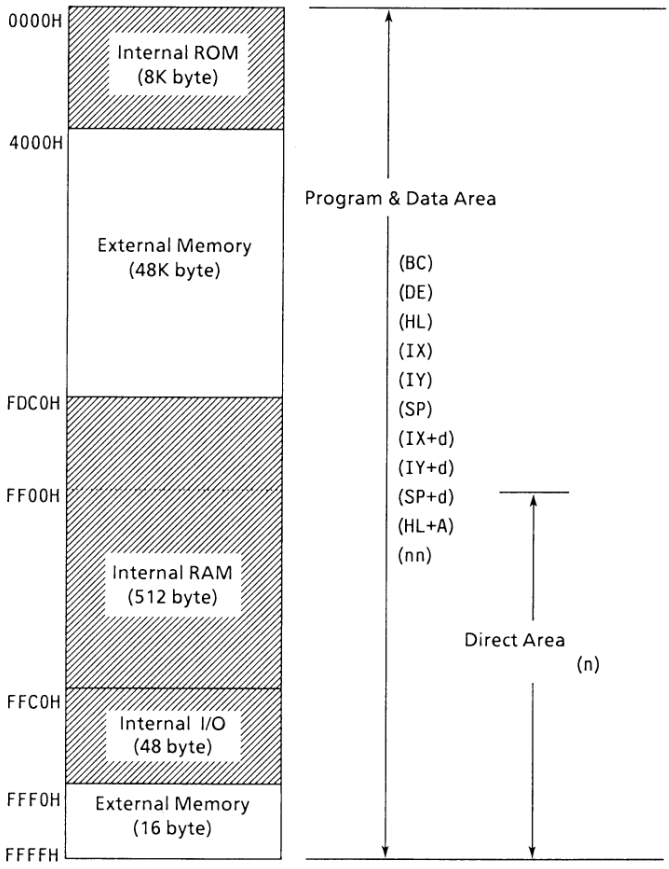


Figure 3.2. Memory Map

4. Electrical Characteristics

TMP90CH02N/TMP90CH02F

4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage	-0.5 ~ + 6.5	V
V_{IN}	Input voltage	-0.5 ~ V_{CC} + 0.5	V
P_D	Power dissipation (Ta = 70°C)	F 500	mW
		N 600	
T_{SOLDER}	Soldering temperature (10s)	260	°C
T_{STG}	Storage temperature	-65 ~ 150	°C
T_{OPR}	Operating temperature	-20 ~ 70	°C

4.2 DC Characteristics

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 16MHz)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (P0)	-0.3	0.8	V	–
V_{IL1}	P1, P2, P3, P8	-0.3	$0.3V_{CC}$	V	–
V_{IL2}	$\overline{RESET}$, INT0, $\overline{NMI}$	-0.3	$0.25V_{CC}$	V	–
V_{IL3}	$\overline{EA}$	-0.3	0.3	V	–
V_{IL4}	X1	-0.3	$0.2V_{CC}$	V	–
V_{IH}	Input Low Voltage (D0 ~ D7)	2.2	V_{CC} + 0.3	V	–
V_{IH1}	P3, P5, P6, P7, P8	$0.7V_{CC}$	V_{CC} + 0.3	V	–
V_{IH2}	$\overline{RESET}$, INT0, $\overline{NMI}$	$0.75V_{CC}$	V_{CC} + 0.3	V	–
V_{IH4}	X1	$0.8V_{CC}$	V_{CC} + 0.3	V	–
V_{OL}	Output Low Voltage	–	0.45	V	I_{OL} = 1.6mA
V_{OH} V_{OH1} V_{OH2}	Output High Voltage	2.4 $0.75V_{CC}$ $0.9V_{CC}$	–	V V V	I_{OH} = -400μA I_{OH} = -100μA I_{OH} = -20μA
I_{DAR}	Darlington Drive Current (8 I/O pins)	-1.0	-3.5	mA	V_{EXT} = 1.5V R_{EXT} = 1.1kΩ
I_{LI}	Input Leakage Current	0.02 (Typ)	±5	μA	0.0 ≤ Vin ≤ V_{CC}
I_{LO}	Output Leakage Current	0.05 (Typ)	±10	μA	0.2 ≤ Vin ≤ V_{CC} - 0.2
I_{CC}	Operating Current (RUN) Idle 1 Idle 2	17 (Typ) 1.5 (Typ) 6 (Typ)	30 5 15	mA mA mA	tosc = 10MHz (60% Up @ 16MHz)
	STOP (TA = -20 ~ 70°C) STOP (TA = 0 ~ 50°C)	0.2 (Typ)	50 10	μA μA	0.2 ≤ Vin ≤ V_{CC} - 0.2
V_{STOP}	Power Down Voltage (@STOP)	2 RAM BACK UP	150	KΩ	V_{IL2} = $0.2V_{CC}$, V_{IH2} = $0.8V_{CC}$
R_{RST}	$\overline{RESET}$ Pull Up Register	50	150	KΩ	–
CIO	Pin Capacitance	–	10	pF	testfreq = 1MHz
V_{TH}	Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0	0.4	1.0 (Typ)	V	–

Note: I_{DAR} is guaranteed for a total of up to 8 optional ports.

4.3 AC Characteristics

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
CL = 50pF TA = -20 ~ 70°C (1 ~ 16MHz)

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{OSC}	OSC. Period = x	62.5	1000	80	–	62.5	–	ns
t_{CYC}	CLK Period	4x	4x	320	–	250	–	ns
t_{WL}	CLK Low width	2x - 40	–	120	–	85	–	ns
t_{WH}	CLK High width	2x - 40	–	120	–	85	–	ns
t_{AC}	Address Setup to $\overline{RD}$, $\overline{WR}$	x - 45	–	35	–	18	–	ns
t_{RR}	$\overline{RD}$ Low width	2.5x - 40	–	160	–	117	–	ns
t_{CA}	Address Hold Time After $\overline{RD}$, $\overline{WR}$	0.5x - 20	–	20	–	12	–	ns
t_{AD}	Address to Valid Data In	–	3.5x - 95	–	185	–	123	ns
t_{RD}	$\overline{RD}$ to Valid Data In	–	2.5x - 80	–	120	–	76	ns
t_{HR}	Input Data Hold After $\overline{RD}$	0	–	0	–	0	–	ns
t_{WW}	$\overline{WR}$ Low width	2.5x - 40	–	160	–	117	–	ns
t_{DW}	Data Setup to $\overline{WR}$	2x - 50	–	110	–	75	–	ns
t_{WD}	Data Hold After $\overline{WR}$	20	70	20	70	20	70	ns
t_{CWA}	$\overline{RD}$, $\overline{WR}$ to Valid $\overline{WAIT}$	–	1.5x - 100	–	20	–	13	ns
t_{AWA}	Address to Valid $\overline{WAIT}$	–	2.5x - 130	–	70	–	26	ns
t_{WAS}	$\overline{WAIT}$ Setup to CLK	50	–	50	–	50	–	ns
t_{WAH}	$\overline{WAIT}$ Hold After CLK	0	–	0	–	0	–	ns
t_{RV}	$\overline{RD}$/$\overline{WR}$ Recovery Time	1.5x - 35	–	85	–	59	–	ns
t_{CPW}	CLK to Port Data Output	–	x + 200	–	280	–	262	ns
t_{PRC}	Port Data Setup to CLK	200	–	200	–	200	–	ns
t_{CPR}	Port Data Hold After CLK	100	–	100	–	100	–	ns
t_{CHCL}	$\overline{RD}$/$\overline{WR}$ Hold After CLK	x - 40	–	40	–	23	–	ns
t_{CLC}	$\overline{RD}$/$\overline{WR}$ Setup to CLK	1.5x - 25	–	95	–	69	–	ns
t_{CLHA}	Address Hold After CLK	1.5x - 80	–	40	–	14	–	ns
t_{ACL}	Address Setup to CLK	2.5x - 80	–	120	–	77	–	ns
t_{CLD}	Data Setup to CLK	x - 50	–	30	–	13	–	ns

- AC output level High 2.2V/Low 0.8V
- AC input level High 2.4V/Low 0.45V (D0 ~ D7)
  High $0.8V_{CC}$/Low $0.2V_{CC}$ (excluding D0 ~ D7)

4.4 Pin Names and Functions

The names of input/output pins and their functions are summarized in Table 2.2.

Table 2.2 Pin Names and Functions (1/1)

Pin Name	No. of Pins	I/O 3 states	Function
P00 ~ P07 /D0 ~ D7	8	I/O	Port 0: 8-bit I/O port that allows selection of input/output on byte basis
		3 states	Data Bus: Also functions as 8-bit bidirectional data bus for external memory
P10 ~ P17 /A0 ~ A7	8	I/O	Port 1: 8-bit I/O port that allows selection on byte basis
		Output	Addrress Bus: The lower 8 bits address bus for external memory
P20 ~ P27 /A8 ~ A 15	8	I/O	Port 2: 8-bit I/O port that allows selection on byte basis
		Output	Addrress Bus: The uppper 8 bits address bus for external memory
P31 /RxD	1	Input	Port 31: 1-bit input port
			Receives Serial Data
P32 /TxD /$\overline{\text{RTS}}$ /SCLK	1	Output	Port 32: 1-bit output port
			Serial clock output
P33 /TxD	1	Output	Port 33: 1-bit output port
			Transmits Serial Data
P35 /$\overline{\text{RD}}$	1	Output	Port 35: 1-bit output port
			Read: Generates strobe signal for reading external memory
P36 /$\overline{\text{WR}}$	1	Output	Port 36: 1-bit output port
			Writes: Generates strobe signal for writing external memory
P37 /$\overline{\text{WAIT}}$ TO1	1	Input	Port 37: 1-bit input port
			Wait: Input pin for connecting slow speed memory or peripheral LSI
		Output	Timer output 1: Output of Timer 0 or 1
P80 /INT0	1	Input	Port 80: 1-bit input port
			Interrupt request pin 0: Interrupt request pin (Level/rising edge is programmable) 
P81 /INT1 /TI2	1	Input	Port 81: 1-bit input port
			Interrupt request pin 1: Interrupt request pin (Rising/falling edge is programmable) 
			Timer input 2: Counter/capture trigger signal for Timer 2
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Falling edge interrupt request pin 
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is pulled up internally during resetting.
$\overline{\text{EA}}$	1	Input	External access: Connects with GND pin in the TMP90CH02 using internal ROM, and with GND pin in the TMP90CH03 with no internal ROM.
$\overline{\text{RESET}}$	1	Input	Reset: Initializes the TMP 90CH02/CH03. (Built-in pull-up resistor)
X1/X2	2	Input/ Output	Pin for quartz crystal or ceramic resonator (1 ~ 16MHz)
V_{CC}	1	–	Power supply (+5V)
V_{SS} (GND)	1	–	Ground (0V)

4.5 Zero-Cross Characteristics

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 16MHz)

Symbol	Parameter	Condition	Min	Max	Unit
V_{ZX}	Zero-cross detection input	AC coupling C = 0.1μF	1	1.8	VAC p - p
A_{ZX}	Zero-cross accuracy	50/60Hz sine wave	–	135	mV
F_{ZX}	Zero-cross detection input frequency	–	0.04	1	kHz

4.6 Serial Channel Timing-I/O Interface Mode

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
CL = 50pF TA = -20 ~ 70°C (1 ~ 16MHz)

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	Serial Port Clock Cycle Time	8x	–	640	–	500	–	ns
t_{OSS}	Output Data Setup SCLK Rising Edge	6x - 150	–	320	–	225	–	ns
t_{OHS}	Output Data Hold After SCLK Rising Edge	2x - 120	–	120	–	45	–	ns
t_{HSR}	Input Data Hold After SCLK Rising Edge	0	–	0	–	0	–	ns
t_{SRD}	SCLK Rising Edge to Input DATA Valid	–	6x - 150	–	450	–	225	ns

4.7 8-bit Event Counter

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 16MHz)

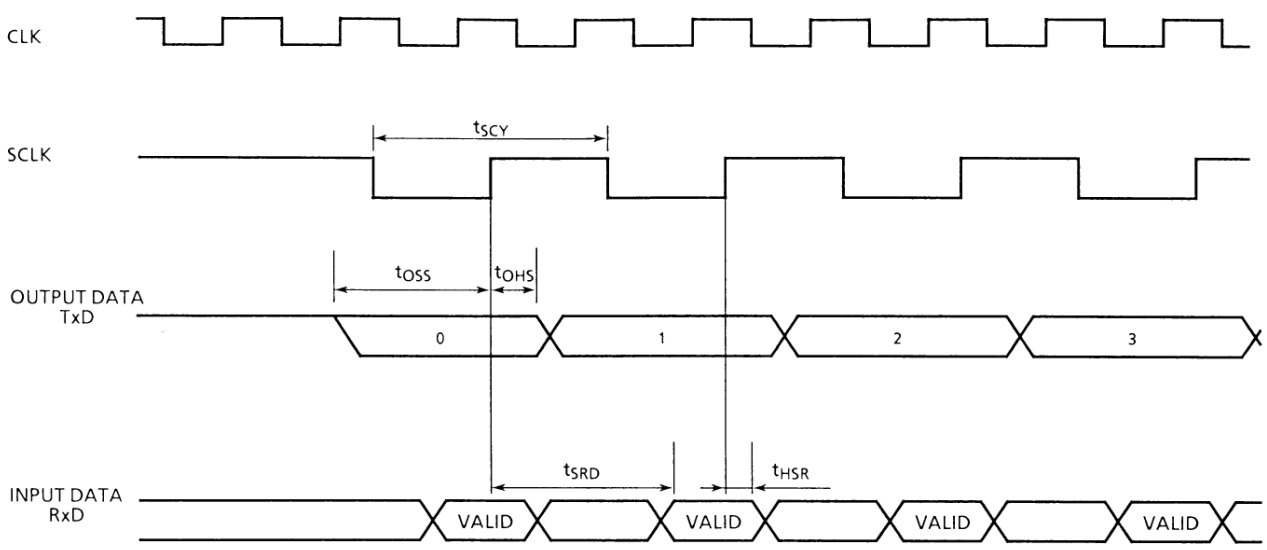
Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	TI2 clock cycle	8x + 100	–	740	–	600	–	ns
t_{VCKL}	TI2 Low clock pulse width	4x + 40	–	360	–	290	–	ns
t_{VCKH}	TI2 High clock pulse width	4x + 40	–	360	–	290	–	ns

4.8 Interrupt Operation

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 16MHz)

Symbol	Parameter	Variable		12.5MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 Low level pulse width 	4x	–	320	–	250	–	ns
t_{INTAH}	$\overline{NMI}$, INT0 High level pulse width 	4x	–	320	–	250	–	ns
t_{INTBL}	INT1, INT2 Low level pulse width 	8x + 100	–	740	–	600	–	ns
t_{INTBH}	INT1, INT2 High level pulse width 	8x + 100	–	740	–	600	–	ns

4.9 I/O Interface Mode Timing Chart



4.10 Timing Chart