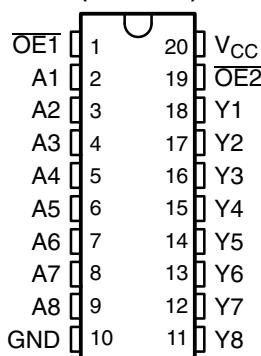
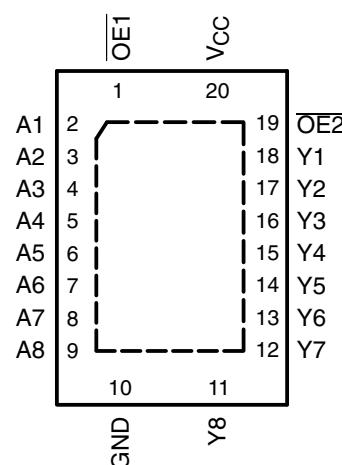


- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 6 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2.3 V at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

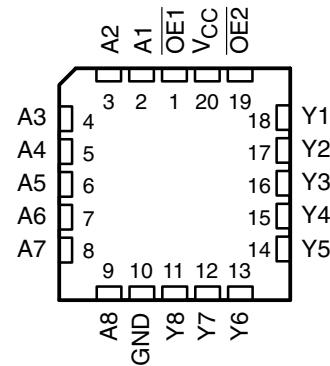
SN54LV541A . . . J OR W PACKAGE  
SN74LV541A . . . DB, DGV, DW, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LV541A . . . RGY PACKAGE  
(TOP VIEW)



SN54LV541A . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

The 'LV541A devices are octal buffers/drivers designed for 2-V to 5.5-V  $V_{CC}$  operation.

## ORDERING INFORMATION

| $T_A$          | PACKAGE <sup>†</sup> | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|-----------------------|------------------|
| –40°C to 85°C  | QFN – RGY            | Reel of 1000          | SN74LV541ARGYR   |
|                | SOIC – DW            | Tube of 25            | SN74LV541ADW     |
|                |                      | Reel of 2000          | SN74LV541ADWR    |
|                | SOP – NS             | Reel of 2000          | SN74LV541ANSR    |
|                | SSOP – DB            | Reel of 2000          | SN74LV541ADBR    |
|                | TSSOP – PW           | Tube of 70            | SN74LV541APW     |
|                |                      | Reel of 2000          | SN74LV541APWR    |
|                |                      | Reel of 250           | SN74LV541APWT    |
| –55°C to 125°C | TVSOP – DGV          | Reel of 2000          | SN74LV541ADGVR   |
|                | CDIP – J             | Tube of 20            | SNJ54LV541AJ     |
|                | CFP – W              | Tube of 85            | SNJ54LV541AW     |
|                | LCCC – FK            | Tube of 55            | SNJ54LV541AFK    |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN54LV541A, SN74LV541A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## description/ordering information (continued)

These devices are ideal for driving bus lines or buffer memory address registers. They feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

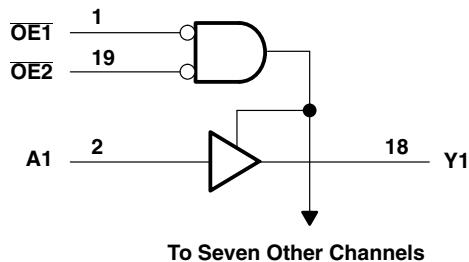
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE  
(each buffer/driver)

| INPUTS |                  |   | OUTPUT<br>Y |
|--------|------------------|---|-------------|
| OE1    | $\overline{OE2}$ | A |             |
| L      | L                | L | L           |
| L      | L                | H | H           |
| H      | X                | X | Z           |
| X      | H                | X | Z           |

## logic diagram (positive logic)



# **SN54LV541A, SN74LV541A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 5.5 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.  
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

**SN54LV541A, SN74LV541A  
OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 5)**

|                 |                                    |                                  | SN54LV541A            |                       | SN74LV541A            |                       | UNIT |
|-----------------|------------------------------------|----------------------------------|-----------------------|-----------------------|-----------------------|-----------------------|------|
|                 |                                    |                                  | MIN                   | MAX                   | MIN                   | MAX                   |      |
| V <sub>CC</sub> | Supply voltage                     |                                  | 2                     | 5.5                   | 2                     | 5.5                   | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 2 V            | 1.5                   | 1.5                   | V <sub>CC</sub> × 0.7 | V <sub>CC</sub> × 0.7 | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.7 | V <sub>CC</sub> × 0.7 |                       |                       |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.7 | V <sub>CC</sub> × 0.7 |                       |                       |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.7 | V <sub>CC</sub> × 0.7 |                       |                       |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 2 V            | 0.5                   | 0.5                   | V <sub>CC</sub> × 0.3 | V <sub>CC</sub> × 0.3 | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.3 | V <sub>CC</sub> × 0.3 |                       |                       |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.3 | V <sub>CC</sub> × 0.3 |                       |                       |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.3 | V <sub>CC</sub> × 0.3 |                       |                       |      |
| V <sub>I</sub>  | Input voltage                      |                                  | 0                     | 5.5                   | 0                     | 5.5                   | V    |
| V <sub>O</sub>  | Output voltage                     | High or low state                | 0                     | V <sub>CC</sub>       | 0                     | V <sub>CC</sub>       | V    |
|                 |                                    | 3-state                          | 0                     | 5.5                   | 0                     | 5.5                   |      |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 2 V            | –50                   | –50                   | –50                   | –50                   | μA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | –2                    | –2                    |                       |                       |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | –8                    | –8                    |                       |                       |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | –16                   | –16                   |                       |                       |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2 V            | 50                    | 50                    | 50                    | 50                    | μA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | 2                     | 2                     |                       |                       |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | 8                     | 8                     |                       |                       |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | 16                    | 16                    |                       |                       |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 2.3 V to 2.7 V | 200                   | 200                   | 200                   | 200                   | ns/V |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | 100                   | 100                   |                       |                       |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | 20                    | 20                    |                       |                       |      |
| T <sub>A</sub>  | Operating free-air temperature     |                                  | –55                   | 125                   | –40                   | 85                    | °C   |

NOTE 5: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER        | TEST CONDITIONS   | V <sub>CC</sub> | SN54LV541A            |      |     | SN74LV541A            |      |     | UNIT |
|------------------|---|-----------------|-----------------------|------|-----|-----------------------|------|-----|------|
|                  |   |                 | MIN                   | TYP  | MAX | MIN                   | TYP  | MAX |      |
| V <sub>OH</sub>  | I <sub>OH</sub> = –50 μA                                    | 2 V to 5.5 V    | V <sub>CC</sub> – 0.1 |      |     | V <sub>CC</sub> – 0.1 |      |     | V    |
|                  | I <sub>OH</sub> = –2 mA                                     | 2.3 V           | 2                     |      |     | 2                     |      |     |      |
|                  | I <sub>OH</sub> = –8 mA                                     | 3 V             | 2.48                  |      |     | 2.48                  |      |     |      |
|                  | I <sub>OH</sub> = –16 mA                                    | 4.5 V           | 3.8                   |      |     | 3.8                   |      |     |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 50 μA                                     | 2 V to 5.5 V    |                       | 0.1  |     |                       | 0.1  |     | V    |
|                  | I <sub>OL</sub> = 2 mA                                      | 2.3 V           |                       | 0.4  |     |                       | 0.4  |     |      |
|                  | I <sub>OL</sub> = 8 mA                                      | 3 V             |                       | 0.44 |     |                       | 0.44 |     |      |
|                  | I <sub>OL</sub> = 16 mA                                     | 4.5 V           |                       | 0.55 |     |                       | 0.55 |     |      |
| I <sub>I</sub>   | V <sub>I</sub> = 5.5 V or GND                               | 0 to 5.5 V      |                       | ±1   |     |                       | ±1   |     | μA   |
| I <sub>OZ</sub>  | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5.5 V           |                       | ±5   |     |                       | ±5   |     | μA   |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           |                       | 20   |     |                       | 20   |     | μA   |
| I <sub>off</sub> | V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V               | 0               |                       | 5    |     |                       | 5    |     | μA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 3.3 V           |                       | 2    |     |                       | 2    |     | pF   |

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER   | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE   | $T_A = 25^\circ\text{C}$ |       |     | SN54LV541A |     | SN74LV541A |     | UNIT |
|-------------|-----------------|----------------|-----------------------|--------------------------|-------|-----|------------|-----|------------|-----|------|
|             |                 |                |                       | MIN                      | TYP   | MAX | MIN        | MAX | MIN        | MAX |      |
| $t_{pd}$    | A               | Y              | $C_L = 15 \text{ pF}$ | 6.7*                     | 11.3* | 1*  | 13.5*      | 1   | 13.5       |     | ns   |
| $t_{en}$    | $\overline{OE}$ | Y              |                       | 8.5*                     | 16.6* | 1*  | 19.5*      | 1   | 19.5       |     |      |
| $t_{dis}$   | $\overline{OE}$ | Y              |                       | 8.4*                     | 13.1* | 1*  | 15*        | 1   | 15         |     |      |
| $t_{pd}$    | A               | Y              | $C_L = 50 \text{ pF}$ | 8.7                      | 15.9  | 1*  | 18.5       | 1   | 18.5       |     | ns   |
| $t_{en}$    | $\overline{OE}$ | Y              |                       | 10.5                     | 20.7  | 1*  | 24         | 1   | 24         |     |      |
| $t_{dis}$   | OE              | Y              |                       | 12.3                     | 17.9  | 1   | 20         | 1   | 20         |     |      |
| $t_{sk(o)}$ |                 |                |                       |                          | 2     |     |            |     |            | 2   |      |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER   | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE   | $T_A = 25^\circ\text{C}$ |       |     | SN54LV541A |     | SN74LV541A |     | UNIT |
|-------------|-----------------|----------------|-----------------------|--------------------------|-------|-----|------------|-----|------------|-----|------|
|             |                 |                |                       | MIN                      | TYP   | MAX | MIN        | MAX | MIN        | MAX |      |
| $t_{pd}$    | A               | Y              | $C_L = 15 \text{ pF}$ | 4.8*                     | 7*    | 1*  | 8.5*       | 1   | 8.5        |     | ns   |
| $t_{en}$    | $\overline{OE}$ | Y              |                       | 6.1*                     | 10.5* | 1*  | 12.5*      | 1   | 12.5       |     |      |
| $t_{dis}$   | $\overline{OE}$ | Y              |                       | 5.8*                     | 11*   | 1*  | 12*        | 1   | 12         |     |      |
| $t_{pd}$    | A               | Y              | $C_L = 50 \text{ pF}$ | 6.1                      | 10.5  | 1*  | 12         | 1   | 12         |     | ns   |
| $t_{en}$    | OE              | Y              |                       | 7.4                      | 14    | 1*  | 16         | 1   | 16         |     |      |
| $t_{dis}$   | OE              | Y              |                       | 8.8                      | 15.4  | 1   | 17.5       | 1   | 17.5       |     |      |
| $t_{sk(o)}$ |                 |                |                       |                          | 1.5   |     |            |     |            | 1.5 |      |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER   | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE   | $T_A = 25^\circ\text{C}$ |      |     | SN54LV541A |     | SN74LV541A |     | UNIT |
|-------------|-----------------|----------------|-----------------------|--------------------------|------|-----|------------|-----|------------|-----|------|
|             |                 |                |                       | MIN                      | TYP  | MAX | MIN        | MAX | MIN        | MAX |      |
| $t_{pd}$    | A               | Y              | $C_L = 15 \text{ pF}$ | 3.5*                     | 5*   | 1*  | 6*         | 1   | 6          |     | ns   |
| $t_{en}$    | $\overline{OE}$ | Y              |                       | 4.3*                     | 7.2* | 1*  | 8.5*       | 1   | 8.5        |     |      |
| $t_{dis}$   | $\overline{OE}$ | Y              |                       | 3.9*                     | 7.5* | 1*  | 8*         | 1   | 8          |     |      |
| $t_{pd}$    | A               | Y              | $C_L = 50 \text{ pF}$ | 4.3                      | 7    | 1*  | 8          | 1   | 8          |     | ns   |
| $t_{en}$    | OE              | Y              |                       | 5.3                      | 9.2  | 1*  | 10.5       | 1   | 10.5       |     |      |
| $t_{dis}$   | $\overline{OE}$ | Y              |                       | 5.6                      | 8.8  | 1   | 10         | 1   | 10         |     |      |
| $t_{sk(o)}$ |                 |                |                       |                          | 1    |     |            |     |            | 1   |      |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**SN54LV541A, SN74LV541A  
OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

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**noise characteristics,  $V_{CC} = 3.3$  V,  $C_L = 50$  pF,  $T_A = 25^\circ\text{C}$  (see Note 6)**

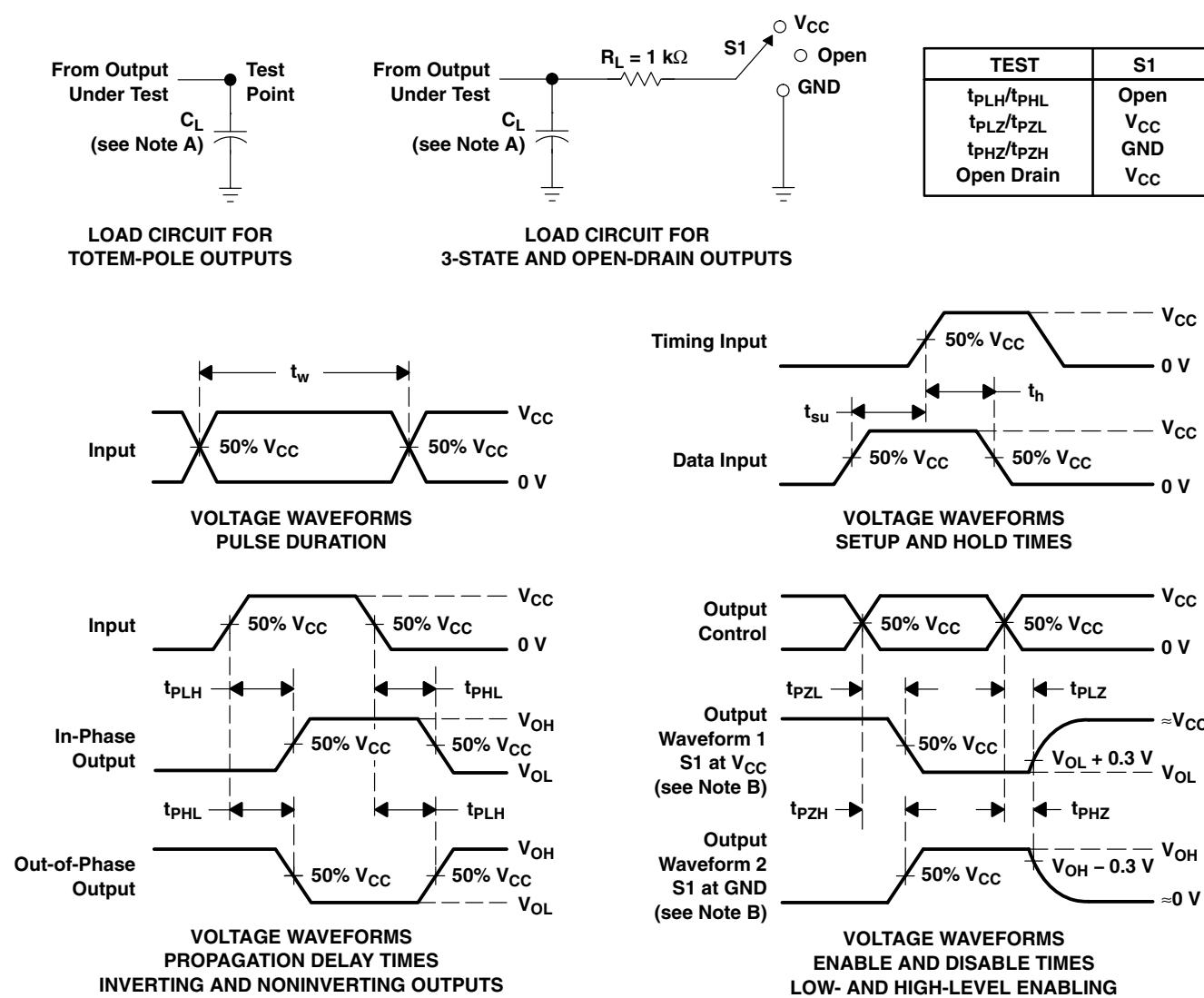
| PARAMETER   | SN74LV541A                             |     |      | UNIT |   |
|-------------|--|-----|------|------|---|
|             | MIN                                    | TYP | MAX  |      |   |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ |     | 0.5  | 0.8  | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ |     | -0.4 | -0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ |     | 2.9  |      | V |
| $V_{IH(D)}$ | High-level dynamic input voltage       |     | 2.31 |      | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage        |     | 0.99 |      | V |

NOTE 6: Characteristics are for surface-mount packages only.

**operating characteristics,  $T_A = 25^\circ\text{C}$**

| PARAMETER | TEST CONDITIONS               |                             | $V_{CC}$ | TYP  | UNIT |
|-----------|-------------------------------|-----------------------------|----------|------|------|
|           | Outputs enabled               | $C_L = 50$ pF, $f = 10$ MHz |          |      |      |
| $C_{pd}$  | Power dissipation capacitance |                             | 3.3 V    | 16.3 | pF   |
|           |                               |                             | 5 V      | 17.8 |      |

PARAMETER MEASUREMENT INFORMATION



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .
- The outputs are measured one at a time, with one input transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device  | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| SN74LV541ADBR     | ACTIVE        | SSOP         | DB              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LV541A                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541ADBRE4   | ACTIVE        | SSOP         | DB              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LV541A                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541ADB RG4  | ACTIVE        | SSOP         | DB              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LV541A                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541ADGVR    | OBSOLETE      | TVSOP        | DGV             | 20   |             | TBD                     | Call TI                 | Call TI              | -40 to 85    | LV541A                  |   |
| SN74LV541ADGVRE4  | OBSOLETE      | TVSOP        | DGV             | 20   |             | TBD                     | Call TI                 | Call TI              | -40 to 85    |                         |   |
| SN74LV541ADGV RG4 | OBSOLETE      | TVSOP        | DGV             | 20   |             | TBD                     | Call TI                 | Call TI              | -40 to 85    |                         |   |
| SN74LV541ADW      | ACTIVE        | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LV541A                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541ADWG4    | ACTIVE        | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LV541A                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541ADWR     | ACTIVE        | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LV541A                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541ADWRE4   | ACTIVE        | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LV541A                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541ANSR     | ACTIVE        | SO           | NS              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | 74LV541A                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541ANSRG4   | ACTIVE        | SO           | NS              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | 74LV541A                | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541APW      | ACTIVE        | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LV541A                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541APWG4    | ACTIVE        | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LV541A                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541APWR     | ACTIVE        | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU   CU SN       | Level-1-260C-UNLIM   | -40 to 85    | LV541A                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541APWRG4   | ACTIVE        | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LV541A                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541APWT     | ACTIVE        | TSSOP        | PW              | 20   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LV541A                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LV541ARGYR    | ACTIVE        | VQFN         | RGY             | 20   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | LV541A                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

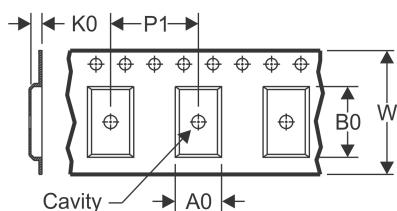
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

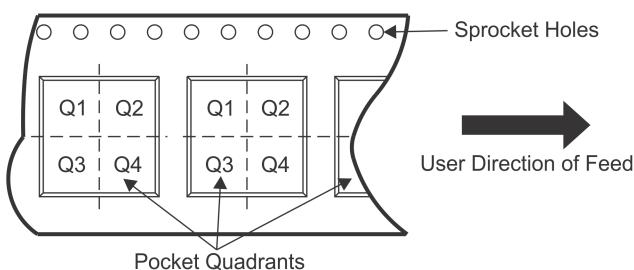
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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV541ADBR  | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LV541ADWR  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LV541ANSR  | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 8.2     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74LV541APWR  | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LV541APWR  | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LV541APWT  | TSSOP        | PW              | 20   | 250  | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LV541ARGYR | VQFN         | RGY             | 20   | 3000 | 330.0              | 12.4               | 3.8     | 4.8     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**

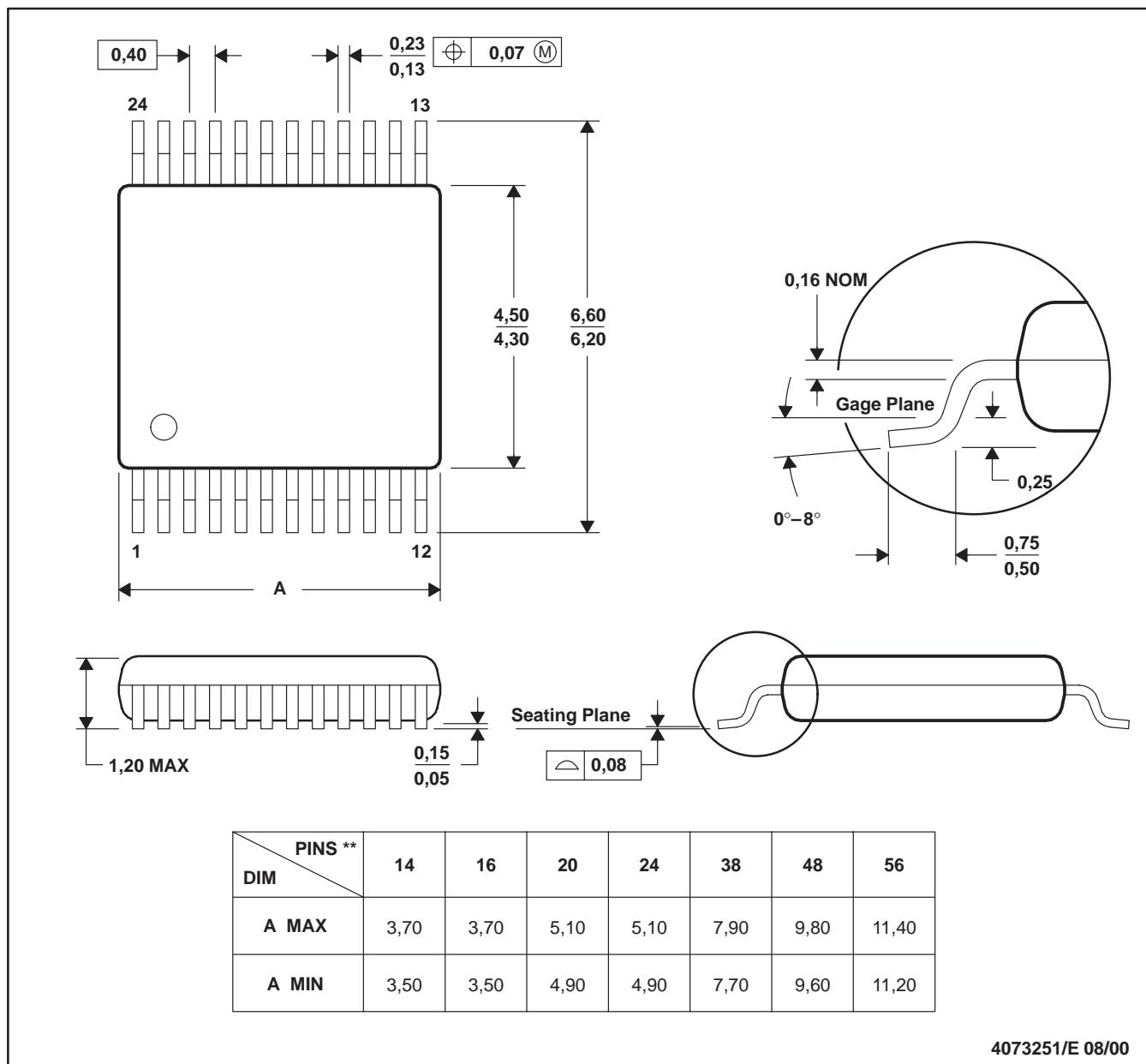

\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV541ADBR  | SSOP         | DB              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LV541ADWR  | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LV541ANSR  | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LV541APWR  | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LV541APWR  | TSSOP        | PW              | 20   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74LV541APWT  | TSSOP        | PW              | 20   | 250  | 367.0       | 367.0      | 38.0        |
| SN74LV541ARGYR | VQFN         | RGY             | 20   | 3000 | 367.0       | 367.0      | 35.0        |

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

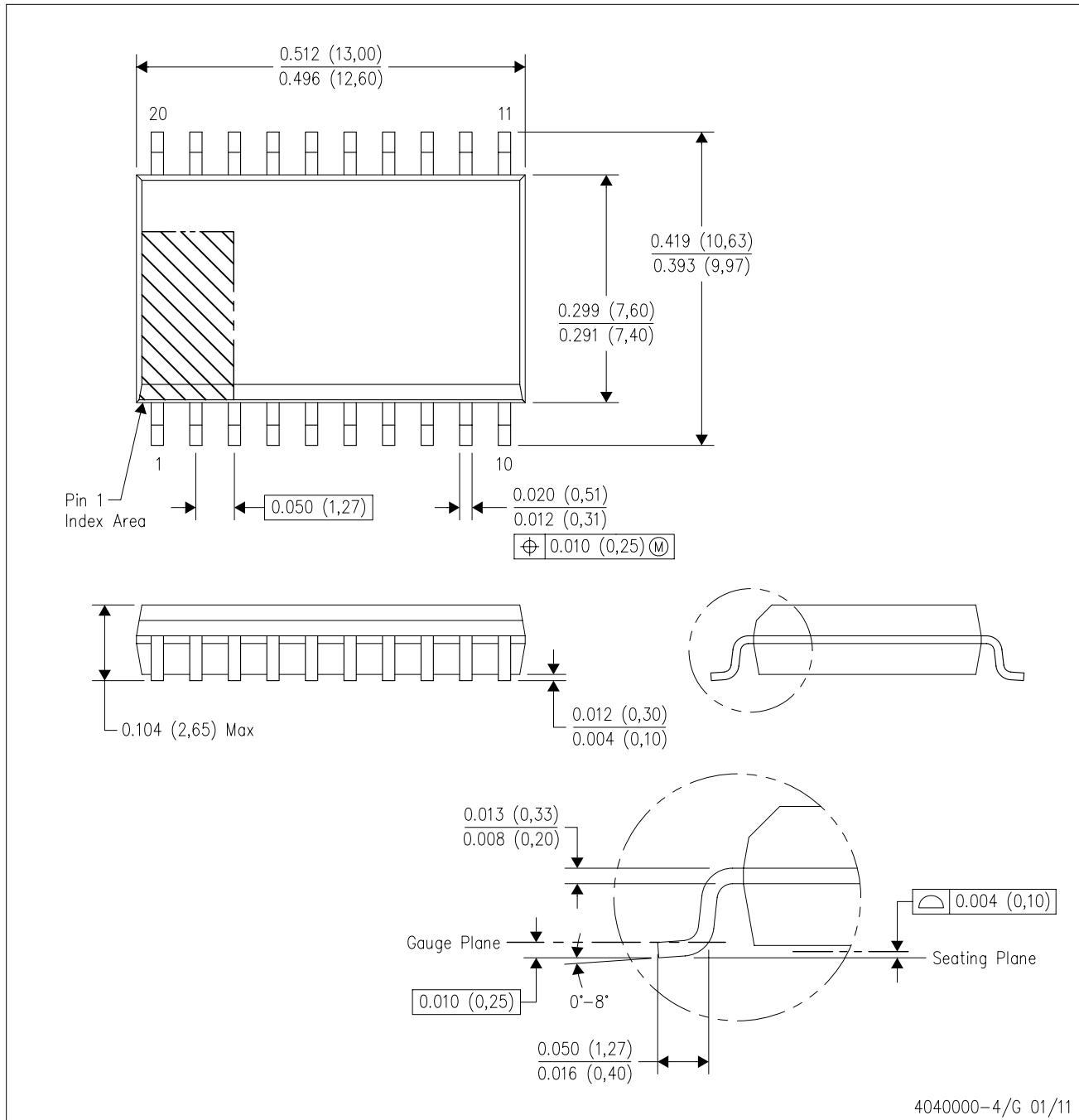
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

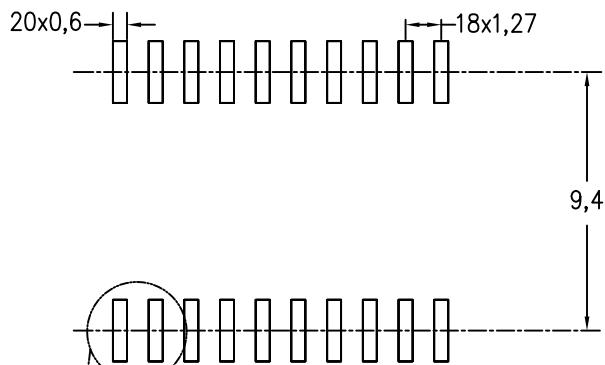
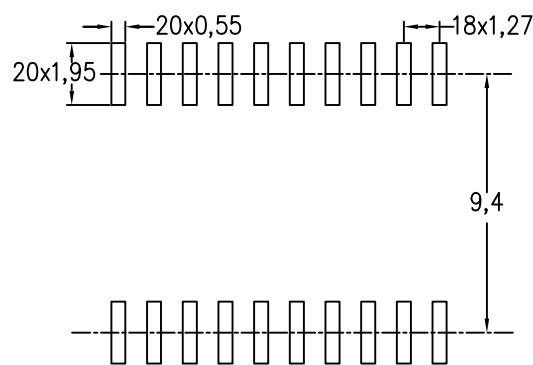


NOTES:

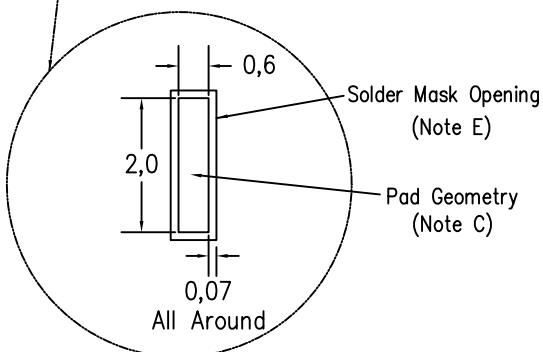
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)

Non Solder Mask Define Pad



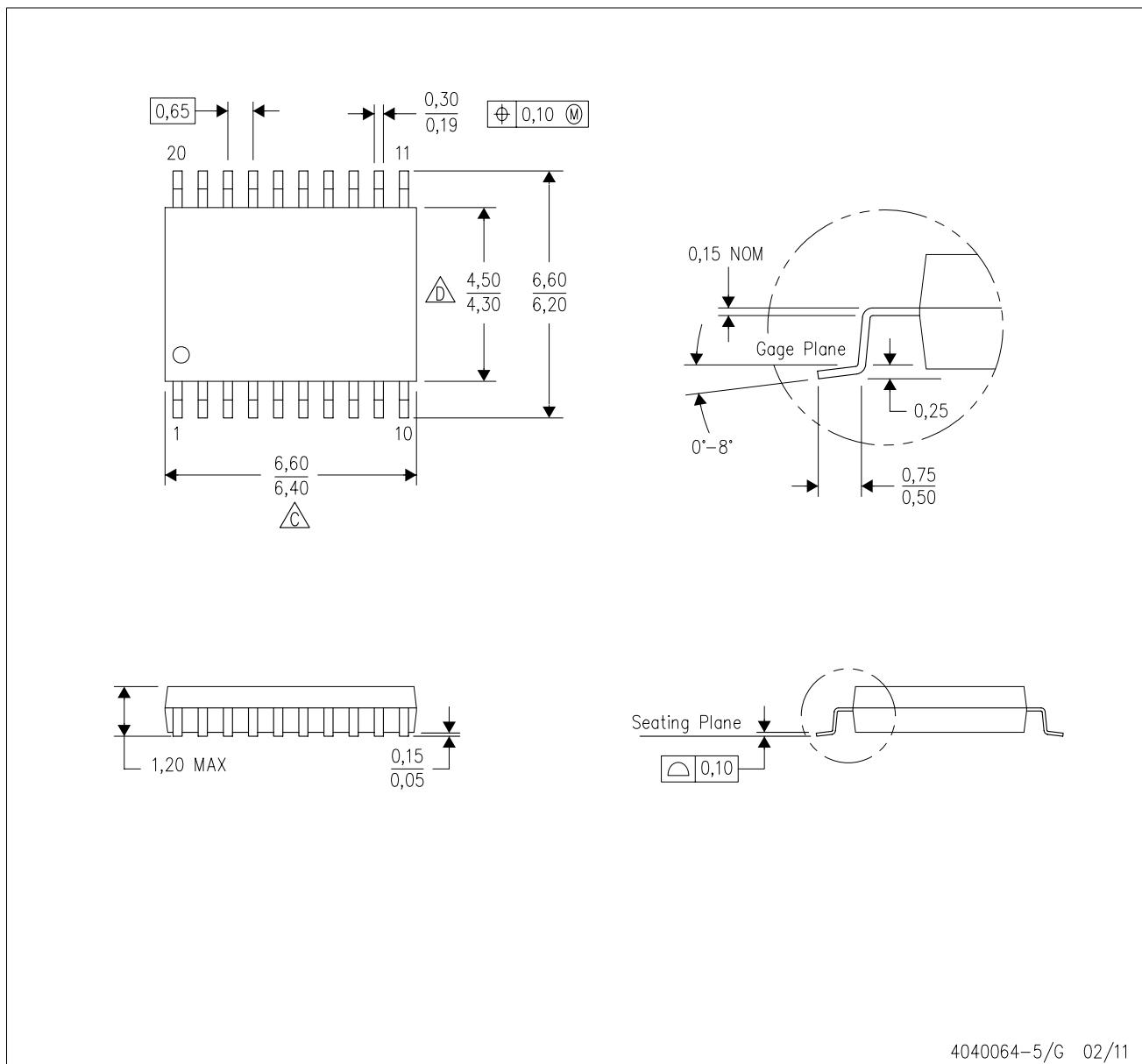
4209202-4/F 08/13

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

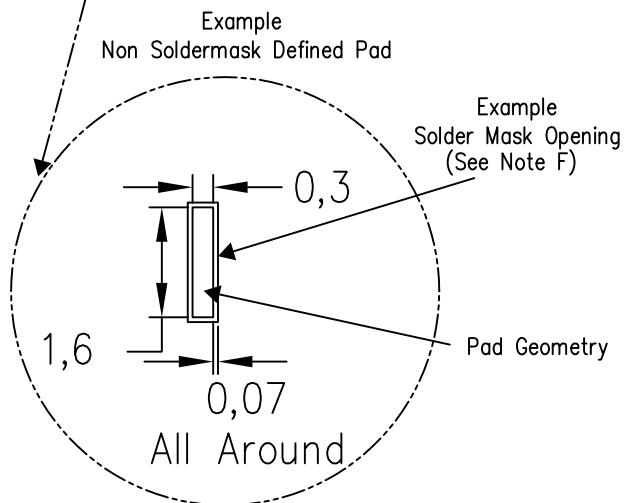
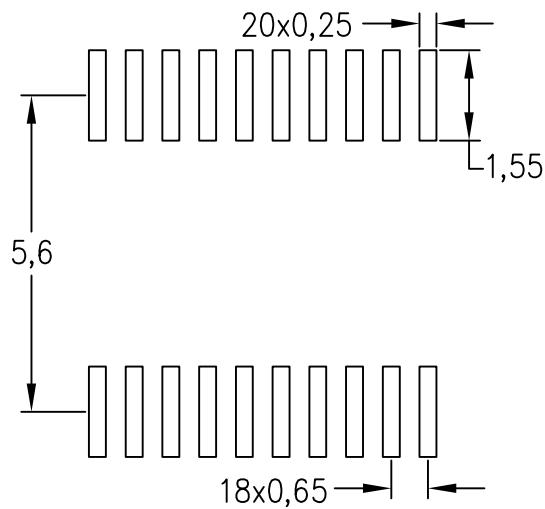
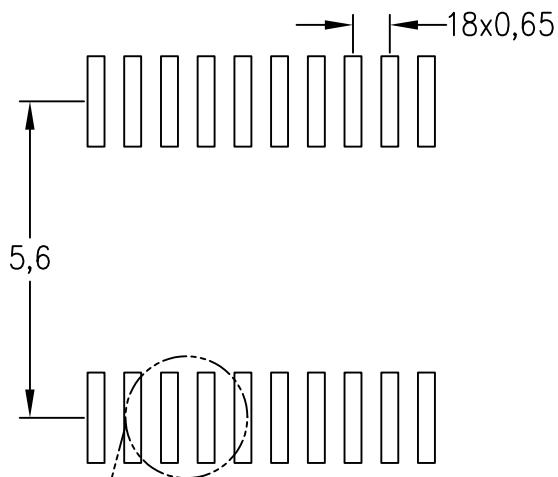
4040064-5/G 02/11

## PW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE

## Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).



4211284-5/F 12/12

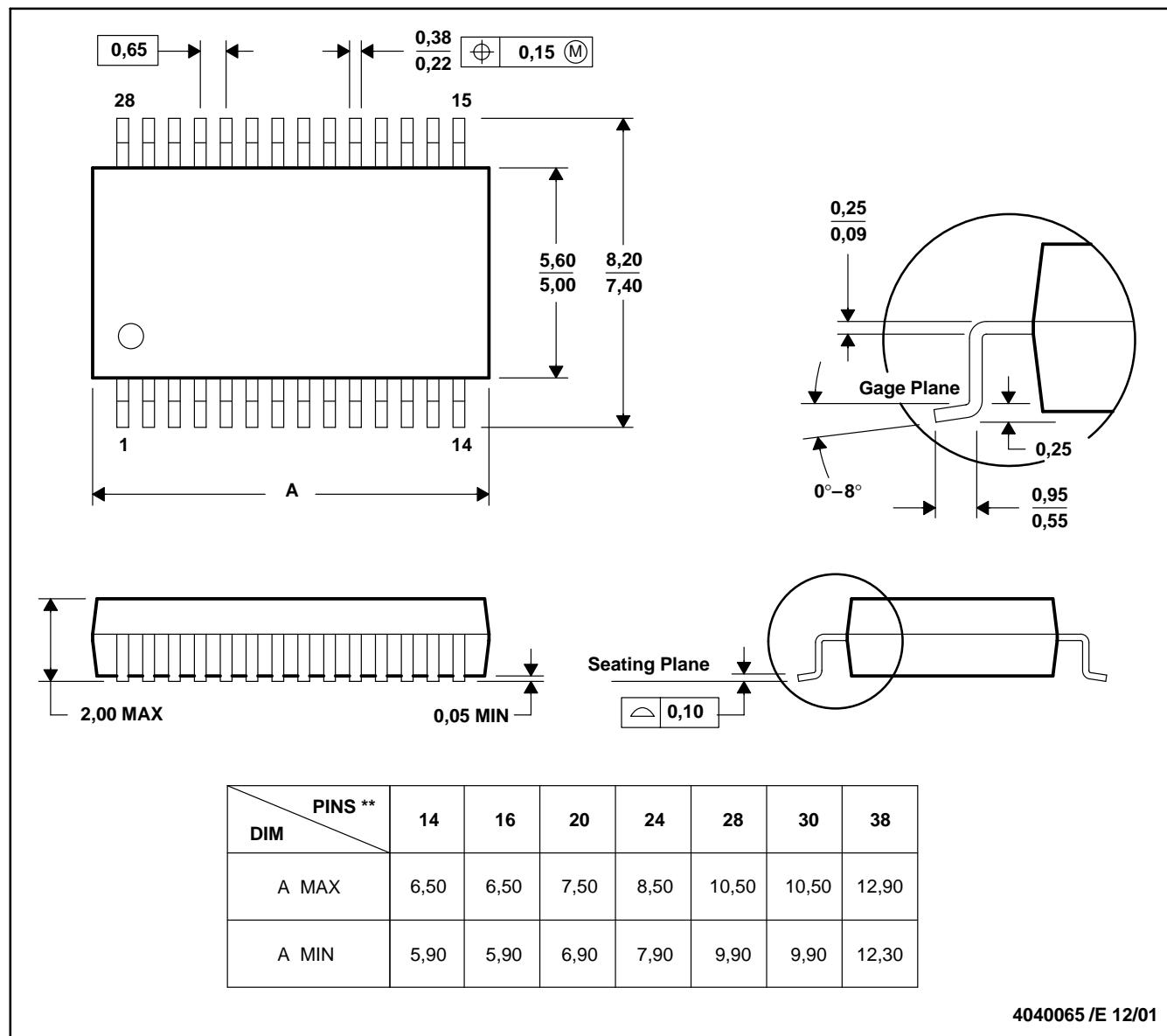
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN

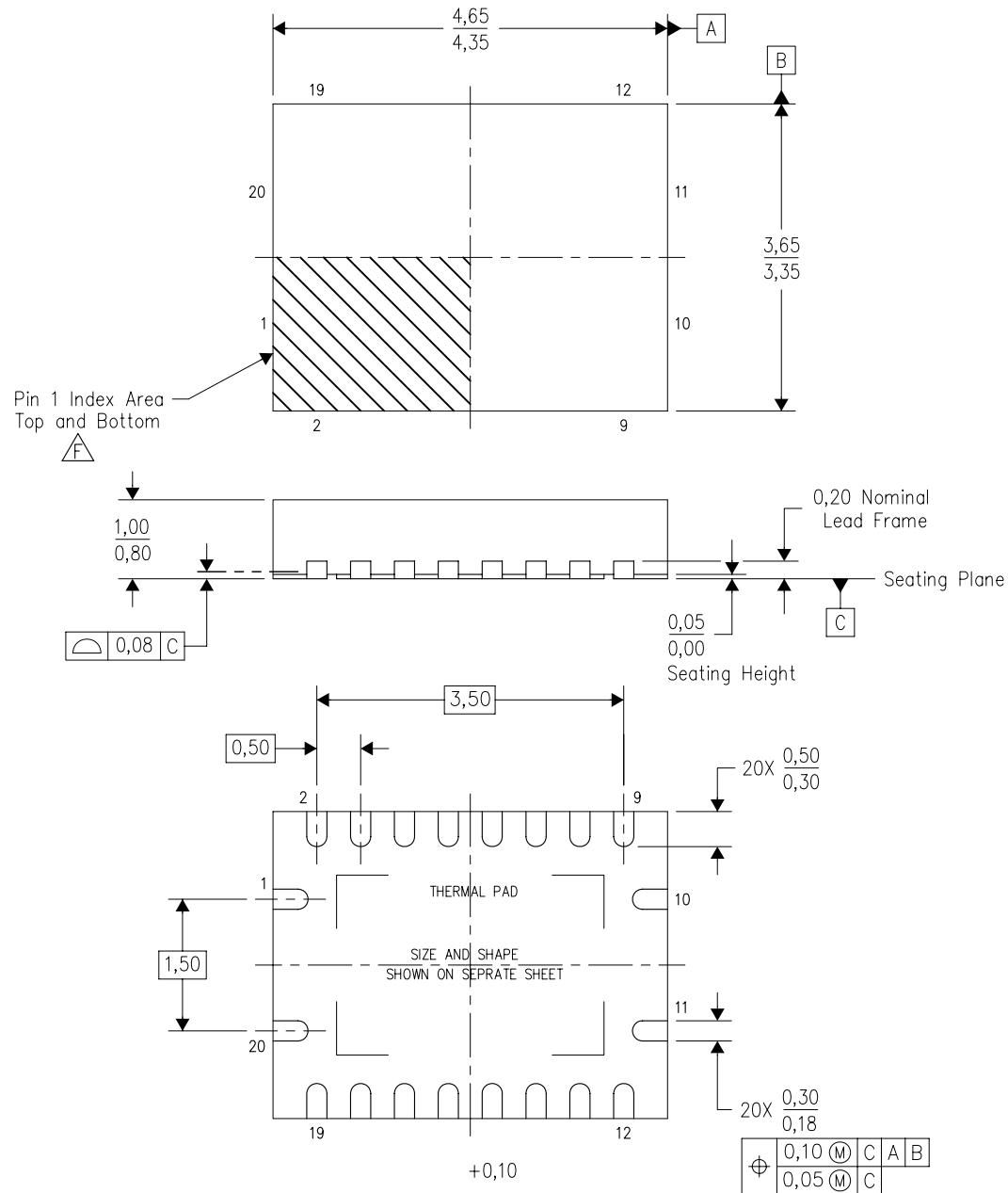


NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## MECHANICAL DATA

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-4/l 06/2011

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- QFN (Quad Flatpack No-Lead) package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance.
- See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

# THERMAL PAD MECHANICAL DATA

RGY (R-PVQFN-N20)

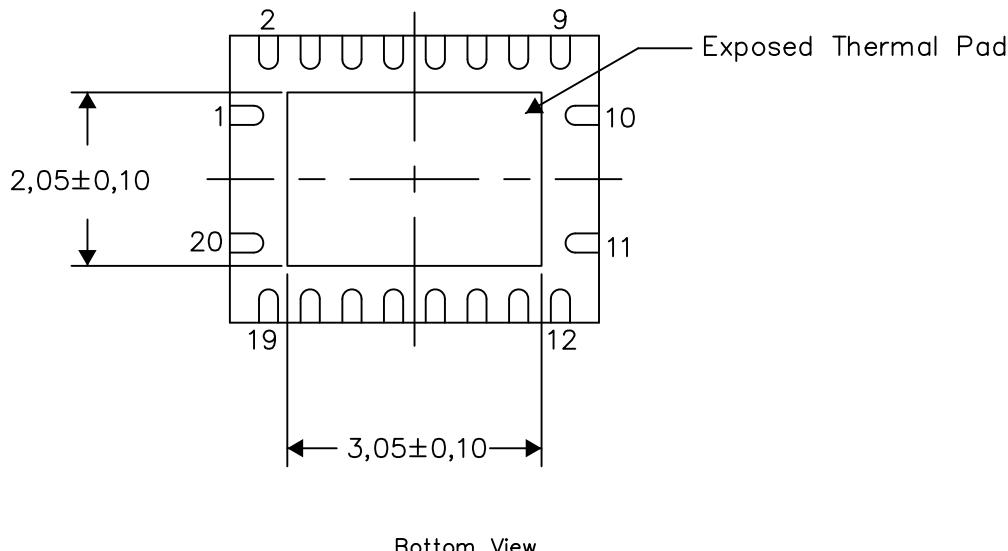
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

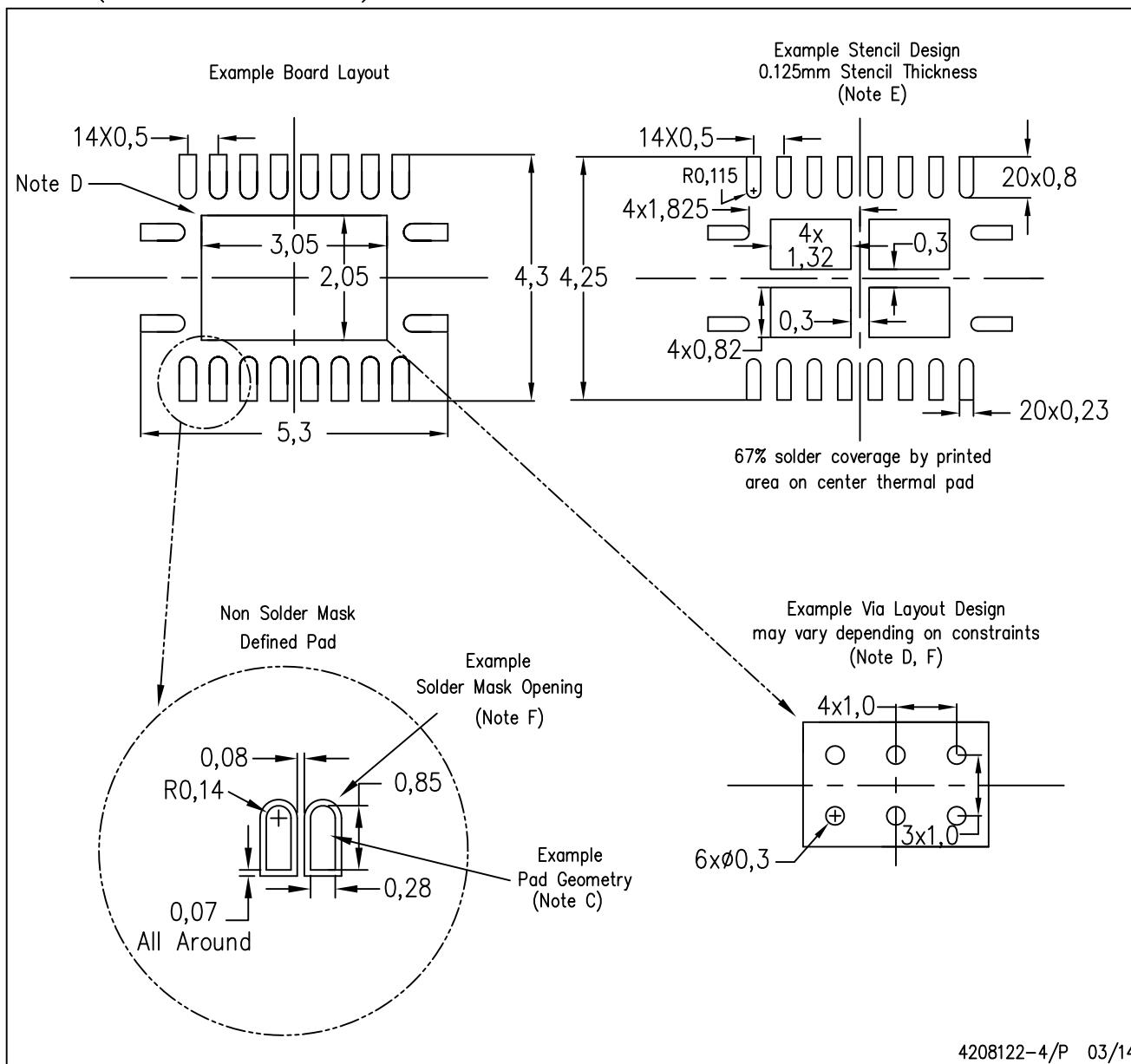
Exposed Thermal Pad Dimensions

4206353-4/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-4/P 03/14

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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| Data Converters              | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>                       |
| DLP® Products                | <a href="http://www.dlp.com">www.dlp.com</a>   |
| DSP                          | <a href="http://dsp.ti.com">dsp.ti.com</a>   |
| Clocks and Timers            | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
| Interface                    | <a href="http://interface.ti.com">interface.ti.com</a>                               |
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| Power Mgmt                   | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers             | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                         | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity        | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |
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|                              | <a href="http://e2e.ti.com">e2e.ti.com</a>   |