HA1630D07

Dual CMOS High Drive Operational Amplifier

REJ03D0859-0200
Rev.2.00
Nov 30, 2007

Description

HA1630D07 is a low power dual CMOS operational amplifier featuring high output current with typical current supply of 120 µA for both channels (2.7 V to 5.5 V). This IC designed to operate from a single power supply and have full swing outputs. Available in MMPAK-8 and TSSOP-8 package, the miniature size of this IC not only allows compact integration in portable devices but also minimizes distance of signal sources (sensors), thus reducing external noise pick up prior to amplification. This IC exhibit excellent current drive-power ratio capable of 2 kΩ load driving and yet resistant to oscillation for capacitive loads up to 200 pF.

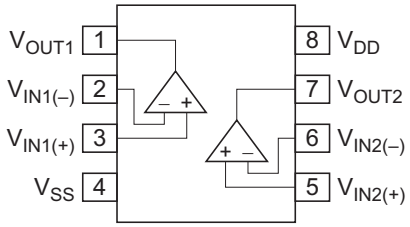
Features

- Low supply current I_{DD} = 120 µA Typ (V_{DD} = 3 V, R_L = No load)
- Low voltage operation V_{DD} = 2.7 V to 5.5 V
- Low input offset voltage V_{IO} = 6 mV Max
- Low input bias current I_{IB} = 1 pA Typ
- High output current $I_{OSOURCE}$ = 15 mA Typ (V_{DD} = 3.0 V, V_{OH} = 2.5 V)
  I_{OSINK} = 15 mA Typ (V_{DD} = 3.0 V, V_{OL} = 0.5 V)
- Input common voltage range includes ground

Ordering Information

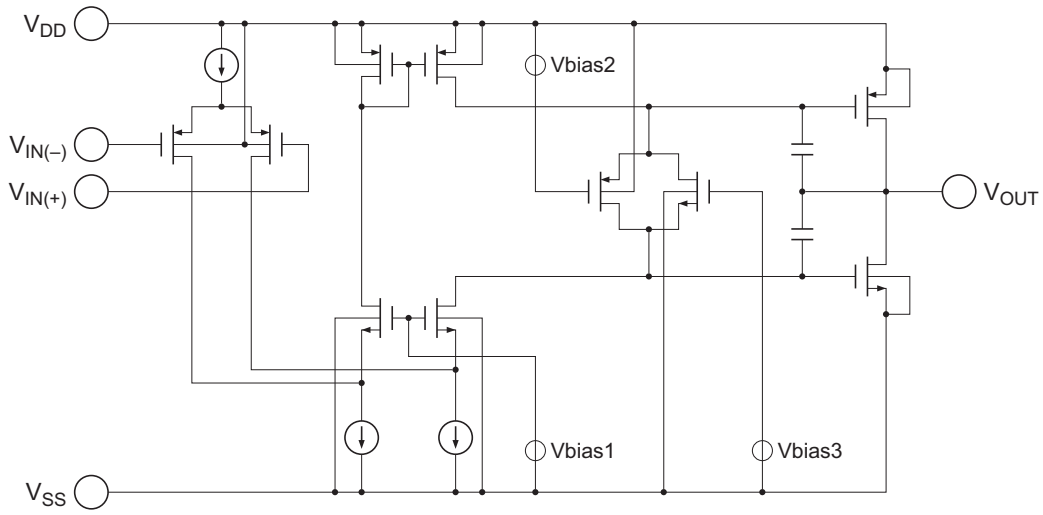
Part No.	Package Name	Package Code
HA1630D07MM	MMPAK-8	PLSP0008JC-A
HA1630D07T	TSSOP-8	PTSP0008JC-B

Pin Arrangement



(Top view)

Equivalent Circuit (1/2)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	7.0	V	
Differential input voltage	$V_{IN(diff)}$	$-V_{DD}$ to $+V_{DD}$	V	1
Input voltage	V_{IN}	–0.1 to $+V_{DD}$	V	
Output current	I_{OUT}	40	mA	
Power dissipation	P_T	145 (MMPAK-8)	mW	2
		192 (TSSOP-8)		
Operating temperature	Topr	–40 to +85	°C	
Storage temperature	Tstg	–55 to +125	°C	

Note: 1. Do not apply input voltage exceeding V_{DD} or 7 V.
2. If Ta > 25°C,
MMPAK-8: derate by –1.45 mW/°C
TSSOP-8: derate by –1.92 mW/°C

Electrical Characteristics

DC Characteristics

(Ta = 25°C, V_{DD} = 3.0 V, V_{SS} = 0 V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input offset voltage	V_{IO}	—	—	6	mV	V_{IN} = 1.5 V, R_L = 1 MΩ
Input bias current	I_{IB}	—	(1)	—	pA	V_{IN} = 1.5 V
Input offset current	I_{IO}	—	(1)	—	pA	V_{IN} = 1.5 V
Common mode input voltage range	V_{CM}	–0.1	—	1.8	V	
Supply current	I_{DD}	—	120	340	µA	$V_{IN(+)}$ = 1.0 V, R_L = ∞
Output source current	$I_{OSOURCE}$	7.5	15	—	mA	V_{OUT} = 2.5 V
Output sink current	I_{OSINK}	7.5	15	—	mA	V_{OUT} = 0.5 V
Open loop voltage gain	A_V	55	80	—	dB	R_L = 100 kΩ
Common mode rejection ratio	CMRR	50	80	—	dB	V_{IN1} = 0 V, V_{IN2} = 1.8 V
Power supply rejection ratio	PSRR	55	80	—	dB	V_{DD1} = 2.7 V, V_{DD2} = 5.5 V
Output high voltage	V_{OH}	2.9	—	—	V	R_L = 2 kΩ to V_{SS}
Output low voltage	V_{OL}	—	—	0.1	V	R_L = 2 kΩ to V_{DD}

Note: ( ) : Design specification

AC Characteristics

(Ta = 25°C, V_{DD} = 3.0 V, V_{SS} = 0 V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Slew rate	SRr	—	(1)	—	V/µs	V_{IN} = 1.5 V, C_L = 15 pF
	SRf	—	(1)	—		(V_{INL} = 0.2 V, V_{INH} = 1.7 V)
Gain bandwidth product	GBW	—	(1.5)	—	MHz	V_{IN} = 1.5 V, C_L = 15 pF

Note: ( ) : Design specification

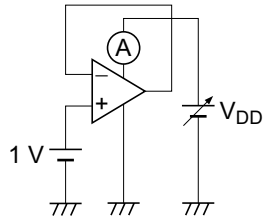
Table of Graphs

Electrical Characteristics			Characteristic Curves	Test Circuit No.
Supply current	I_{DD}	vs. Supply voltage	1	1
		vs. Temperature	2	1
Output high voltage	V_{OH}	vs. Rload	3	2
Output low voltage	V_{OL}	vs. Rload	4	3
Output source current	$I_{OSOURCE}$	vs. Output high voltage	5	4
		vs. Temperature	6	4
Output sink current	I_{OSINK}	vs. Output low voltage	7	5
		vs. Temperature	8	5
Input offset voltage	V_{IO}	vs. Supply voltage	9	6
		vs. Input voltage	10	6
		vs. Temperature	11	7
Common mode input voltage range	V_{CM}	vs. Supply voltage	12	8
		vs. Temperature	13	8
Common mode rejection ratio	CMRR	vs. Input voltage	14	9
Power supply rejection ratio	PSRR	vs. Supply voltage	15	10
Input bias current	I_{IB}	vs. Input voltage	16	11, 12
		vs. Temperature	17	11, 12
Slew rate (rising)	SRr	vs. Cload	18	13
		vs. Temperature	19	13
		Time waveform	20	13
Slew rate (falling)	SRf	vs. Cload	21	13
		vs. Temperature	22	13
		Time waveform	23	13
Open loop gain	A_V	vs. Rload	24	14
		vs. Frequency	25, 26	14
Phase margin	PM	vs. Cload	27	14
Channel separation	CS	vs. Frequency	28	15
Noise input voltage	VNI	vs. Frequency	29	16

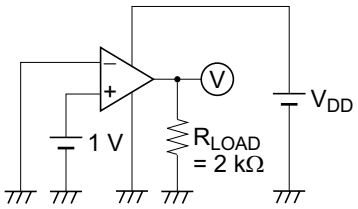
Test Circuits

(Unless otherwise noted, V_{DD} = 3 V, V_{SS} = 0 V, Ta = 25°C)

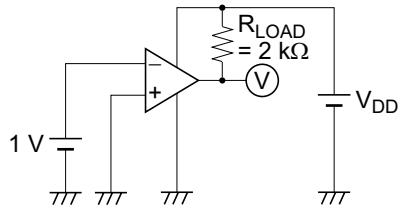
1. Supply Current, I_{DD}



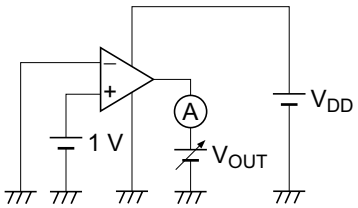
2. Output High Voltage, V_{OH}



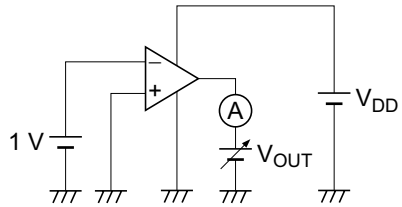
3. Output Low Voltage, V_{OL}



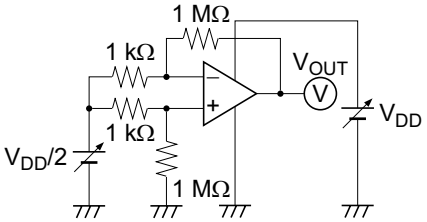
4. Output Source Current, $I_{OSOURCE}$



5. Output Sink Current, I_{OSINK}

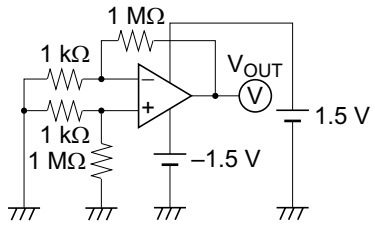


6. Input Offset Voltage vs. Operating Voltage



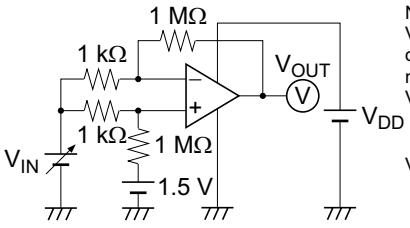
$V_{IO} = V_{OUT} / 1001$

7. Input Offset Voltage, V_{IO}

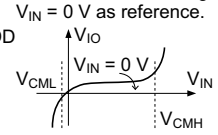


$V_{IO} = V_{OUT} / 1001$

8. Common Mode Input Voltage Range, V_{CM}



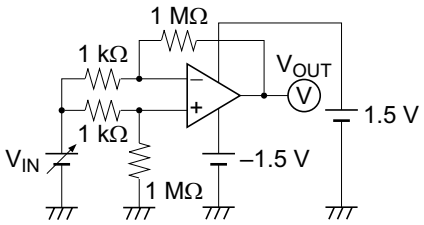
Note:
V_{CML} and V_{CMH} are values of V_{IN} when V_{IO} changes more than 50 dB taking V_{IN} = 0 V as reference.



Test Circuits (cont.)

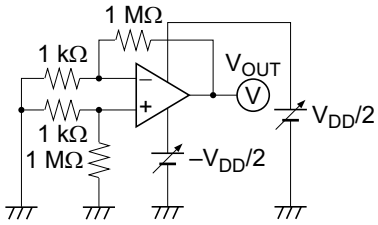
(Unless otherwise noted, V_{DD} = 3 V, V_{SS} = 0 V, Ta = 25°C)

9. Common Mode Rejection Ratio, CMRR



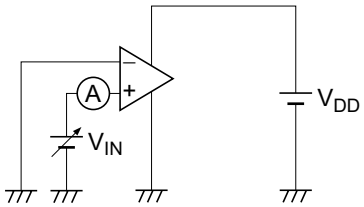
V_{IN}	Measure Point	Calculate V_{IO}	CMRR Calculation
–1.5 V	V_{OUT1}	$V_{IO1} = V_{OUT1} / 1001$	$CMRR = \left\| 20\log_{10} \frac{\|[V_{IO2} - V_{IO1}]\|}{0.3 - (-1.5\ V)} \right\|$
0.3 V	V_{OUT2}	$V_{IO2} = V_{OUT2} / 1001$	

10. Power Supply Rejection Ratio, PSRR

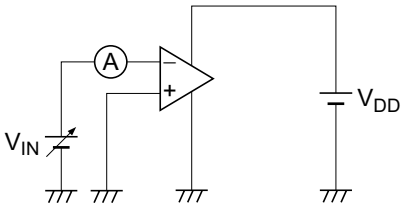


V_{DD}	Measure Point	Calculate V_{IO}	CMRR Calculation
2.7 V	V_{OUT1}	$V_{IO1} = V_{OUT1} / 1001$	$PSRR = \left\| 20\log_{10} \frac{\|[V_{IO2} - V_{IO1}]\|}{5.5\ V - 2.7\ V} \right\|$
5.5 V	V_{OUT2}	$V_{IO2} = V_{OUT2} / 1001$	

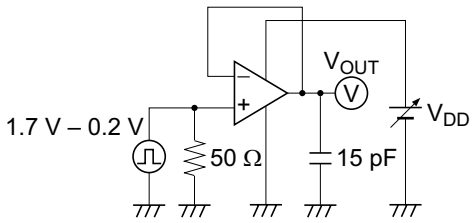
11. Input Bias Current, I_{IB+}

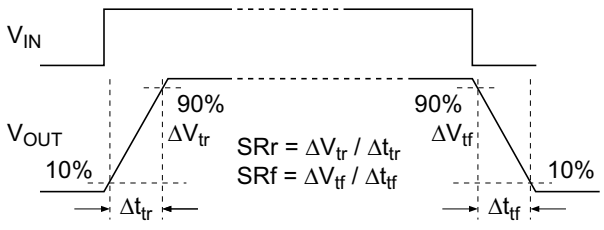


12. Input Bias Current, I_{IB-}



13. Slew Rate (Large Signal Input)

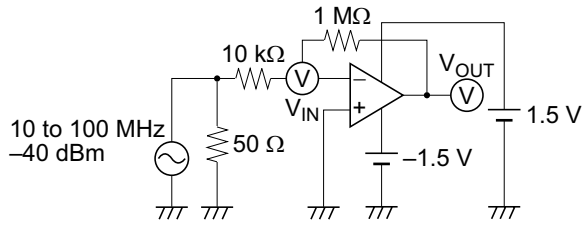




Test Circuits (cont.)

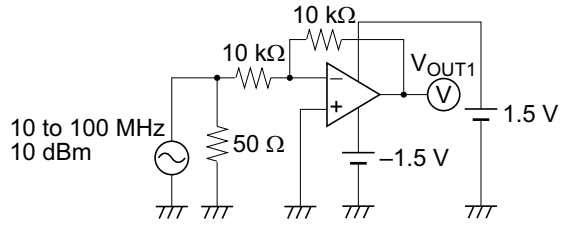
(Unless otherwise noted, V_{DD} = 3 V, V_{SS} = 0 V, Ta = 25°C)

14. Open Loop Voltage Gain, A_V

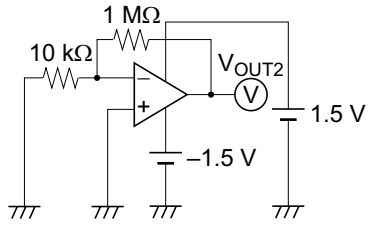


$$A_V = \left| 20\log_{10} \frac{101 \times |V_{OUT}|}{|V_{IN}|} \right|$$

15. Channel Separation, CS



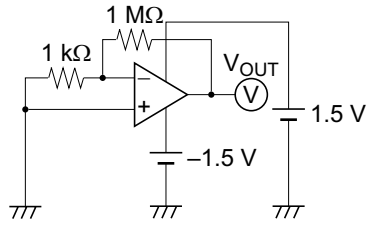
Channel 1



Channel 2

$$CS = \left| 20\log_{10} \frac{101 \times |V_{OUT2}|}{|V_{OUT1}|} \right|$$

16. Noise Input Voltage, VNI



$$VNI = \frac{V_{OUT}}{1001}$$

Characteristic Curves

Figure 1 HA1630D07
Supply Current vs. Supply Voltage

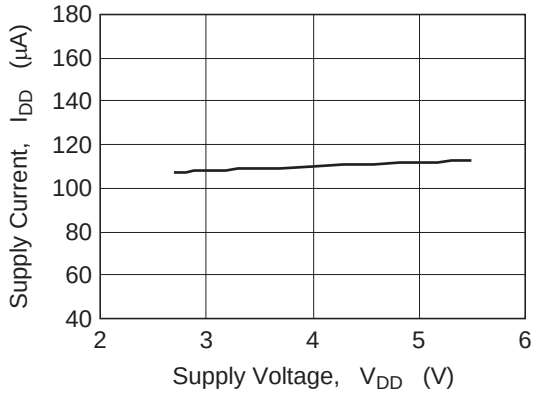


Figure 2 HA1630D07
Supply Current vs. Ambient Temperature

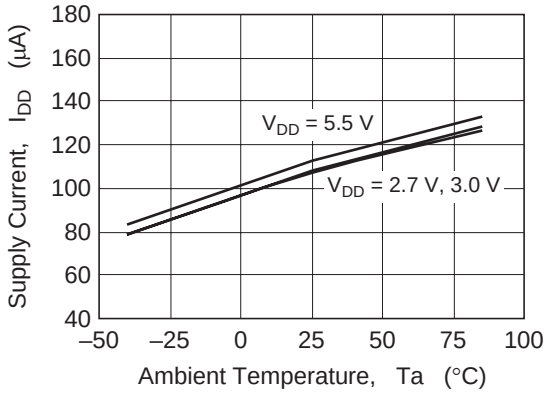


Figure 3 HA1630D07
Output High Voltage vs. Resistor Load

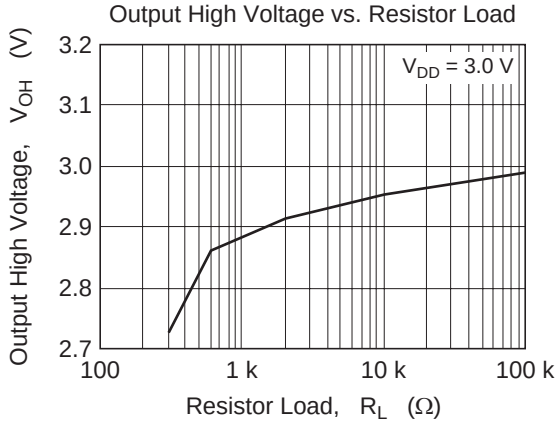


Figure 4 HA1630D07
Output Low Voltage vs. Resistor Load

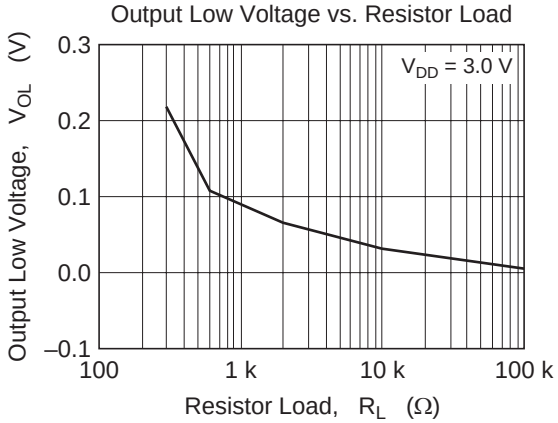


Figure 5 HA1630D07
Output High Voltage vs. Output Source Current

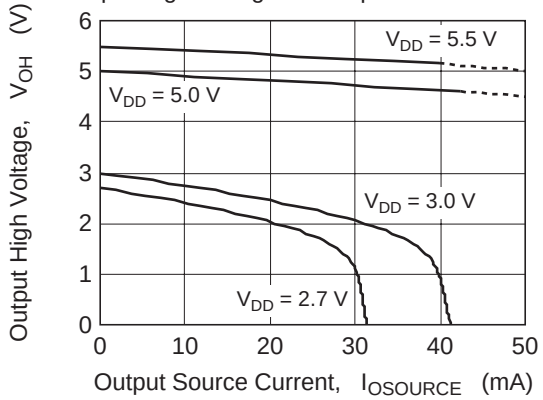
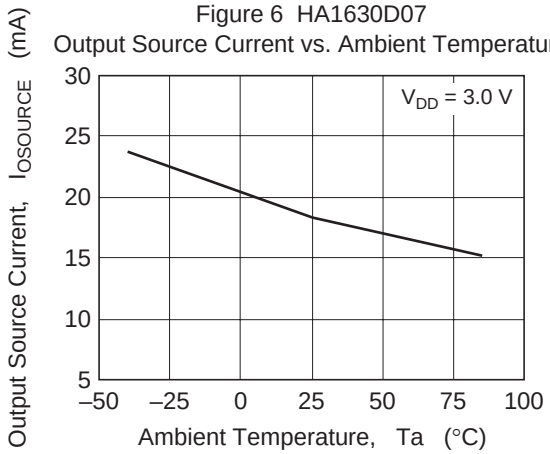


Figure 6 HA1630D07
Output Source Current vs. Ambient Temperature



Characteristic Curves (cont.)

Figure 7 HA1630D07
Output Low Voltage vs. Output Sink Current

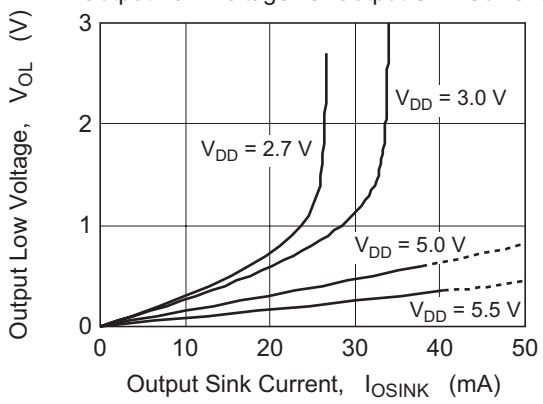


Figure 8 HA1630D07
Output Sink Current vs. Ambient Temperature

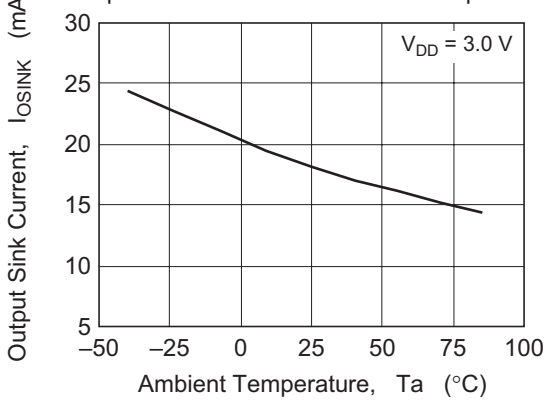


Figure 9 HA1630D07
Input Offset Voltage vs. Supply Voltage

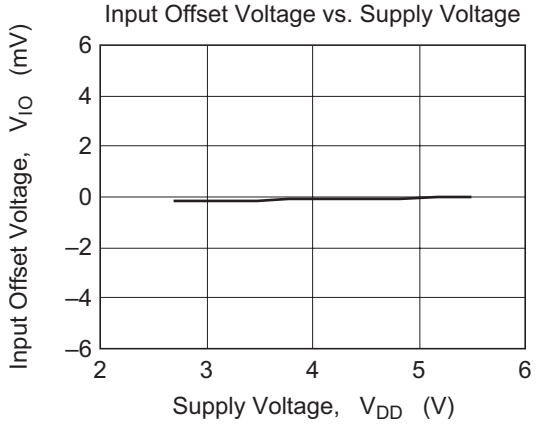


Figure 10 HA1630D07
Input Offset Voltage vs. Input Voltage

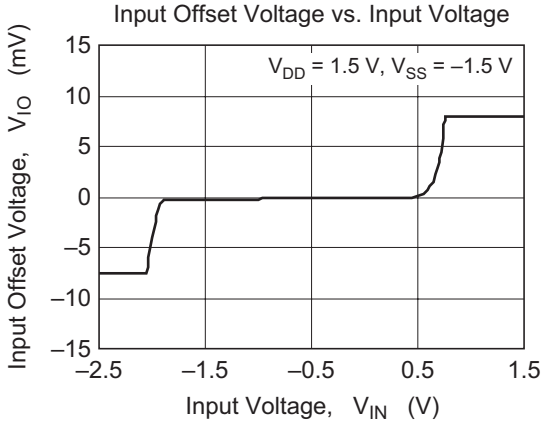


Figure 11 HA1630D07
Input Offset Voltage vs. Ambient Temperature

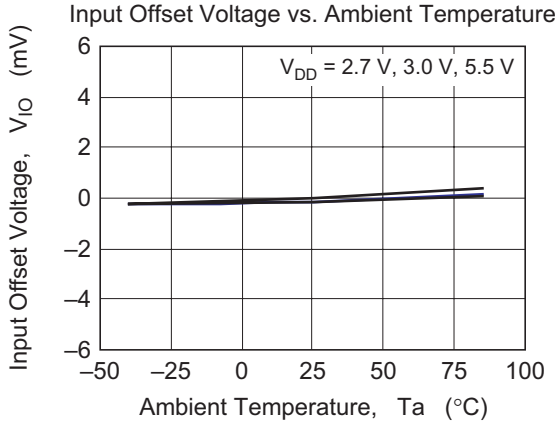
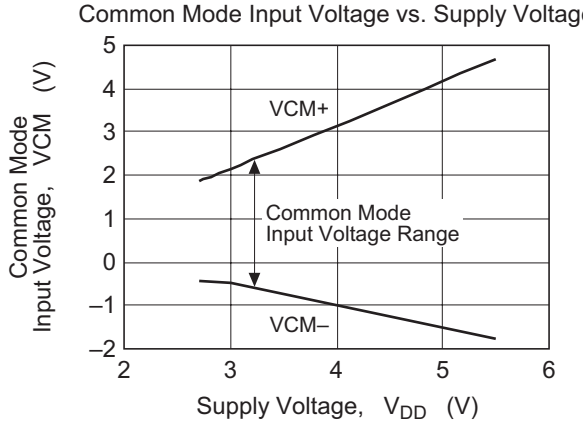


Figure 12 HA1630D07
Common Mode Input Voltage vs. Supply Voltage



Characteristic Curves (cont.)

Figure 13 HA1630D07
Common Mode Input Voltage vs. Ambient Temperature

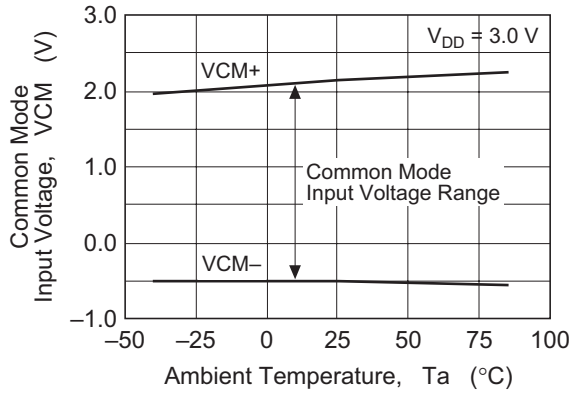


Figure 14 HA1630D07
Common Mode Rejection Ratio vs. Input Voltage

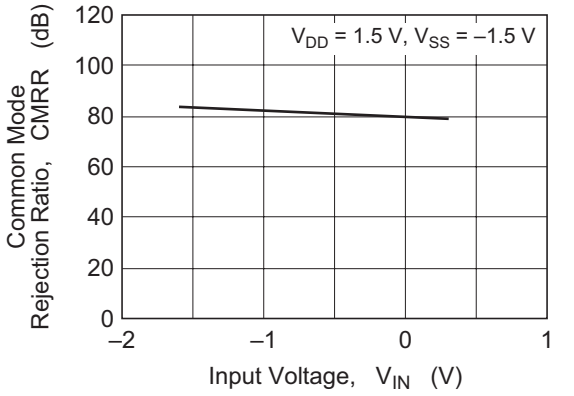


Figure 15 HA1630D07
Power Supply Rejection Ratio vs. Supply Voltage

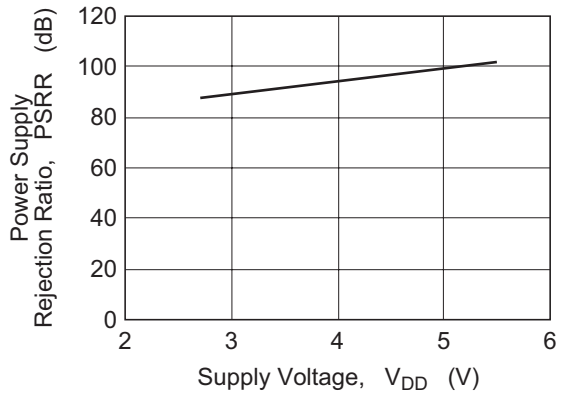


Figure 16 HA1630D07
Input Bias Current vs. Input Voltage

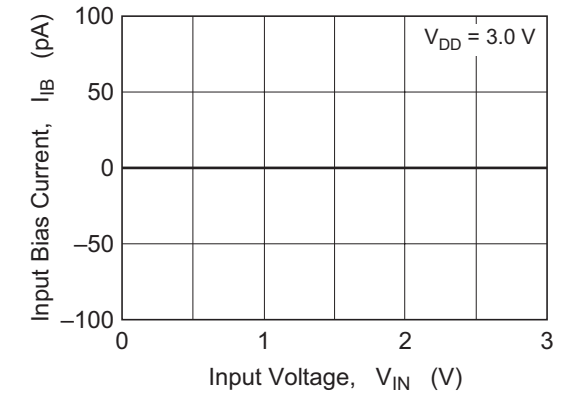


Figure 17 HA1630D07
Input Bias Current vs. Ambient Temperature

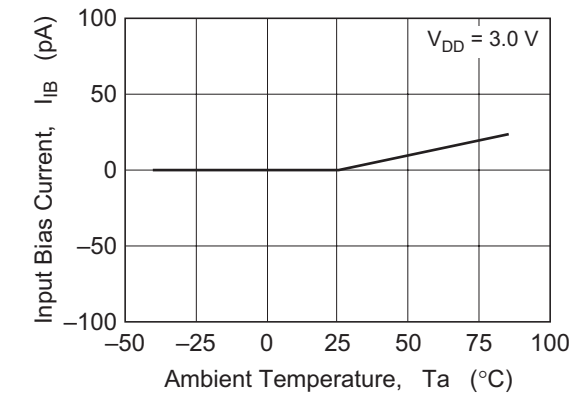
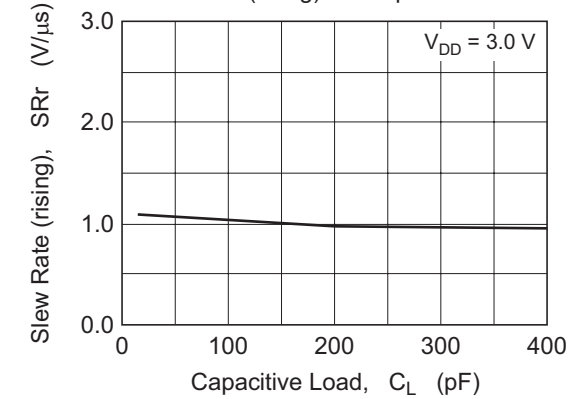


Figure 18 HA1630D07
Slew Rate (rising) vs. Capacitive Load



Characteristic Curves (cont.)

Figure 19 HA1630D07
Slew Rate (rising) vs. Ambient Temperature

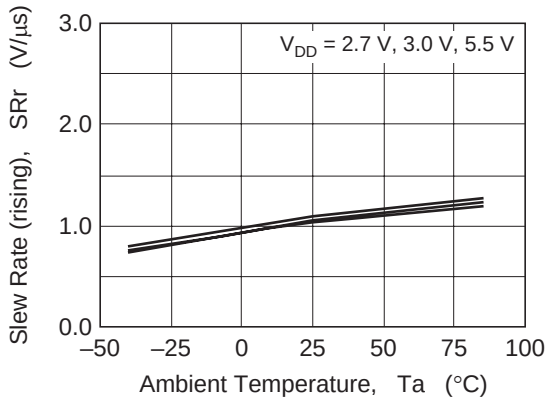


Figure 20 HA1630D07
Slew Rate (rising)

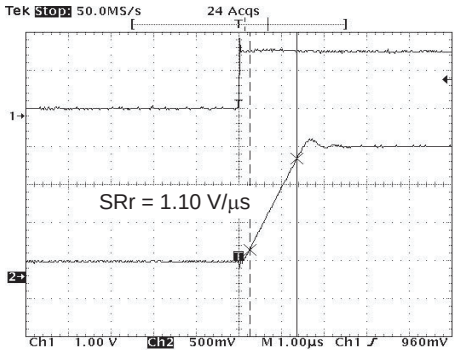


Figure 21 HA1630D07
Slew Rate (falling) vs. Capacitive Load

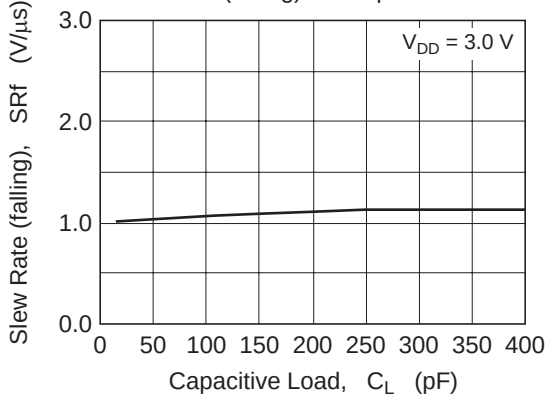


Figure 22 HA1630D07
Slew Rate (falling) vs. Ambient Temperature

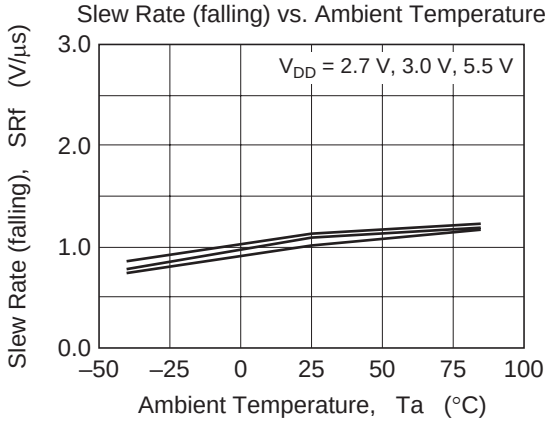


Figure 23 HA1630D07
Slew Rate (falling)

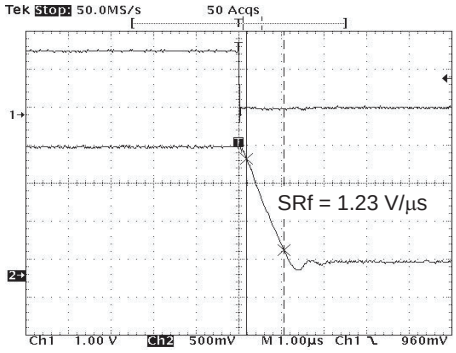
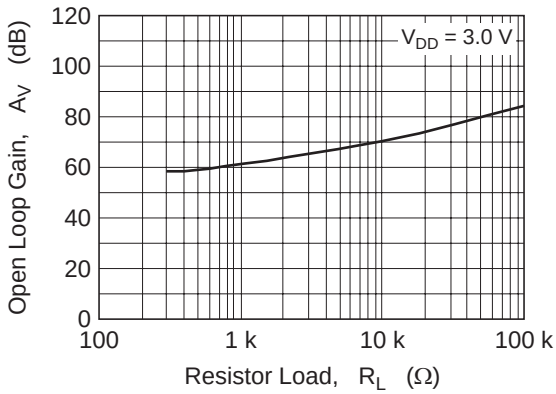


Figure 24 HA1630D07
Open Loop Gain vs. Resistor Load



Characteristic Curves (cont.)

Figure 25 HA1630D07
Open Loop Gain, Phase vs. Frequency

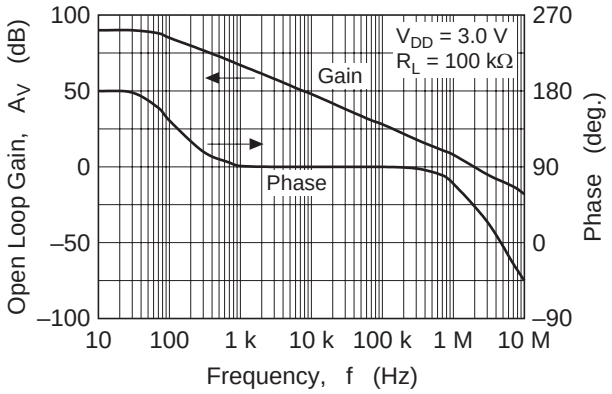


Figure 26 HA1630D07
Open Loop Gain, Phase vs. Frequency

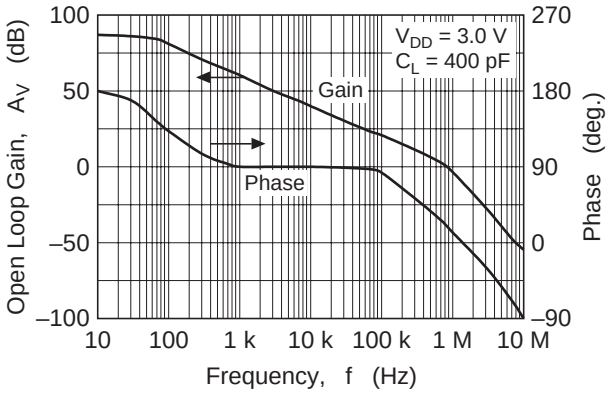


Figure 27 HA1630D07
Phase Margin vs. Capacitive Load

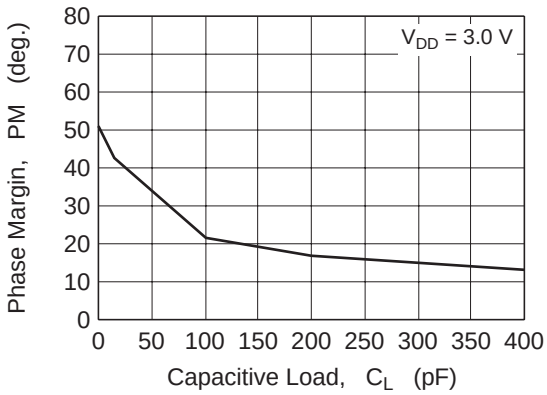


Figure 28 HA1630D07
Channel Separation vs. Frequency

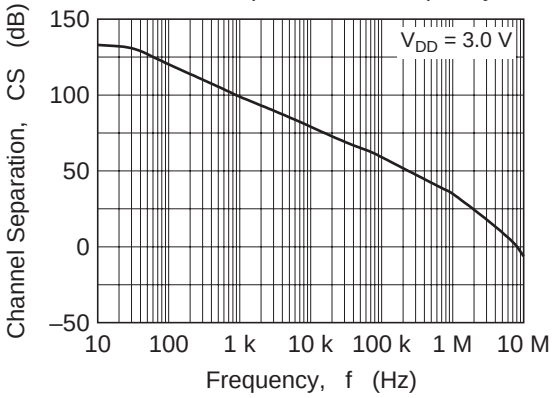
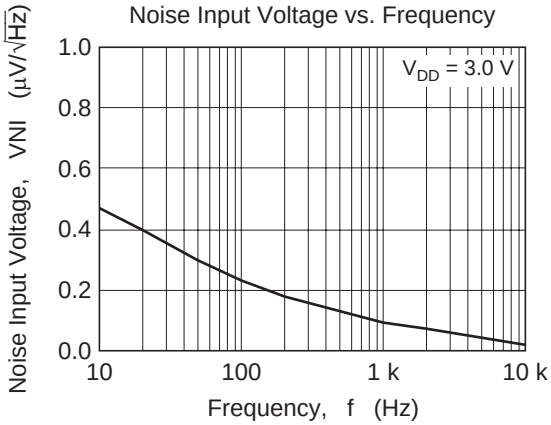


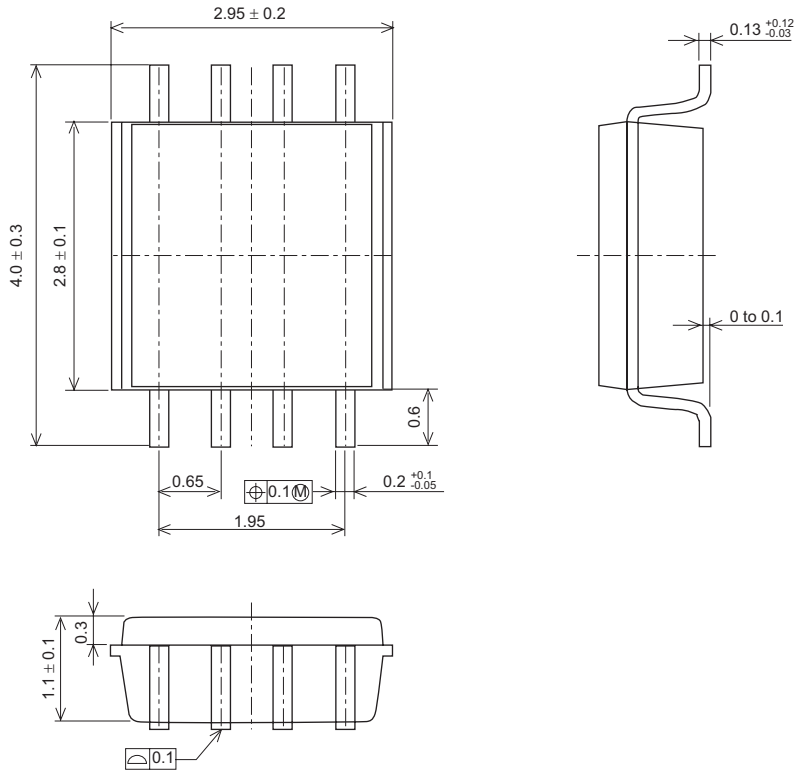
Figure 29 HA1630D07
Noise Input Voltage vs. Frequency



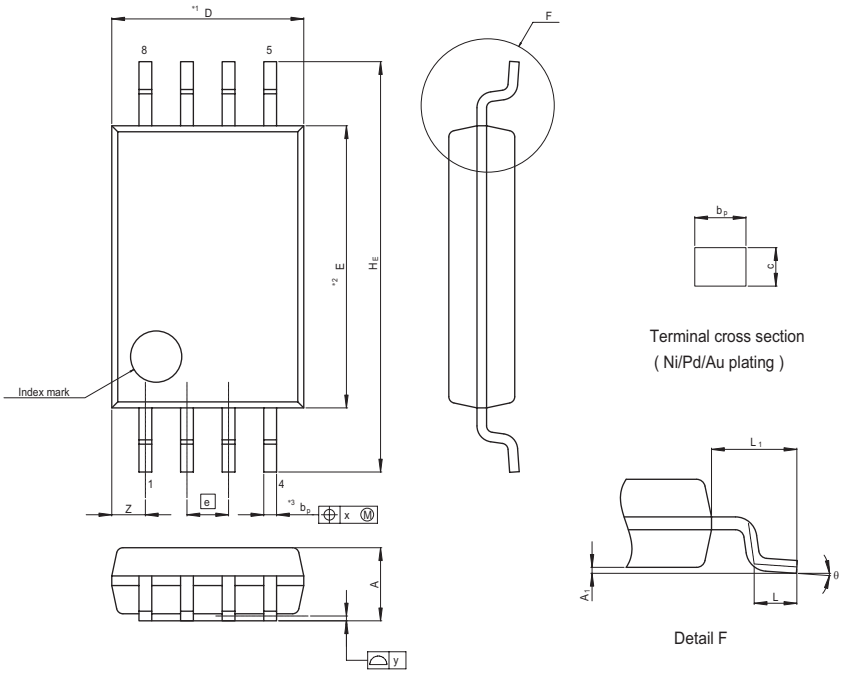
Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
MMPAK-8	P-LSOP8-2.8 x 2.95 - 0.65	PLSP0008JC-A	—	0.02 g

Unit: mm



JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP8-4.4x3-0.65	PTSP0008JC-B	TTP-8DAV	0.034g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

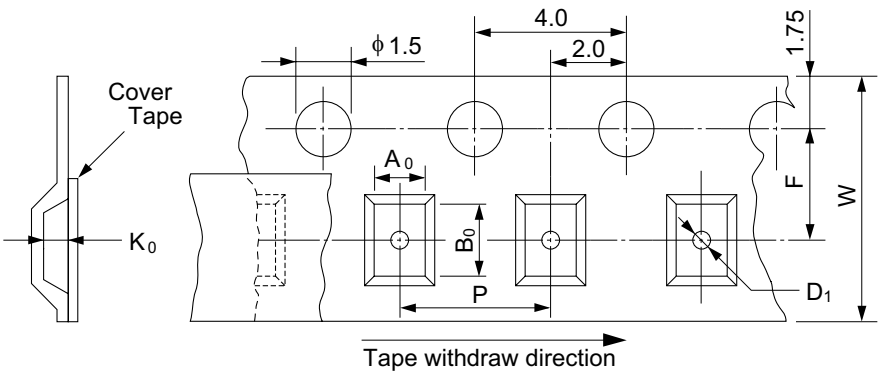
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	3.00	3.30
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.805
L	0.40	0.50	0.60
L_1	—	1.00	—

Taping & Reel Specification

[Taping]

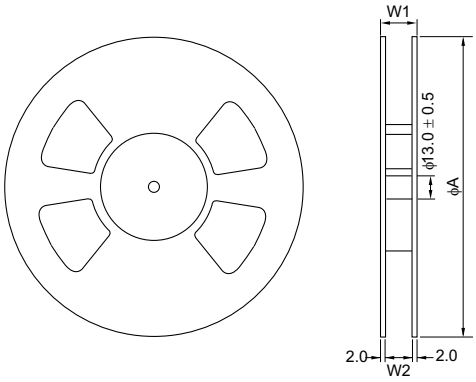
Package Code	W	P	Ao	Bo	Ko	E	F	D1	Maximum Storage No.
TSSOP-8	12	8	6.9	3.6	1.7	1.75	5.5	1.5	3,000 pcs/reel
MMPAK-8	12	4.0	3.15	4.35	—	—	5.5	1.05	3,000 pcs/reel

Unit: mm



[Reel]

Package	Tape width	W1	W2	A
TSSOP-8	12	17.4	13.4	330
MMPAK-8	12	17.0	13.0	178

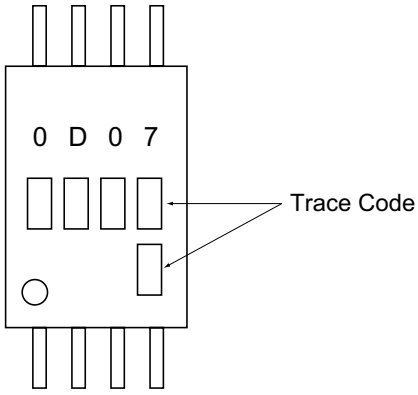


[Ordering Information]

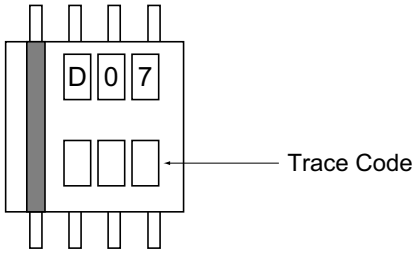
Ordering Unit
3,000 pcs

Mark Indication

• TSSOP-8



• MMPAK-8



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Colophon .7.2