

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ C6 600V

600V CoolMOS™ C6 Power Transistor
IPx60R160C6

Data Sheet

Rev. 2.2
Final

600V CoolMOS™ C6 Power Transistor

IPA60R160C6, IPB60R160C6
IPP60R160C6 IPW60R160C6

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ C6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The offered devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter, and cooler.

Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- JEDEC¹⁾ qualified, Pb-free plating, Halogen free

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

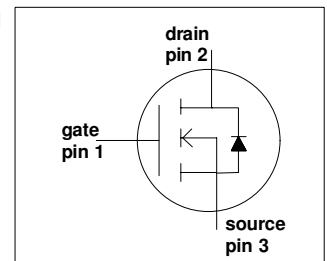


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	0.16	Ω
$Q_{g,typ}$	75	nC
$I_{D,pulse}$	70	A
$E_{oss} @ 400V$	6	μJ
Body diode di/dt	500	A/ μs

Type / Ordering Code	Package	Marking	Related Links
IPW60R160C6	PG-TO247	6R160C6	IFX C6 Product Brief IFX C6 Portfolio IFX CoolMOS Webpage IFX Design tools
IPB60R160C6	PG-TO263		
IPP60R160C6	PG-TO220		
IPA60R160C6	PG-TO220 FullPAK		

1) J-STD20 and JESD22

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2 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	23.8	A	$T_C = 25\text{ °C}$
				15		$T_C = 100\text{ °C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	70	A	$T_C = 25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	497	mJ	$I_D = 4.1\text{ A}, V_{DD} = 50\text{ V}$ (see table 21)
Avalanche energy, repetitive	E_{AR}	-	-	0.75		$I_D = 4.1\text{ A}, V_{DD} = 50\text{ V}$
Avalanche current, repetitive	I_{AR}	-	-	4.1	A	
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 480\text{ V}$
Gate source voltage	V_{GS}	-20	-	20	V	static
		-30		30		AC ($f > 1\text{ Hz}$)
Power dissipation for TO-220, TO-247, TO-263	P_{tot}	-	-	176	W	$T_C = 25\text{ °C}$
Power dissipation for TO-220 FullPAK	P_{tot}	-	-	34		
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	
Mounting torque TO-220, TO-247		-	-	60	Ncm	M3 and M3.5 screws
Mounting torque TO-220 FullPAK				50		M2.5 screws
Continuous diode forward current	I_S	-	-	20.6	A	$T_C = 25\text{ °C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	70	A	$T_C = 25\text{ °C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{ V}, I_{SD} \leq I_D,$ $T_j = 25\text{ °C}$
Maximum diode commutation speed ³⁾	di/dt			500	A/μs	

1) Limited by $T_{j,max}$. Maximum duty cycle $D = 0.75$

2) Pulse width t_p limited by $T_{j,max}$

3) Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics TO-220 (IPP60R160C6), TO-247 (IPW60R160C6)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.71	°C/W	leaded
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 4 Thermal characteristics TO-220FullPAK (IPA60R160C6)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.67	°C/W	leaded
Thermal resistance, junction - ambient	R_{thJA}	-	-	80		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 5 Thermal characteristics TO-263 (IPB60R160C6)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.71	°C/W	SMD version, device on PCB, minimal footprint
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		
		-	35	-		
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

1) Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

Electrical characteristics, at $T_J=25\text{ °C}$, unless otherwise specified.

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0\text{ V}$, $I_D=0.25\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5		$V_{DS}=V_{GS}$, $I_D=0.75\text{ mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_J=25\text{ °C}$
		-	10	-		$V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_J=150\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.14	0.16	Ω	$V_{GS}=10\text{ V}$, $I_D=11.3\text{ A}$, $T_J=25\text{ °C}$
		-	0.37	-		$V_{GS}=10\text{ V}$, $I_D=11.3\text{ A}$, $T_J=150\text{ °C}$
Gate resistance	R_G	-	6.4	-	Ω	$f=1\text{ MHz}$, open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1660	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	100	-		
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	66	-		$V_{GS}=0\text{ V}$, $V_{DS}=0\dots480\text{ V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	314	-		$I_D=\text{constant}$, $V_{GS}=0\text{ V}$ $V_{DS}=0\dots480\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	$V_{DD}=400\text{ V}$, $V_{GS}=13\text{ V}$, $I_D=11.3\text{ A}$, $R_G=1.7\Omega$ (see table 20)
Rise time	t_r	-	13	-		
Turn-off delay time	$t_{d(off)}$	-	96	-		
Fall time	t_f	-	8	-		

1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	9	-	nC	$V_{DD}=480\text{ V}$, $I_D=11.3\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	38	-		
Gate charge total	Q_g	-	75	-		
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	

Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0\text{ V}$, $I_F=11.3\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	460	-	ns	$V_R=400\text{ V}$, $I_F=11.3\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$ (see table 22)
Reverse recovery charge	Q_{rr}	-	8.2	-	μC	
Peak reverse recovery current	I_{rrm}	-	35	-	A	

5 Electrical characteristics diagrams

Table 10

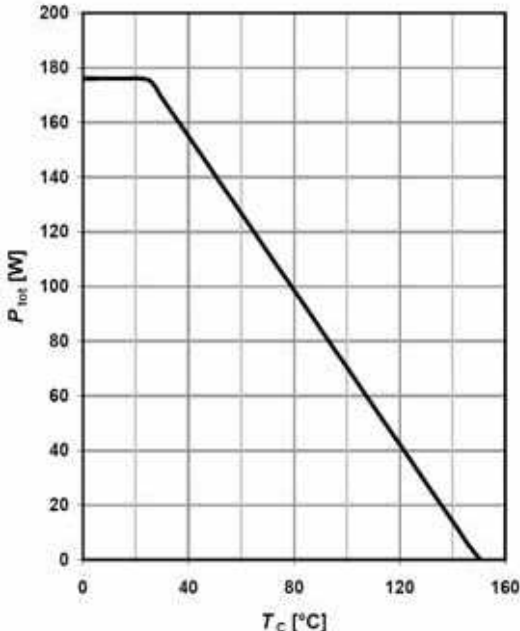
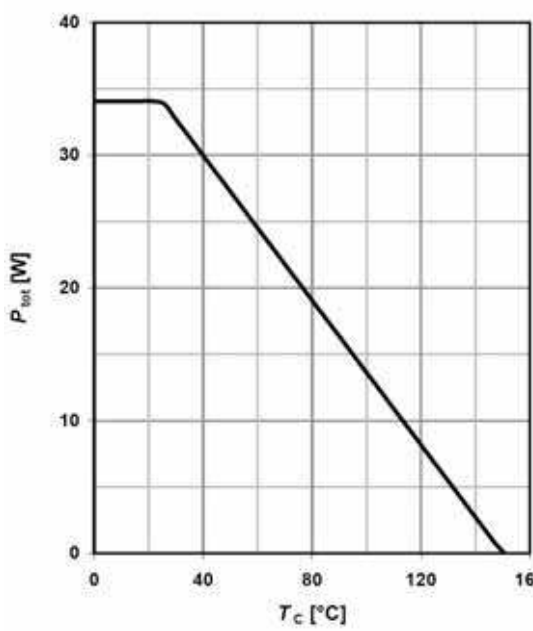
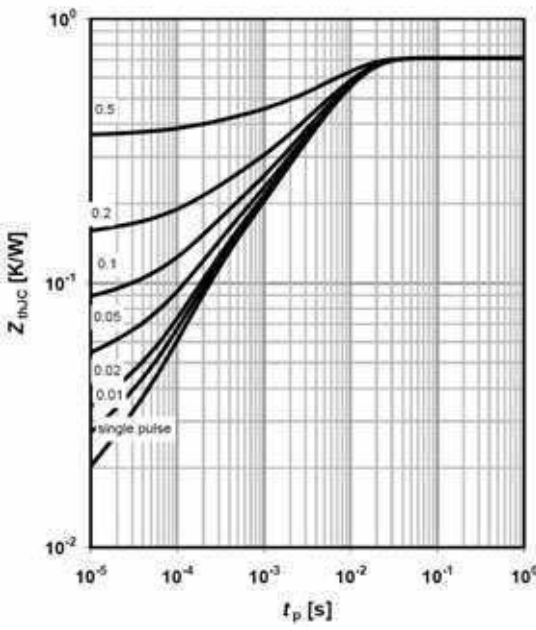
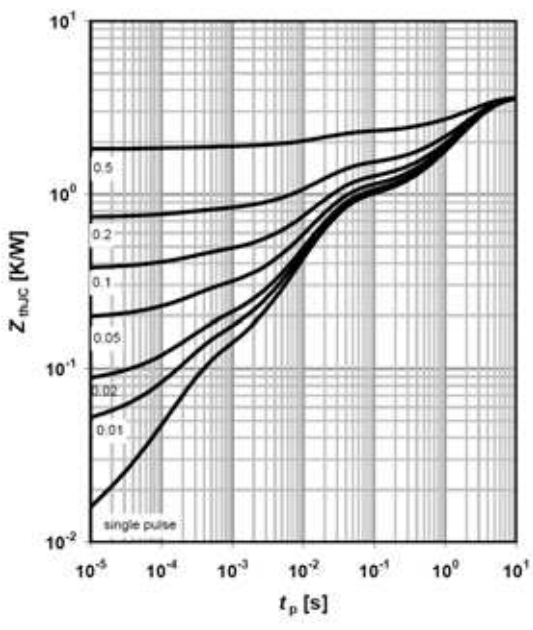
Power dissipation TO-220, TO-247, TO-263	Power dissipation TO-220 FullPAK
	
$P_{tot} = f(T_C)$	$P_{tot} = f(T_C)$

Table 11

Max. transient thermal impedance TO-220, TO-247, TO-263	Max. transient thermal impedance TO-220 FullPAK
	
$Z_{(thJC)} = f(t_p)$; parameter: $D = t_p / T$	$Z_{(thJC)} = f(t_p)$; parameter: $D = t_p / T$

Electrical characteristics diagrams

Table 12

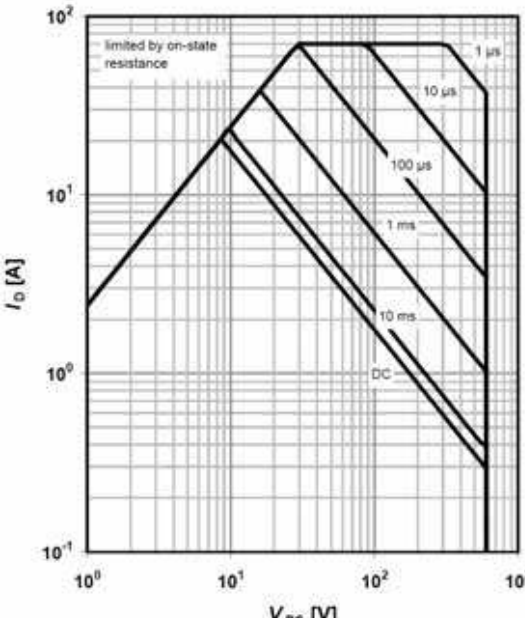
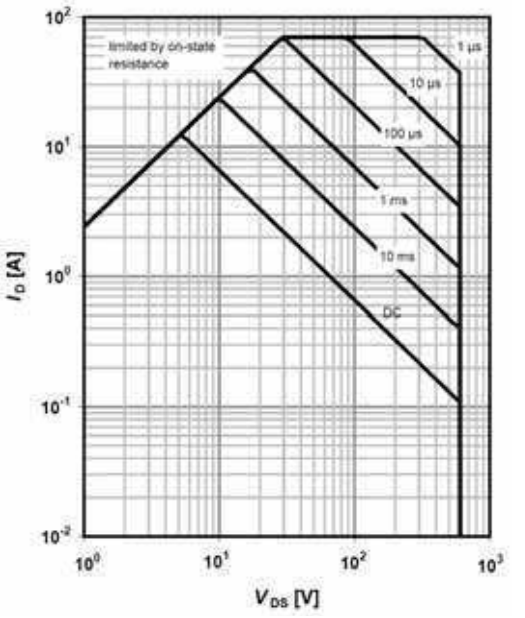
Safe operating area $T_C=25\text{ °C}$ TO-220, TO-247, TO-263	Safe operating area $T_C=25\text{ °C}$ TO-220 FullPAK
	
$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0; \text{parameter } t_p$	$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0; \text{parameter } t_p$

Table 13

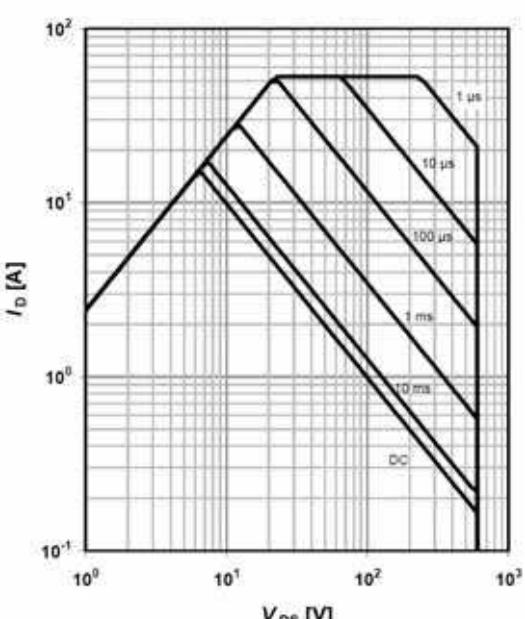
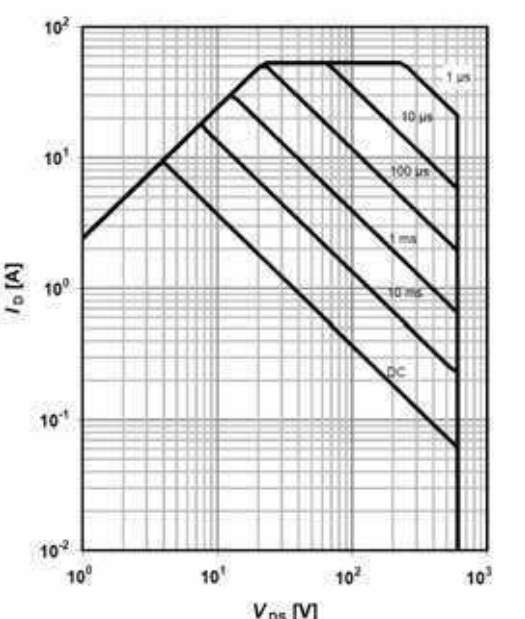
Safe operating area $T_C=80\text{ °C}$ TO-220, TO-247, TO-263	Safe operating area $T_C=80\text{ °C}$ TO-220 FullPAK
	
$I_D=f(V_{DS}); T_C=80\text{ °C}; D=0; \text{parameter } t_p$	$I_D=f(V_{DS}); T_C=80\text{ °C}; D=0; \text{parameter } t_p$

Table 14

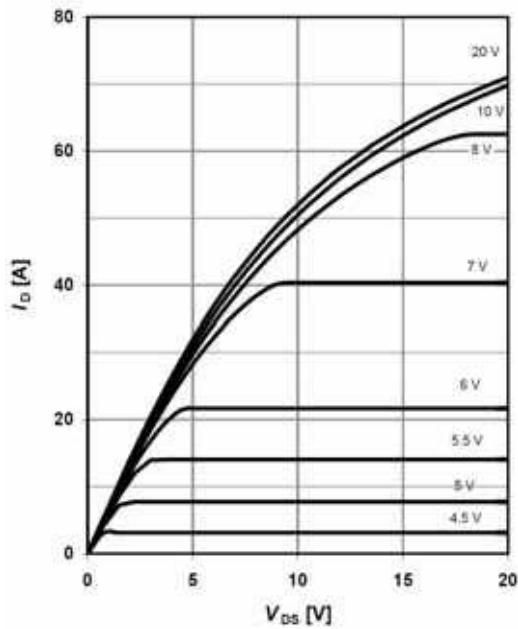
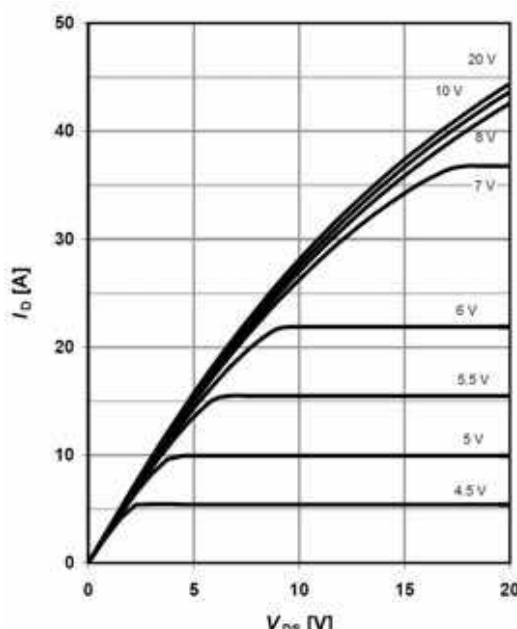
Typ. output characteristics $T_c=25\text{ °C}$	Typ. output characteristics $T_j=125\text{ °C}$
	
$I_D=f(V_{DS}); T_j=25\text{ °C}; \text{parameter: } V_{GS}$	$I_D=f(V_{DS}); T_j=125\text{ °C}; \text{parameter: } V_{GS}$

Table 15

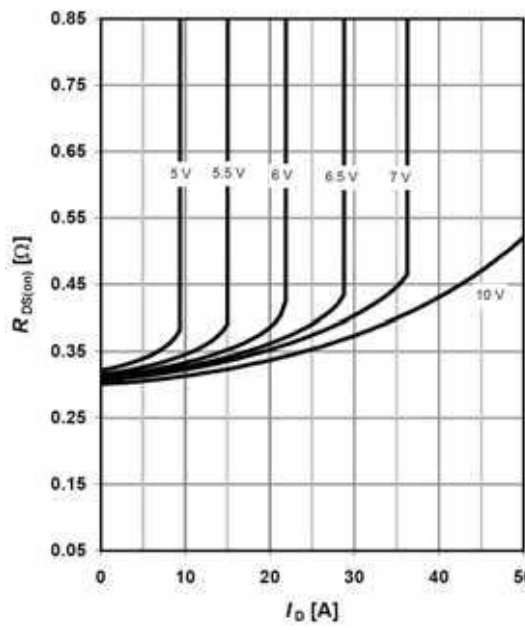
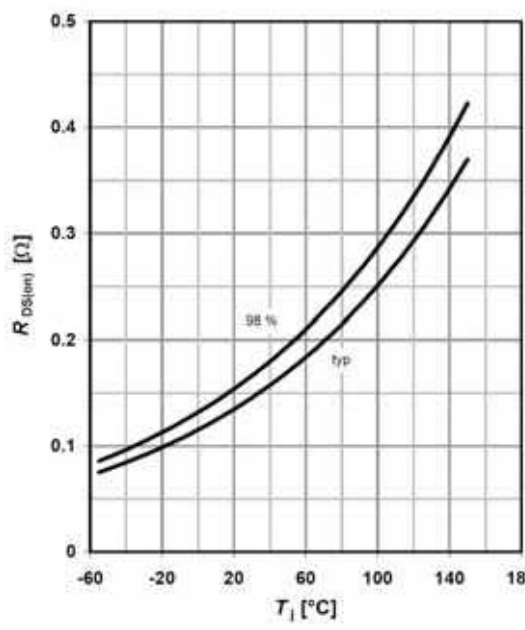
Typ. drain-source on-state resistance	Drain-source on-state resistance
	
$R_{DS(on)}=f(I_D); T_j=125\text{ °C}; \text{parameter: } V_{GS}$	$R_{DS(on)}=f(T_j); I_D=11.3\text{ A}; V_{GS}=10\text{ V}$

Table 16

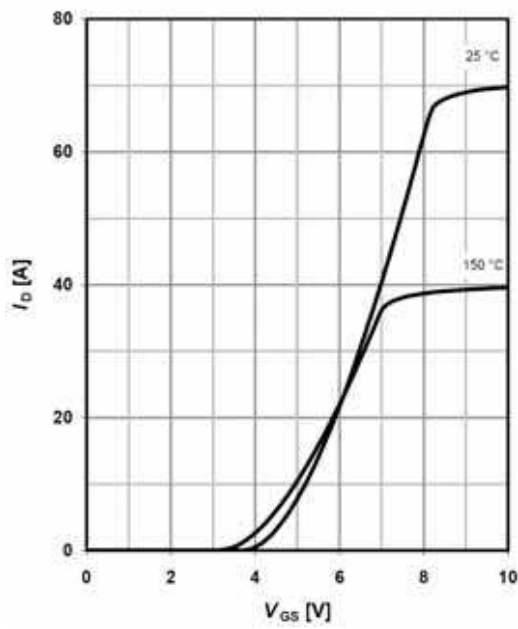
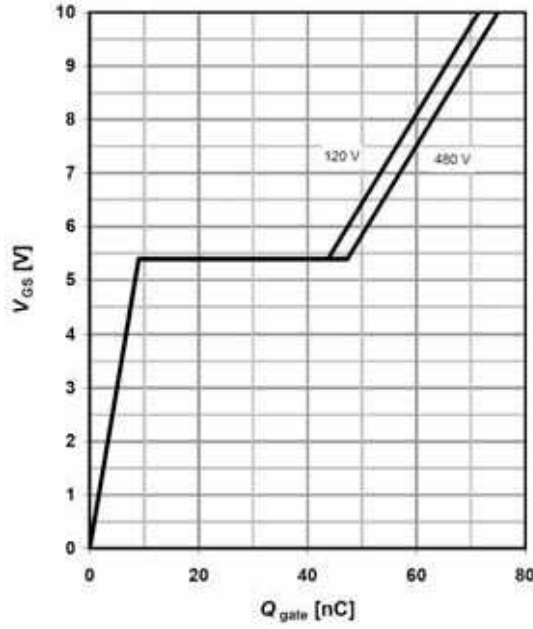
Typ. transfer characteristics	Typ. gate charge
	
$I_D = f(V_{GS}); V_{DS} = 20V$	$V_{GS} = f(Q_{gate}), I_D = 11.3 A \text{ pulsed}$

Table 17

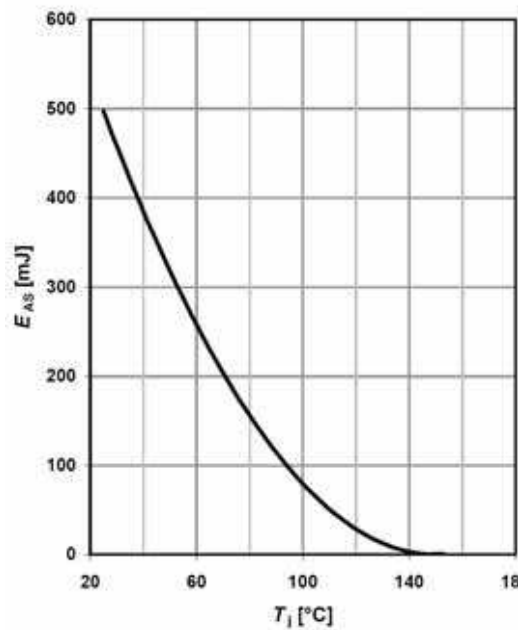
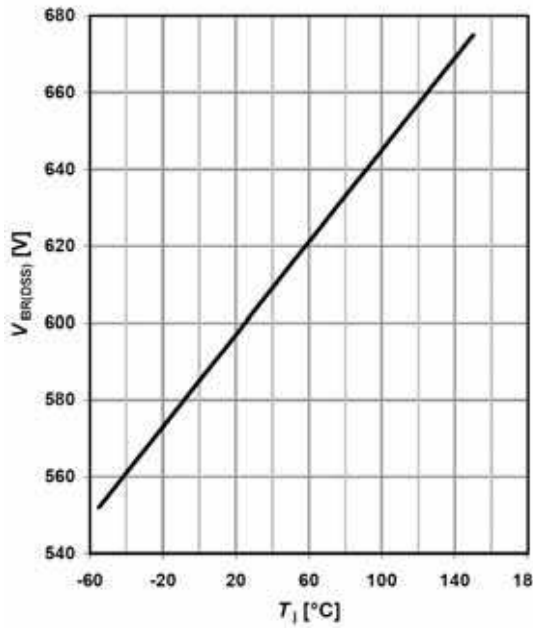
Avalanche energy	Drain-source breakdown voltage
	
$E_{AS} = f(T_i); I_D = 4.1 A; V_{DD} = 50 V$	$V_{BR(DSS)} = f(T_i); I_D = 0.25 mA$

Table 18

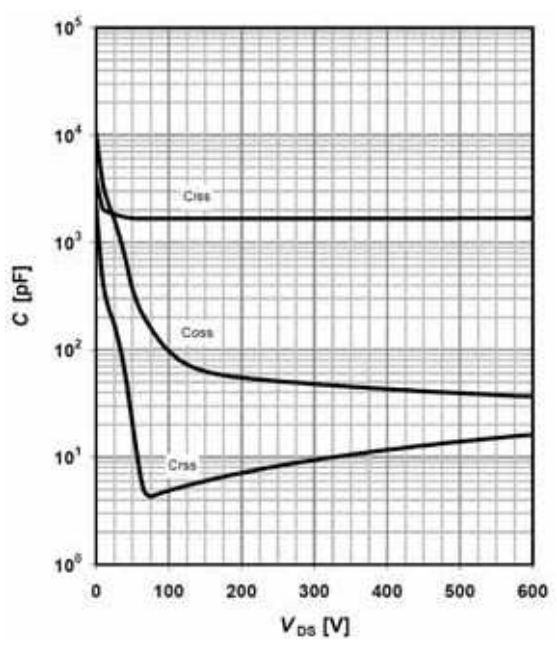
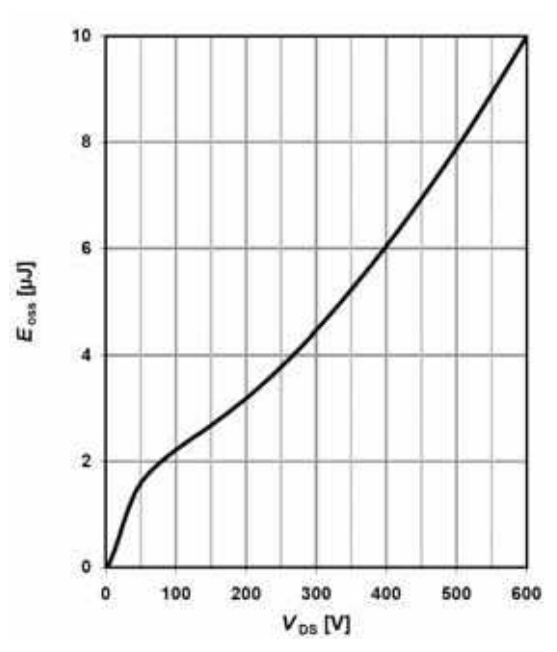
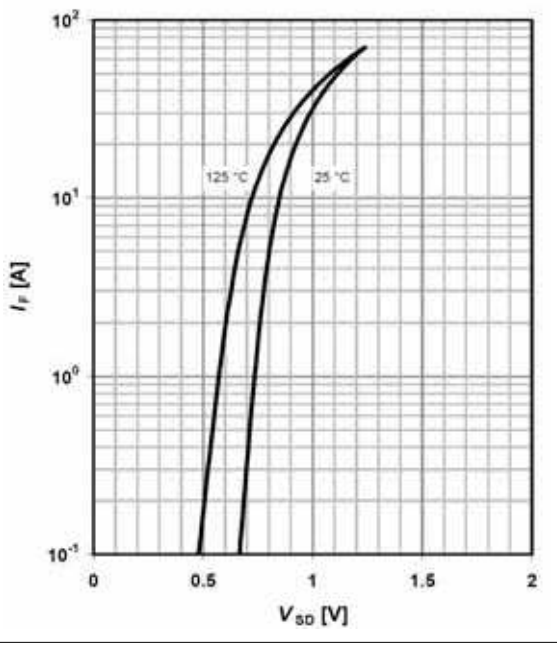
Typ. capacitances	Typ. C_{oss} stored energy
 $C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$	 $E_{oss} = f(V_{DS})$

Table 19

Forward characteristics of reverse diode
 $I_F = f(V_{SD}); \text{parameter: } T_j$

6 Test circuits

Table 20 Switching times test circuit and waveform for inductive load

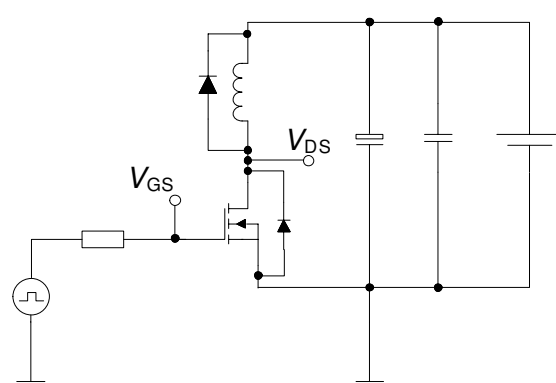
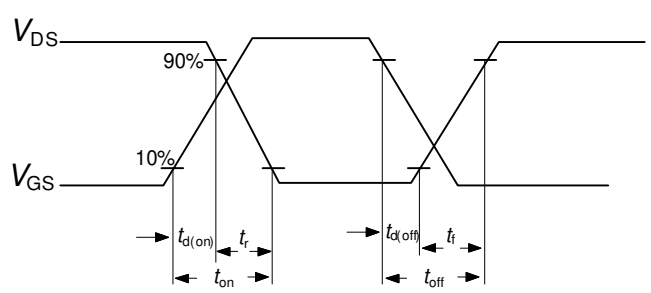
Switching times test circuit for inductive load	Switching time waveform
	

Table 21 Unclamped inductive load test circuit and waveform

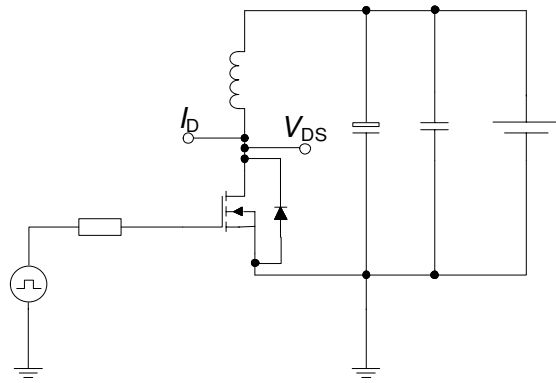
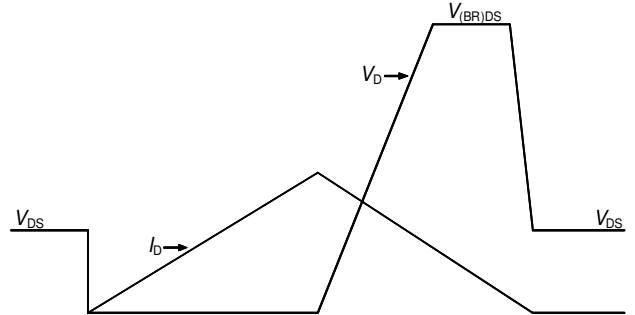
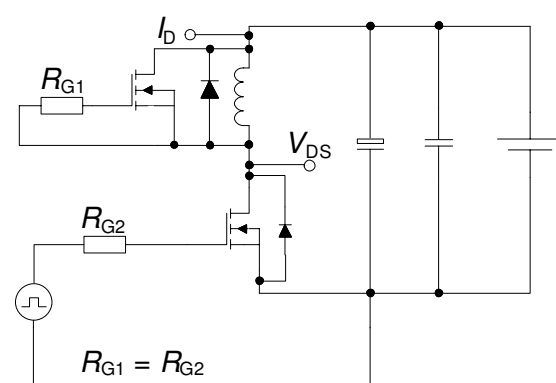
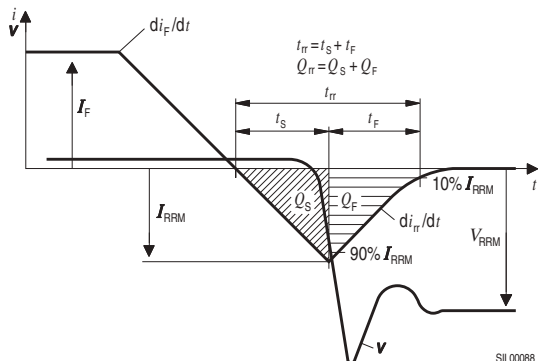
Unclamped inductive load test circuit	Unclamped inductive waveform
	

Table 22 Test circuit and waveform for diode recovery times

Test circuit for diode recovery times	Diode recovery waveform
 $R_{G1} = R_{G2}$	 $i_n = t_s + t_F$ $Q_n = Q_S + Q_F$ $10\% I_{RRM}$ $90\% I_{RRM}$ V_{RRM} SIL00088

7 Package outlines

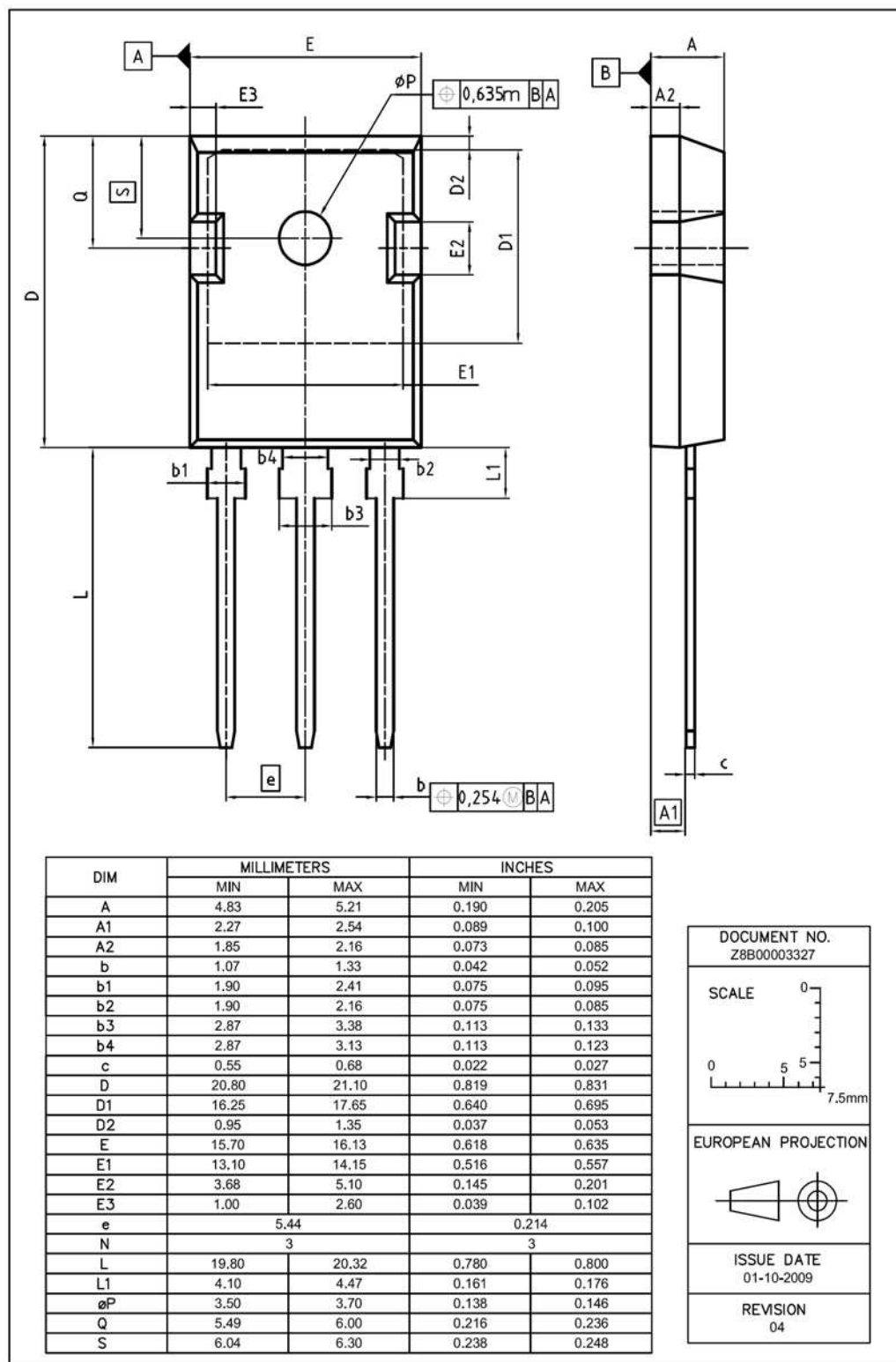
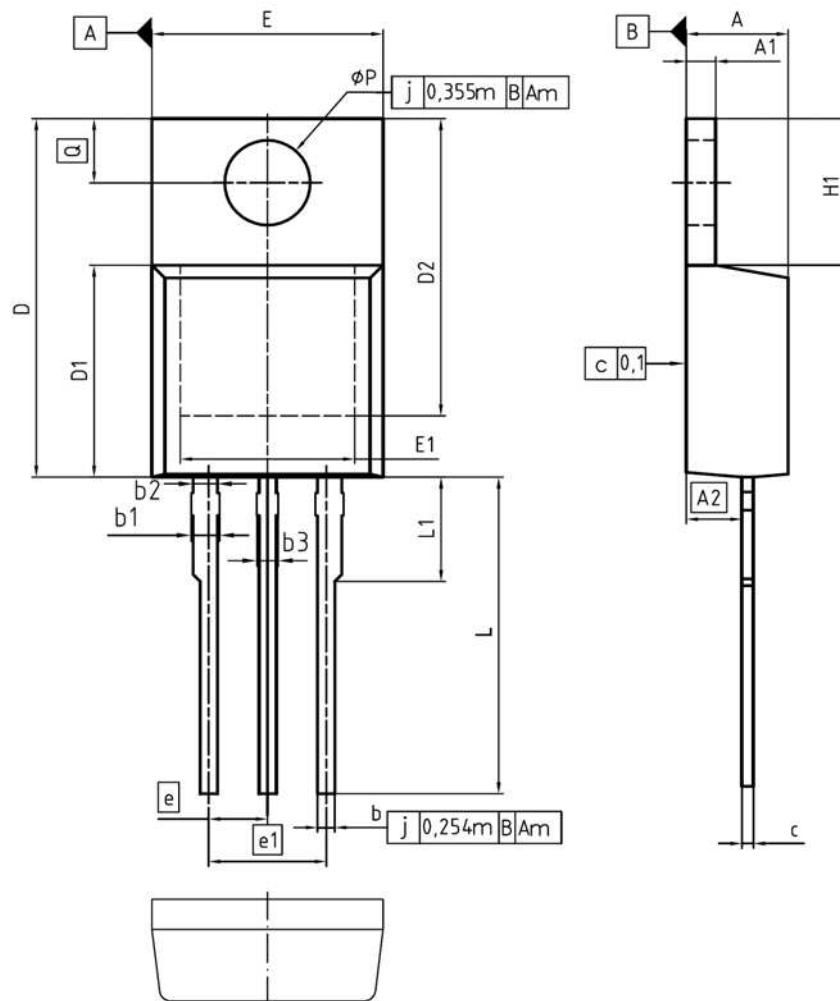


Figure 1 Outlines TO-247, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

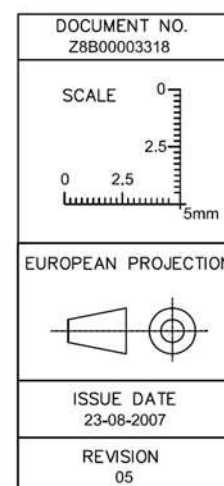
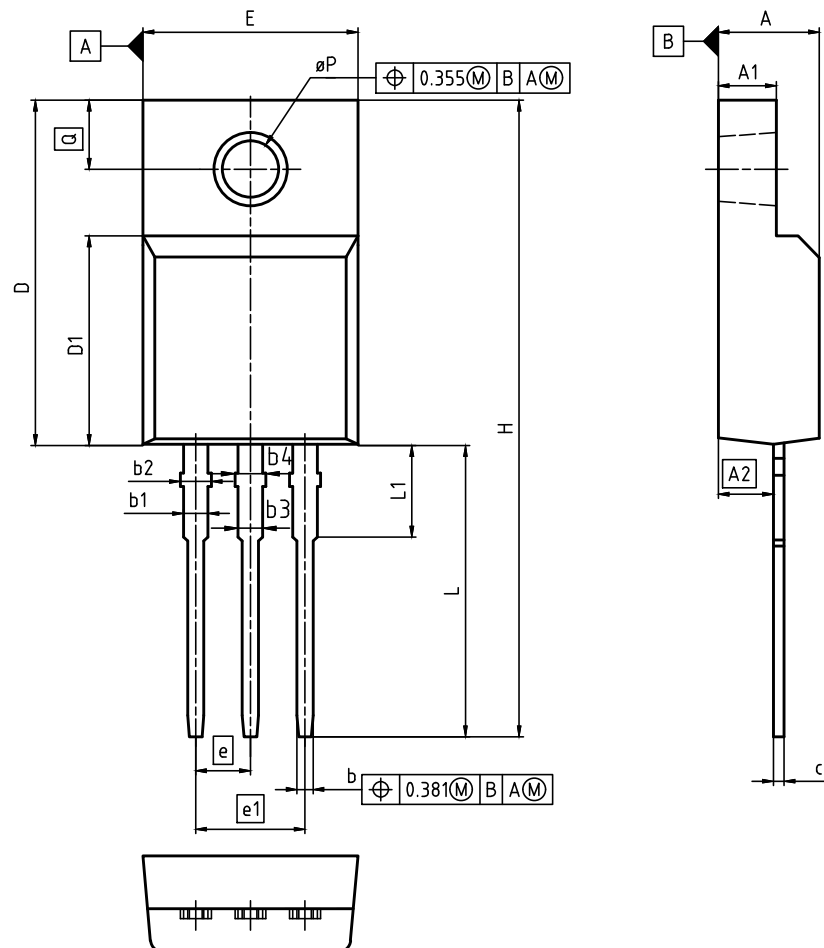


Figure 2 Outlines TO-220, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

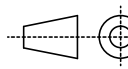
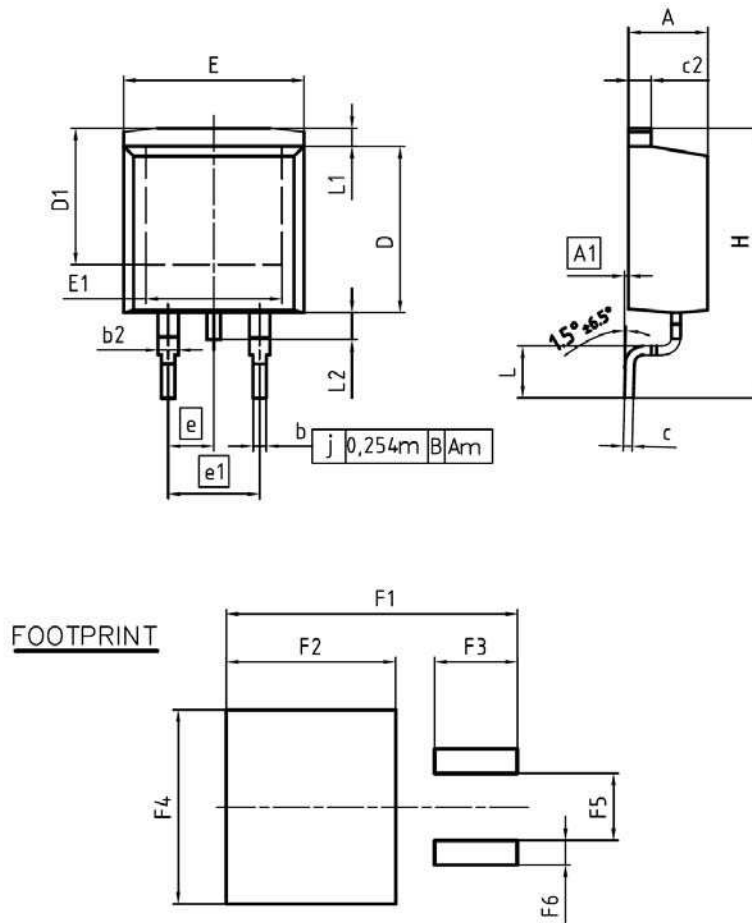
DOCUMENT NO. Z8B00003319
SCALE 0 2.5 5mm
EUROPEAN PROJECTION 
ISSUE DATE 05-05-2014
REVISION 04

Figure 3 Outline PG-TO 220 FullPAK, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	2		2	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	3.65	3.85	0.144	0.152
F6	1.25	1.45	0.049	0.057

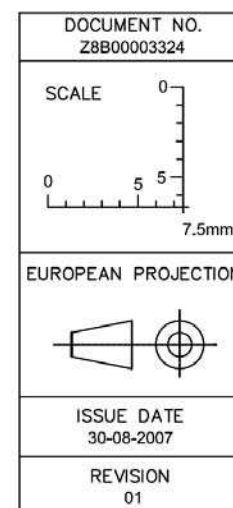


Figure 4 Outlines TO-263, dimensions in mm/inches

Revision History

IPx60R160C6

Revision: 2015-02-03, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2011-06-08	Release of final data sheet
2.1	2011-09-14	-
2.2	2015-02-03	PG-TO220 FullPAK package outline update (creation:2014-12-02)

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Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

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