Numbers in parenthesis denote pin numbers for F package (Case 650).

FUNCTIONS AND CHARACTERISTICS (continued)

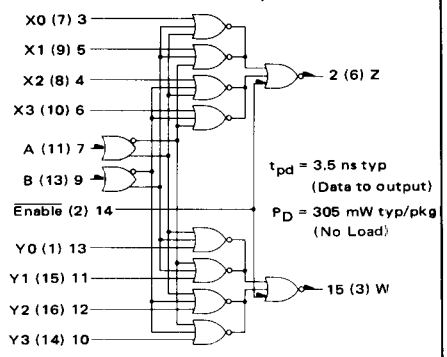
Function	Type ①		Propagation Delay ns typ	Power Dissipation mW typ/pkg*	Case
	-30 to +85°C	-55 to +125°C			
Universal Decade Counter	MC10137	MC10537	f = 150 MHz	625	620,650
Bi-Quinary Counter	MC10138	–	f = 150 MHz	370	620
64-Bit Random Access Memory (90 Ω)	MCM10140	–	t_{Access} = 15 (max)	420	620,690
Four-Bit Universal Shift Register	MC10141	MC10541	f = 200 MHz	425	620,648,650
64-Bit Random Access Memory (50 Ω)	MCM10142	–	t_{Access} = 10 (max)	420	620
8 x 2 Multiport Register File (RAM)	MCM10143	–	t_{Access} = 10	610	623
256-Bit Random Access Memory	MCM10144	–	t_{Access} = 30 (max)	420	620,690
64-Bit Register File (RAM)	MCM10145	–	t_{Access} = 10	625	620
128-Bit Random Access Memory	MCM10147	–	t_{Access} = 12 (max)	420	620
64-Bit Random Access Memory (50 Ω)	MCM10148	–	t_{Access} = 15 (max)	420	620
1024-Bit Programmable Read Only Memory	MCM10150	–	t_{Access} = 20	–	690
Quad Latch	MC10153	–	4.0	310	620
12-Bit Parity Generator-Checker	MC10160	MC10560	5.0	320	620,648,650
Binary to 1-8 Decoder (Low)	MC10161	MC10561	4.0	315	620,648,650
Binary to 1-8 Decoder (High)	MC10162	MC10562	4.0	315	620,648,650
Error Detection-Correction Circuit	MC10163	–	5.0	520	620
8-Line Multiplexer	MC10164	MC10564	3.0	310	620,648,650
8-Input Priority Encoder	MC10165	–	7.0	545	620,648
5-Bit Magnitude Comparator	MC10166	–	6.0	440	620
Quad Latch	MC10168	–	3.0	310	620
Dual Binary To 1-4 Decoder (Low)	MC10171	MC10571	4.0	325	620,648,650
Dual Binary To 1-4 Decoder (High)	MC10172	MC10572	4.0	325	620,648,650
Quad 2-Input Multiplexer/Latch	MC10173	–	2.5	275	620,648
Dual 4 To 1 Multiplexer	MC10174	MC10574	3.5	305	620,650
Quint Latch	MC10175	MC10575	2.5	400	620
Hex "D" Master-Slave Flip-Flop	MC10176	–	f = 250 MHz	460	620
Triple MECL to NMOS Translator	MC10177	–	–	1.0 W	620
Binary Counter	MC10178	–	f = 150 MHz	370	620
Look-Ahead Carry Block	MC10179	MC10579	3.0 (Cn,P) 4.0 (G)	300	620,648,650
Dual High Speed Adder/Subtractor	MC10180	MC10580	4.5	360	620,648,650
4-Bit Arithmetic Logic Unit/Function Generator	MC10181	MC10581	See Logic Diag.	600	623,649,652
2-Bit Arithmetic Logic Unit/Function Generator	MC10182	–	See Logic Diag.	575	620
Error Detection-Correction Circuit	MC10193	–	7.5	520	620
Hex Inverter/Buffer	MC10195	–	2.0	200	620
Hex "AND" Gate	MC10197	–	2.8	200	620
High Speed Dual 3-Input 3-Output OR Gate	MC10210	–	1.5	160	620
High Speed Dual 3-Input 3-Output NOR Gate	MC10211	–	1.5	160	620
High Speed Dual 3-Input 3-Output OR/NOR Gate	MC10212	–	1.5	160	620
High Speed Triple Line Receiver	MC10216	MC10616	1.8	100	620,648,650
High Speed Dual Type D Master-Slave Flip-Flop	MC10231	MC10631	f = 225 MHz	270	620,648,650
High Speed 2 x 1 Bit Array Multiplier Block	MC10287	–	–	400	620

① L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, F suffix denotes flat package (i.e., MC10100L = Ceramic Dual In-Line Package, MC10100P = Plastic Dual In-Line Package and MC10500F = Ceramic Flat Package.)

*Load Power not included

DATA SELECTORS/MULTIPLEXERS (continued)

MC10174 / MC10574
Dual 4 to 1 Multiplexer

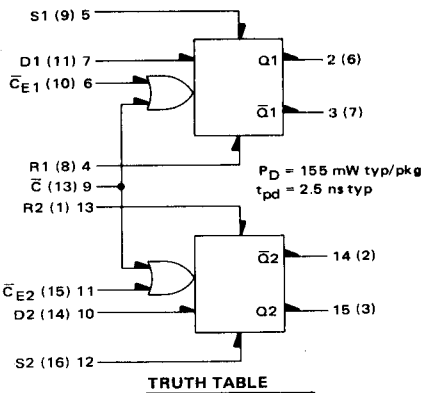


TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	B	A	Z	W
H	ϕ	ϕ	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

ϕ = Don't Care

MC10130 / MC10530
Quad Latch



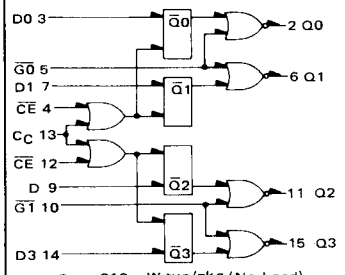
TRUTH TABLE

D	$\overline{C}$	$\overline{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
ϕ	L	H	Q_n
ϕ	H	L	Q_n
ϕ	H	H	Q_n

ϕ = Don't Care.

LATCHES

MC10133 / MC10533
Quad Latch



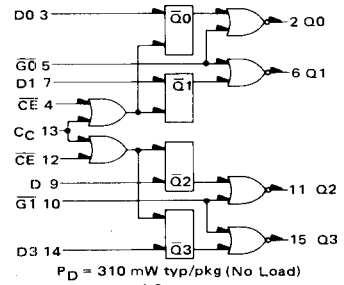
PD = 310 mW typ/pkg (No Load)
tpd = 4.0 ns typ

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

ϕ = Don't Care
C = $\overline{C}_C$ + CE

MC10153
Quad Latch



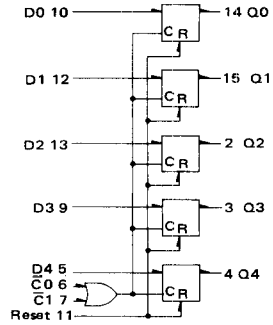
PD = 310 mW typ/pkg (No Load)
tpd = 4.0 ns typ

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	H	ϕ	Q_n
L	L	L	L
L	L	H	H

ϕ = Don't Care
C = $\overline{C}_C$ + CE

MC10175 / MC10575
Quint Latch



PD = 400 mW typ/pkg (No Load)
tpd = 2.5 ns typ

TRUTH TABLE

D	C0	C1	Reset	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
ϕ	H	ϕ	L	Q_n
ϕ	ϕ	H	L	Q_n
ϕ	H	ϕ	H	L
ϕ	ϕ	H	H	L

QUAD LATCH

MC10153

Advance Information

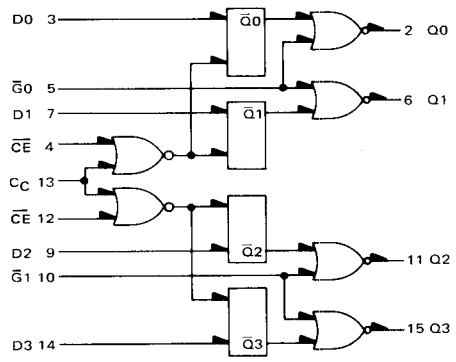
The MC10153 is a high speed, low power, MECL quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire-ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is low, outputs will follow D inputs. Information is latched on positive going transition of the clock. The MC10153 provides the same logic function as the MC10133, except for inversion of the clock.

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	H	ϕ	Q_n
L	L	L	L
L	L	H	H

ϕ = Don't Care
$C = C_C + \overline{CE}$

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

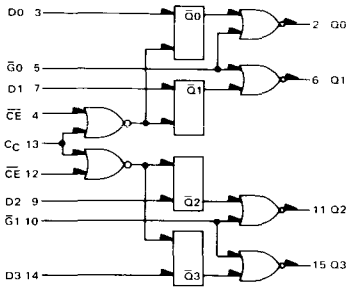


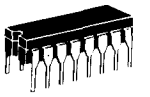
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

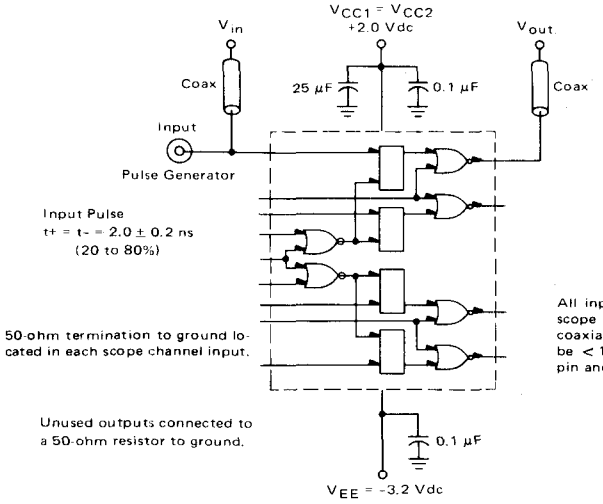
Characteristic	Symbol	Pin Under Test	MC10153L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	75	–	–	mAdc	–	13	–	–	8	1,16
Input Current	I_{inH}	3	–	–	–	–	245	–	–	µAdc	3	–	–	–	8	1,16
		4	–	–	–	–	290	–	–		4	–	–	–		
		5	–	–	–	–	350	–	–		5	–	–	–		
		13	–	–	–	–	350	–	–		13	–	–	–		
	I_{inL}	3	–	–	0.5	–	–	–	–	µAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	3	4	–		8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3	13	–		8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	–	3,13	–	–	8	1,16
		2									3,5	13	–	–		
		2									–	3,4	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	3	4	–	5	8	1,16
		2		–		–	–		–		–	4	3	–		
		2		–		–	–		–		3	4		–		
		2†		–		–	–		–		3	–		–		
		2††		–			–		–		–	–	–	–		
		2††					–		–		–	–	–	–		
		2		–		–	–		–		3		–	4		
		2		–		–	–		–		3	–	–	13		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	3	4	5	–	8	1,16
		2			–	–		–			–	4	–	3		
		2	–		–	–		–			–	4	–	–		
		2†	–		–	–		–			–	–	–	–		
		2††	–			–		–			3	–	–	–		
		2††	–			–		–			3	–	–	13		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	–	–	–	3.0	–	–	–	ns	–	–	3	2	8	1,16
	t_{13+2+}	2	–	–	–	4.0	–	–	–		3 *	–	4	2		
	t_{5-2+}	2	–	–	–	2.0	–		–		–	–	5	2		
	t_{Setup}	3	–	–	–	0.7	–		–		–	–	3	2		
	t_{Hold}	3	–	–	–	0.7	–	–	–		–		3	2		
Rise Time (20% to 80%)	t_{2+}	2	–	–	–	2.0	–	–	–		–	–	3	2		
Fall Time (20% to 80%)	t_{2-}	2	–	–	–	2.0	–	–	–		–	–	3	2		

†Output level to be measured after a clock pulse has been applied to the clock input (Pin 4). V_{IH} max / V_{IL} min

††Data input at proper high/low level while clock pulse is low so that device latches at proper high/low level for test. Levels are measured after device has latched.

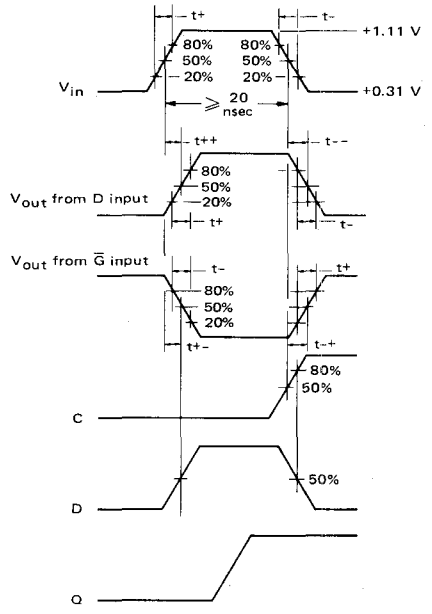
*Latch set to zero state before test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

PROPAGATION DELAY



t_{setup} is minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).